LV52400XA

Product Preview

Triple Output Power Supply, For AMOLED

Overview

The LV52400XA is a Triple Output Power Supply composed with 2 boost voltages and 1 inverting Buck-boost negative voltage required by AMOLED.

Features

- 2.9 V to 4.5 V Input Voltage Range
- External Output Sense Pin for VPOS and VNEG
- Excellent Line Transient Regulation
- High Accuracy Output Voltage
- VPOS = 5.0 V, 4.8 V, 4.6 V or 4.4 V selectable, default 4.6 V
- VAVDD = 7.6 V, 6.9 V, 6.2 V or 5.5 V selectable, default 7.6 V
- Selectable VNEG = −1.4 V to −5.4 V, default −2.4 V
- 300 mA Output Current for VPOS and VNEG
- Short Circuit Protection
- Thermal Shutdown
- 1.97 mm × 1.97 mm × 0.60 mm WLCSP25
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- AMOLED Display BIAS

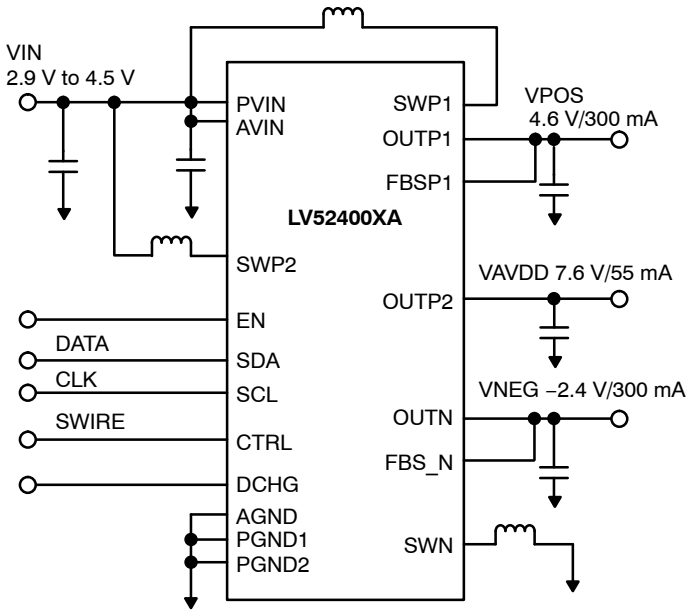

Figure 1.

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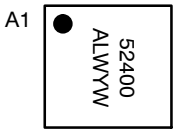
WLCSP25
CASE 567UY

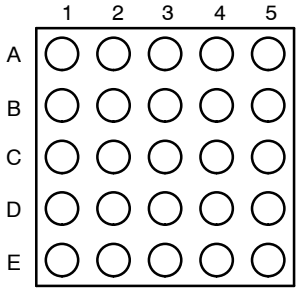
MARKING DIAGRAM



(Top View)

• = Device Mark
A = Assembly Site Code
LW = Lot Code
YW = Date Code

PIN ASSIGNMENT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
LV52400XATAG	WLCSP25 (Pb-Free/ Halogen Free)	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Units
Pin Voltage	PVIN, AVIN,EN, CTRL, CLK, DATA, SWP1, OUTP1, FBSP1		−0.3	6	V
	OUTP2, SWP2		−0.3	10	V
	OUTN, FBS_N		−6.5	0.3	V
	SWN		−6.5	5.5	V
Allowable Power Dissipation	P_d max	T_A = 25°C (Note 1)	TBD		W
Operating Temperature	T_{opr}		−40	85	°C
Storage Temperature	T_{stg}		−55	125	°C
Junction Temperature	T_{jmax}		−	125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on the following board: xx mm × xx mm × xx mm (x layer glass epoxy)

ELECTRICAL CHARACTERISTICS ANALOG BLOCK

(T_A = 25°C, VIN = 3.7 V, EN = 3.7 V, VPOS = 4.6 V, VNEG = −2.4 V, VAVDD = 7.6 V, unless otherwise specified) (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE AND SUPPLY CURRENT AND THERMAL PROTECTION						
Vin	Input Voltage Range		2.9	3.7	4.5	V
Isd	Shutdown Current into VIN	CTRL = GND, EN = GND	−	0.1	−	μA
Vuvlo	Under-voltage Lockout Threshold	Vin falling	2.25	2.35	2.45	V
		Hysteresis between falling and rising	−	0.15	−	
Tsd	Thermal Shutdown Temperature	Temperature rising	−	145	−	°C
BOOST CONVERTER1 (VPOS)						
Vpos	Positive Output1 Voltage Default		−	4.6	−	V
	Output Voltage Range	0.2 V step	4.4	−	5.0	V
	Output Voltage Accuracy	T_A = 25°C, No Load	−25	−	+25	mV
		−40°C ≤ T_A ≤ 85°C. No Load	−40	−	+40	mV
Rdson1A	SWP1 MOSFET On-resistance	ISWP1 = 200 mA	−	250	−	mΩ
Rdson1B	SWP1 MOSFET Rectifier-resistance		−	350	−	mΩ
Fswp1	SWP1 Switching Frequency	Ipos = 200 mA	−	1.5	−	MHz
Iswp1	SWP1 Switching Current Limit		0.8	1	−	A
Vpos (scp)	Short Circuit Threshold in Operation	Percentage of nominal VPOS	−	90	−	%
Tpos (scp)	Short Circuit Detection Time in Operation		−	3	−	ms
RDCHG1	Discharge Resistance	CTRL = GND, VPOS = 0.1 V	−	30	−	Ω
Vposline	Line Regulation	Ipos = 200 mA	−	0.01	−	%/V
Vposload	Load Regulation	1 mA ≤ Ipos ≤ 300 mA	−	0.02	−	%/A
INVERTING BUCK-BOOST CONVERTER (VNEG)						
Vneg	Output Voltage Default		−	−2.4	−	V
	Output Voltage Range	0.1 V step	−1.4	−	−5.4	V
	Output Voltage Accuracy	T_A = 25°C, No Load	−50	−	50	mV
		−40°C ≤ T_A ≤ 85°C. No Load	−60	−	60	mV

ELECTRICAL CHARACTERISTICS ANALOG BLOCK (continued)
(T_A = 25°C, VIN = 3.7 V, EN = 3.7 V, VPOS = 4.6 V, VNEG = −2.4 V, VAVDD = 7.6 V, unless otherwise specified) (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INVERTING BUCK-BOOST CONVERTER (VNEG)						
RdsonNA	SWN MOSFET On-resistance	ISWN = 200 mA	–	250	–	mΩ
RdsonNB	SWN MOSFET Rectifier-resistance		–	350	–	mΩ
Fswn	SWN Switching Frequency	Ineg = 10 mA	–	1.5	–	MHz
Iswn	SWN Switching Current Limit		1.2	1.5	–	A
VscpN	Short Circuit Threshold in Operation	Voltage increase from nominal VNEG	–	500	–	mV
TscpN	Short Circuit Detection Time in Operation		–	3	–	ms
RDCHGN	Discharge Resistance	CTRL = GND, VNEG = −0.1 V	–	150	–	Ω
Vnegline	Line Regulation	Ineg = 200 mA	–	0.004	–	%/V
Vnegload	Load Regulation	1m A ≤ Ineg ≤ 300 mA	–	0.1	–	%/A
BOOST CONVERTER2 (VAVDD)						
VAVDD	Output Voltage		–	7.6	–	V
	Output Voltage Range	0.7 V step	5.5	–	7.6	V
	Output Voltage Accuracy	T_A = 25°C, No Load	−80	–	80	mV
		−40°C ≤ T_A ≤ 85°C. No Load	−100	–	100	mV
Rdson2A	SWP2 MOSFET On-resistance	ISWP2 = 55 mA	–	500	–	mΩ
Rdson2B	SWP2 MOSFET Rectifier-resistance		–	1200	–	mΩ
Fswp2	SWP2 Switching Frequency	IAVDDs = 0 mA	–	1.5	–	MHz
Iswp2	SWP2 Switching Current Limit		0.25	0.35	–	A
Vavdd (scp)	Short Circuit Threshold in Operation	Percentage of nominal VAVDD	–	90	–	%
Tavdd (scp)	Short Circuit Detection Time in Operation		–	3	–	ms
RDCHG2	Discharge Resistance	CTRL = GND, VAVDD = 0.1 V	–	30	–	Ω
Vavddline	Line Regulation	IAVDD = 55 mA	–	0.04	–	%/V
Vavddload	Load Regulation	1 mA ≤ IAVDD ≤ 55 mA	–	0.30	–	%/A
DCHG PIN INTERFACE						
DCIH	Logic input high level voltage		0.9 × Vin	–	–	V
DCIL	Logic input low level voltage		–	–	0.1 × Vin	V
CTRL and EN PIN INTERFACE						
VIH	Logic Input High Level Voltage		1.2	–	–	V
VIL	Logic Input Low Level Voltage		–	–	0.4	V
Rpden	Pull-down Resistance	EN	–	500	–	kΩ
Rpdct		CTRL	–	500	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
2. Limits mentioned with temperature range are verified by design.

BLOCK DIAGRAM

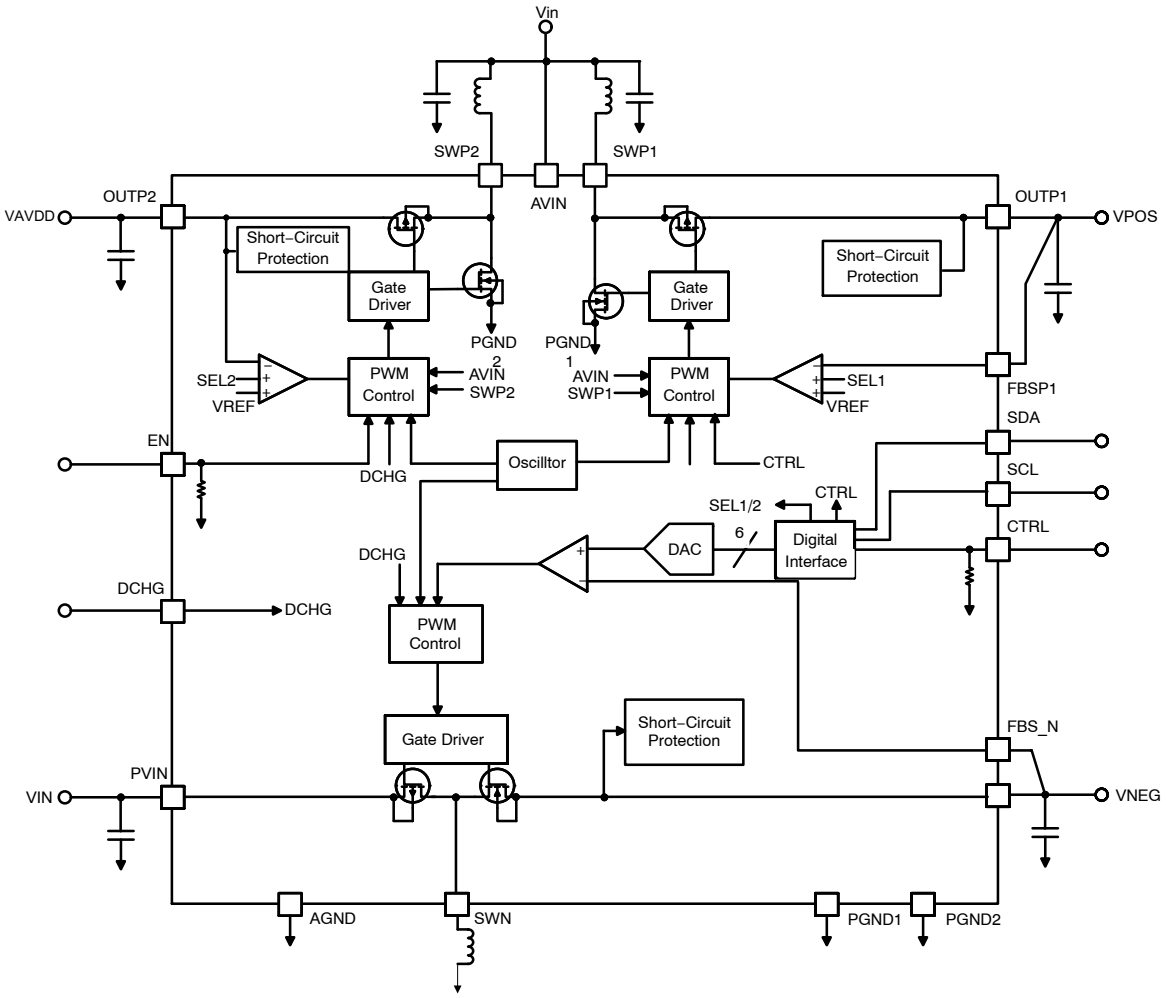
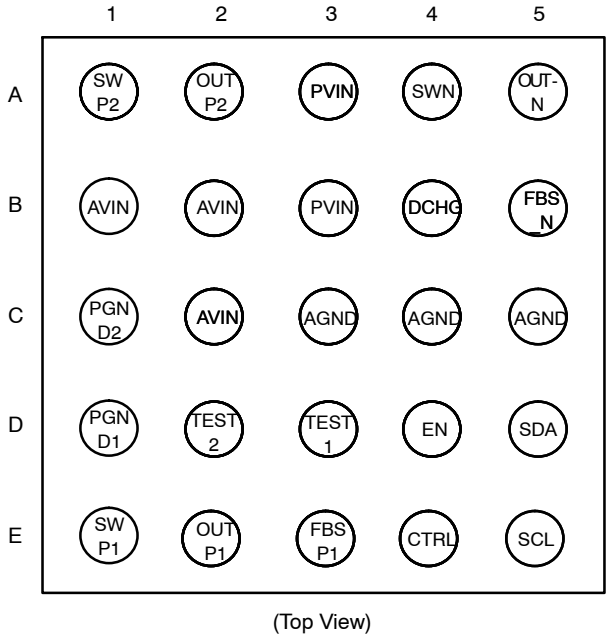


Figure 2. Block Diagram

PIN INFORMATION



(Top View)

Figure 3. Pin Assignment

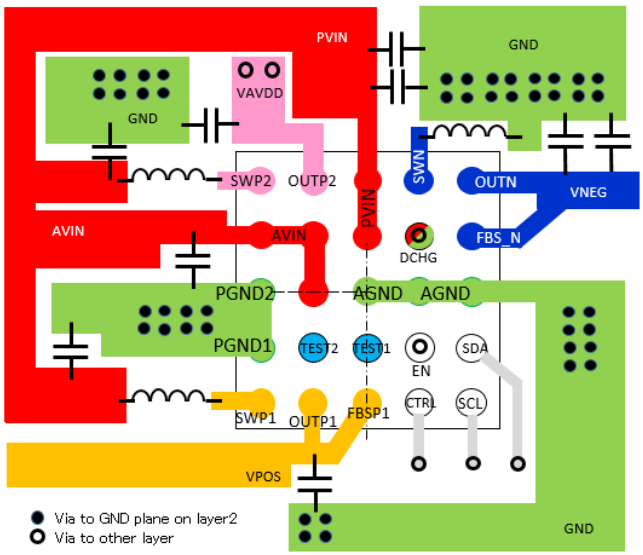


Figure 4. Recommended PCB Layout Image

Table 1. PIN FUNCTION

Pin No.	Pin Name	Description
A1	SWP2	Boost converter2 switch pin
A2	OUTP2	Boost converter2 output (VAVDD)
A3, B3	PVIN	Inverting buck-boost converter power stage supply voltage
A4	SWN	Inverting buck-boost converter switch pin
A5	OUTN	Inverting buck-boost converter output (VNEG)
B1, B2, C2	AVIN	Supply voltage for the device
B4	DCHG	Discharge select PIN (GND is discharge OFF mode for all 3 outputs)
B5	FBS_N	Inverting buck-boost converter (VNEG) sense input
C1	PGND2	Boost converter2 power ground
C3, C4, C5	AGND	Analog ground
D1	PGND1	Boost converter1 power ground
D2	TEST2	No connection (for Test Mode only)
D3	TEST1	No connection (for Test Mode only)
D4	EN	Boost converter2 (AVDD) enable
D5	SDA	DATA line of I^2C BUS control
E1	SWP1	Boost converter1 switch pin
E2	OUTP1	Boost converter1output (VPOS)
E3	FBSP1	Boost converter1 (VPOS) sense input
E4	CTRL	Control line for Single Wire control
E5	SCL	CLK line of I^2C BUS control

GENERAL POWER ON FLOWCHART

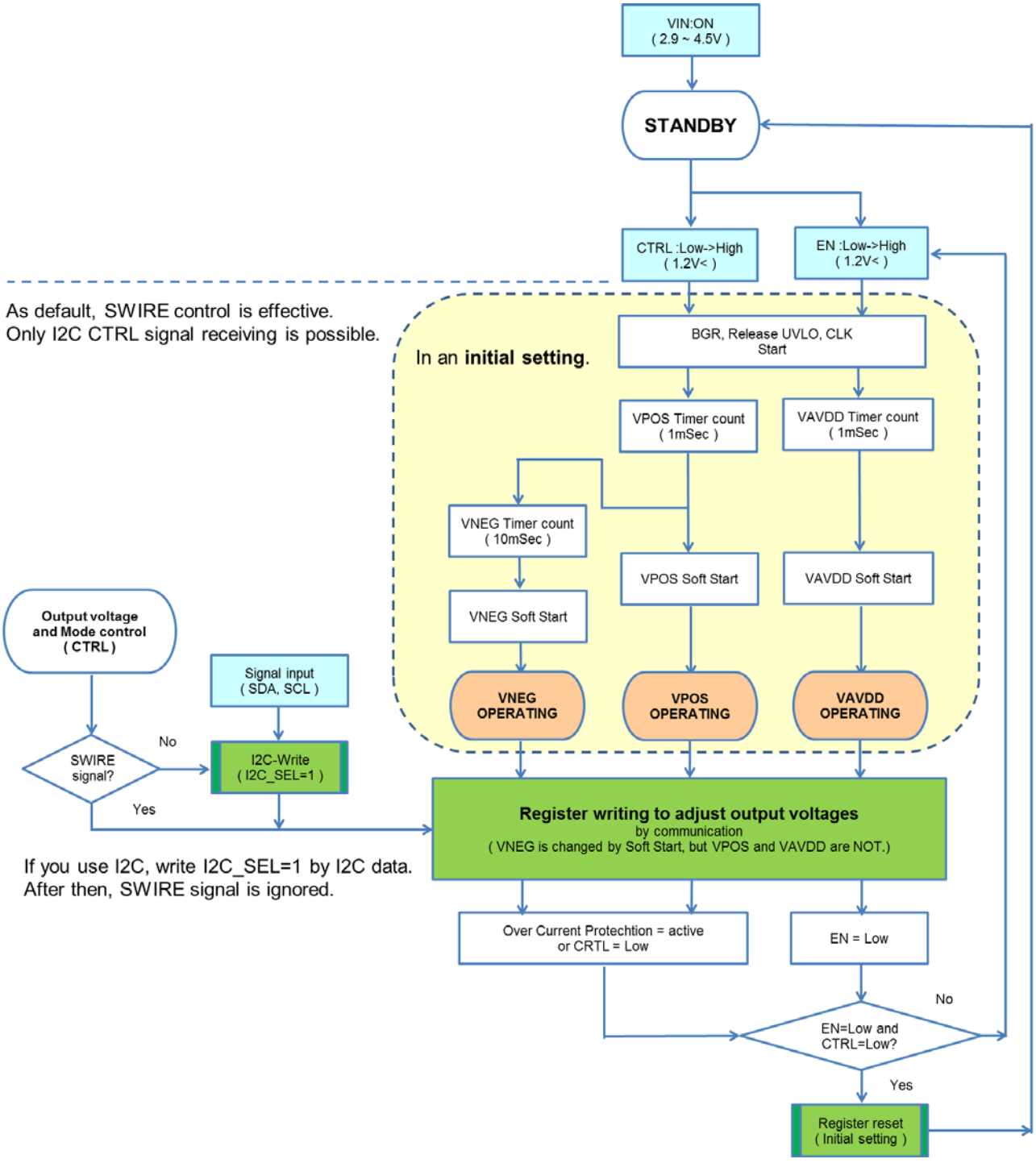


Figure 5. General Power ON Flowchart

DESCRIPTION

1. Boost Converters for Panel Power Supply (VPOS and VNEG)

Both boost and inverting buck-boost converters operate with fixed-frequency current-mode topology. They have a dedicated output sense pin (FBSP1 and FBS_N) on each. Maximum output current is 300 mA and the output voltage can be programmed by communication. VPOS is selectable for 5.0/4.8/4.6 and 4.4 V and VNEG can be programmed from −1.4 V to −5.4 V with 0.1 V steps. Each default setting are 4.6 V and −2.4 V. Both output have superior Line and Load Regulation properties.

2. Output Sense (FBSP1 and FBS_N)

VPOS and VNEG have dedicated output sense pin to get higher precision for each output voltage.

3. Discharge mode selection (DCHG)

Discharge mode can be selected by the condition of DCHG pin. It is common setting for all 3 outputs. In the case of pulled-high, discharge is performed at shutdown. If it was pulled-low to GND, discharging function is turned off. It can be controlled by I^2C communication after setting select DCHGOFF_SEL High.

4. Boost Converter 2 for Display Driver IC (VAVDD)

Boost converter 2 uses a fixed-frequency current-mode topology. Maximum output current is 55 mA and the output voltage is selectable for 7.6/6.9/6.2 and 5.5 V with 0.7 V steps by communication. The default setting is 7.6 V.

5. Enable for VAVDD (EN)

Boost converter 2 and others are operated individually. EN pin is to enable and disable only for VAVDD.

6. Enable and programming for VPOS and VNEG (CTRL)

The CTRL pin serves two functions: one is to enable and disable for VPOS and VNEG output, and the other is to program the output voltages. When either EN or CTRL is High, this device can receive the communication signal. When it is used only enable, CTRL is pulled high, and change disable with pulled-low.

All output voltages can be programmed in discrete steps with using simple digital interface. Please refer to Figure 6 for the timing details. When CTRL is pulled high the device starts up with its default voltages 4.6 V and –2.4 V. To control for VNEG, there is a 6-bit DAC that generates the output voltages shown in Negative output voltage levels. The interface counts the rising edges applied to the CTRL pin once the device is enabled. According to Negative output voltage levels, VNEG is programmed to –5.2 V since 39 rising edges are detected. In addition, this device can be changed PFM Mode by Programming. PFM Mode is used at light load (ex. Always ON mode).

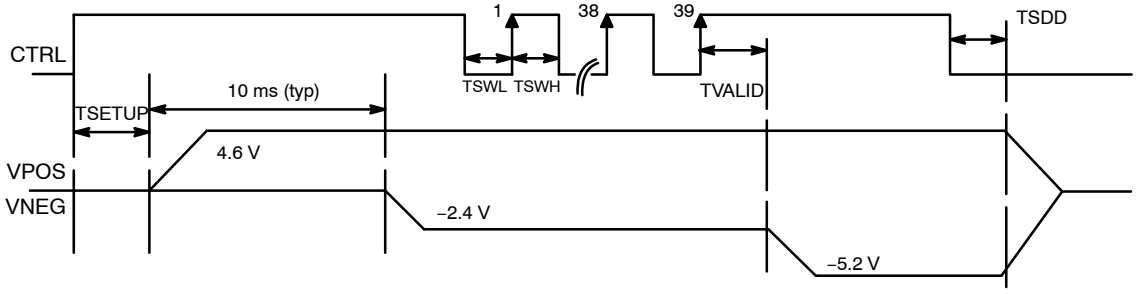


Figure 6. Digital Interface Using CTRL

Table 2. TRIPLE OUTPUT VOLTAGE LEVELS AND PFM MODE (BY SWIRE)
(Default: VNEG = −2.4 V, VPOS = 4.6 V, VAVDD = 7.6 V and Normal Mode)

Pulse	VNEG [V]	Pulse	VNEG [V]	Pulse	VNEG [V]	Pulse	VNEG [V]
1	−1.4	12	−2.5	23	−3.6	34	−4.7
2	−1.5	13	−2.6	24	−3.7	35	−4.8
3	−1.6	14	−2.7	25	−3.8	36	−4.9
4	−1.7	15	−2.8	26	−3.9	37	−5.0
5	−1.8	16	−2.9	27	−4.0	38	−5.1
6	−1.9	17	−3.0	28	−4.1	39	−5.2
7	−2.0	18	−3.1	29	−4.2	40	−5.3
8	−2.1	19	−3.2	30	−4.3	41	−5.4
9	−2.2	20	−3.3	31	−4.4		
10	−2.3	21	−3.4	32	−4.5		
11	−2.4	22	−3.5	33	−4.6		

Pulse	VPOS [V]	Pulse	VAVDD [V]	Pulse	Mode	Pulse	Mode
42	4.4	46	5.5	50	EL PFM	57	Reserved
43	4.6	47	6.2	51	EL Normal	58	Reserved
44	4.8	48	6.9	52	VAVDD PFM	59	Reserved
45	5.0	49	7.6	53	VAVDD Normal	60	Reserved
				54	Reserved	61	Reserved
				55	Reserved	62	Reserved
				56	Reserved	63	Initial Reset

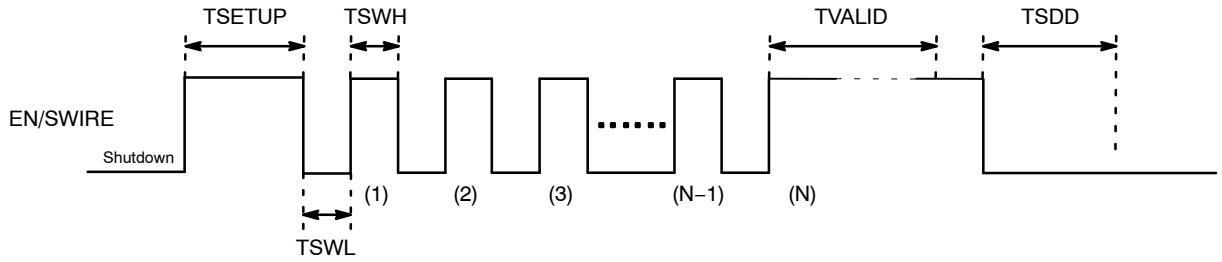


Figure 7. SWIRE Programming Diagram

Table 3. SWIRE

(T_A = 25°C, VIN = 3.7 V, EN = 3.7 V, VPOS = 4.6 V, VNEG = −2.4 V, VAVDD = 7.6 V, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SWIRE Setup Time from shutdown	TSETUP		300	–	–	μs
SWIRE High	TSWH		2	10	20	μs
SWIRE Low	TSWL		2	10	20	μs
Time to Valid Data	TVALID		–	300	400	μs
Time to Shut Down Delay	TSDD		–	85	–	μs
Time between First SWIRE Data to VPOS Startup	TDTM1		1	–	–	μs
Time Wait after Data	TDTM2		1	–	–	μs
SWIRE Rising Time	TR		–	–	200	ns
SWIRE Falling Time	TF		–	–	200	ns
Input SWIRE Frequency	FSWFR		–	–	250	kHz

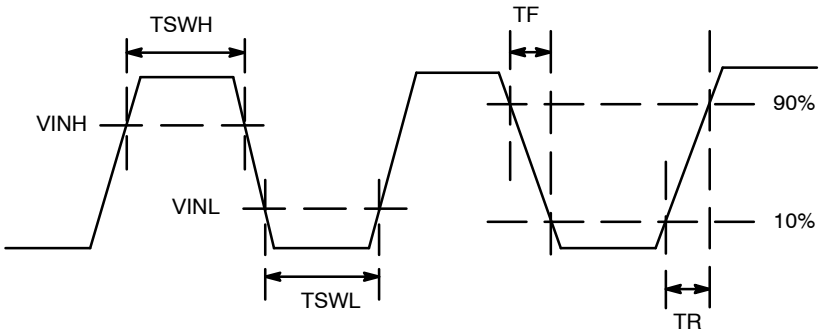


Figure 8. SWIRE Logic Diagram

7. I²C Serial Bus Communication (SDA, SCL)

BITMAP (I²C control) / I²C disable at standby

IC Address: 0111110 and 0: Write mode or 1: Read mode.

Table 4. SERIAL BUS COMMUNICATION SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STANDARD MODE						
SCL Clock Frequency	fscl	SCL clock frequency	0	–	100	kHz
Data Set Up Time	ts1	SCL setup time relative to the fall of SDA	4.7	–	–	μs
	ts2	SDA setup time relative to the rise of SCL	250	–	–	ns
	ts3	SCL setup time relative to the rise of SDA	4.0	–	–	μs
Data Hold Time	th1	SCL data hold time relative to the rise of SDA	4.0	–	–	μs
	th2	SDA hold time relative to the fall of SCL	0	–	–	μs
Pulse Width	twL	SCL pulse width for the L period	4.7	–	–	μs
	twH	SCL pulse width for the H period	4.0	–	–	μs
Input Waveform Conditions	ton	SCL and SDA (input) rise time	–	–	1000	ns
	tof	SCL and SDA (input) fall time	–	–	300	ns
Bus Free Time	tbuf	Time between STOP and START conditions	4.7	–	–	μs
FAST MODE						
SCL Clock Frequency	fscl	SCL clock frequency	0	–	400	kHz
Data Setup Time	ts1	SCL setup time relative to the fall of SDA	0.6	–	–	μs
	ts2	SDA setup time relative to the rise of SCL	100	–	–	ns
	ts3	SCL setup time relative to the rise of SDA	0.6	–	–	μs
Data Hold Time	th1	SCL data hold time relative to the rise of SDA	0.6	–	–	μs
	th2	SDA hold time relative to the fall of SCL	0	–	–	μs
Pulse Width	twL	SCL pulse width for the L period	1.3	–	–	μs
	twH	SCL pulse width for the H period	0.6	–	–	μs
Input Waveform Conditions	ton	SCL and SDA (input) rise time	–	–	300	ns
	tof	SCL and SDA (input) fall time	–	–	300	ns
Bus Free Time	tbuf	Time between STOP and START conditions	1.3	–	–	μs

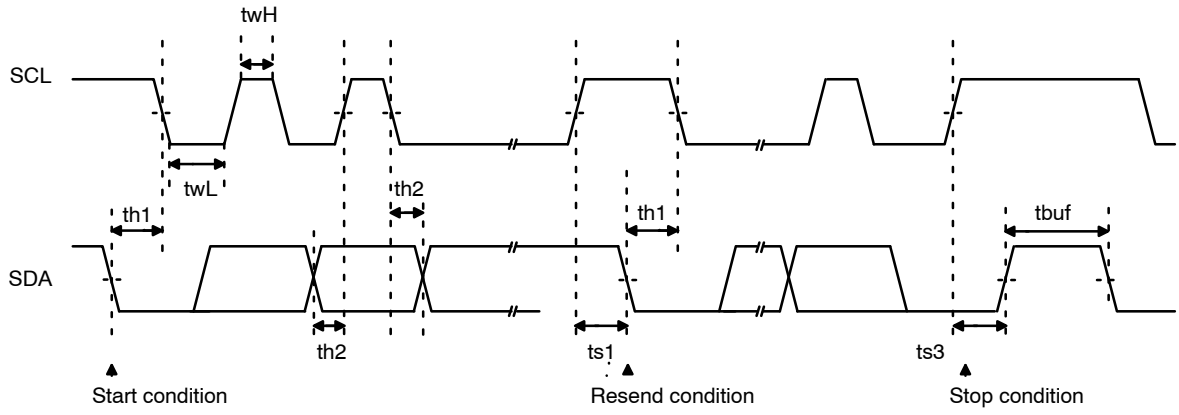


Figure 9. I²C Serial Transfer Timing Conditions

Input Waveform Condition and I²C Control Transmission Method

In start and stop conditions of the I²C bus, SDA should be, kept in the constant state while SCL is “H” as shown below during data transfer.

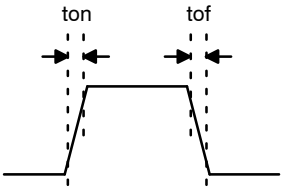


Figure 10.

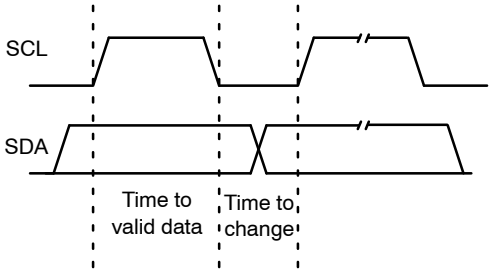


Figure 11.

When data transfer is not made, both SCL and SDA are in the “H” state.

When SCL = SDA = “H”, change of SDA from “H” to “L” enables the start conditions to start access.

When SCL is “H”, change of SDA from “L” to “H” enables the stop conditions to stop access.

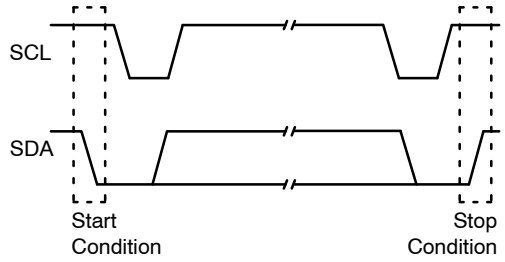


Figure 12.

Data Transfer and Acknowledgement Response

After establishment of start conditions, Data transfer is made by one byte (8-bits). Data transfer enables continuous transfer of any number of bytes. Each time of the 8-bit data is transferred, the ACK signal is sent from the receive side to the send side. The ACK signal is issued when SDA (on the send side) is released and SDA(on the receive side) is set “L” immediately after fall of the clock pulse at the SCL eighth bit of data transfer to “L”. When the next 1-byte transfer is left in the receive state after transmission of the ACK signal from the receive side, the receive side releases SDA at fall of the SCL ninth clock.

In the I²C bus, there is no CE signal. Instead, 7-bit slave address is assigned to each device and the first byte of transfer is assigned to the command (R/W) representing the 7-bit slave address and subsequent transfer direction. Note that only WRITE is valid in this IC. The 7-bit address is transferred sequentially from MSB and the eighth bit is “L” representing WRITE.

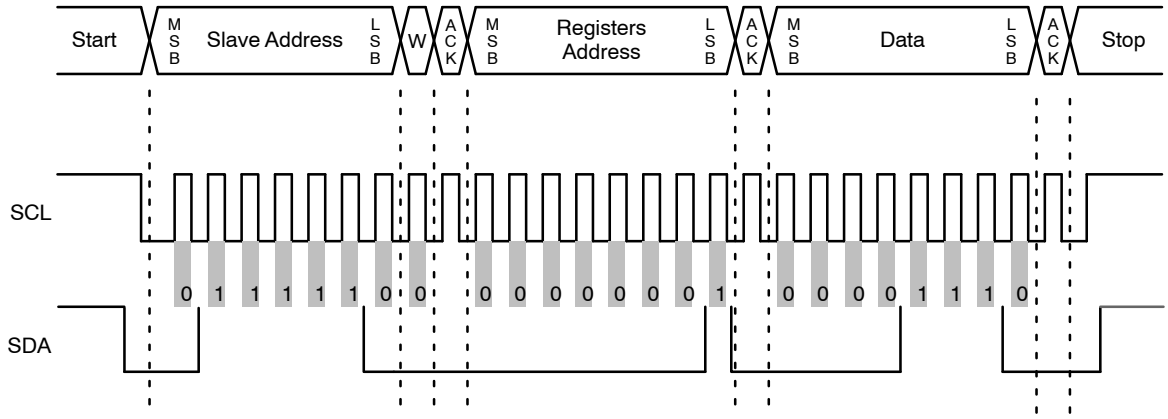


Figure 13. Input 1 Data

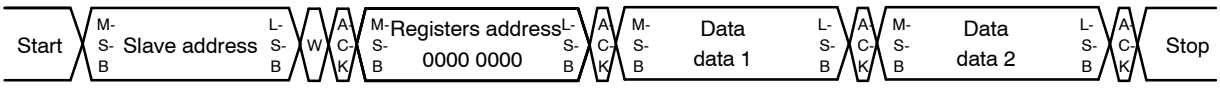
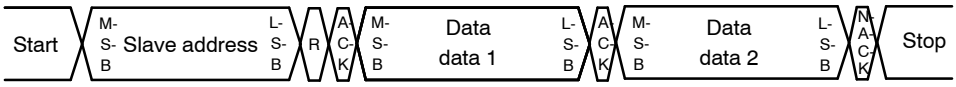


Figure 14. Input 2 Data (Register Address Auto Increment)



*NACK ← Notify end of read by not sending out ACK

Figure 15. Output 2 Data (Register Address Auto Increment)

Table 5. IC ADDRESS: 0111110 AND 0: WRITE MODE OR 1: READ MODE

Sub_ Address	Access	MSB							LSB
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	R/W	I2C_SEL	DCHG OFF_SEL	DCHG_ POS	DCHG_ NEG	DCHG_ AVD	DCM_ POS	DCM_ NEG	DCM_ AVD
		0	0	0	0	0	0	0	0
1	R/W	I2C_NEG_LVL[5:0]						–	
		0	1	1	1	0	0	–	
2	R/W	I2C_POS_LVL[1:0]		I2C_AVDD_LVL[1:0]		–	–	–	–
		0	1	1	1	–	–	–	–

For Test mode allocation, you must not order to Address 3 – 31.

Table 6. DESCRIPTION FOR EACH ITEM IN BITMAP

Item	Function	0 (min)	1 (max)
I2C_SEL	Select communication method	SWIRE	I^2C
DCHGOFF_SEL	Select control of discharge OFF mode	External Pin	I^2C
DCHG_POS	Select VPOS discharge mode	Discharge OFF	Discharge ON
DCHG_NEG	Select VNEG discharge mode	Discharge OFF	Discharge ON
DCHG_AVD	Select VAVDD discharge mode	Discharge OFF	Discharge ON
DCM_POS	Select VPOS operation mode	Normal	PFM
DCM_NEG	Select VNEG operation mode	Normal	PFM
DCM_AVD	Select VAVDD operation mode	Normal	PFM
I2C_NEG_LVL	Select VNEG output voltage	–1.4 V	–5.4 V
FUSE_READ	Select FUSE_READ Mode	Normal	FUSE Read
I2C_POS_LVL	Select VPOS output voltage	4.4 V	5.0 V
I2C_AVDD_LVL	Select VAVDD output voltage	5.5 V	7.6 V

8. Soft Start and Start-Up Sequence

The devices feature a soft-start function to limit inrush current. Boost converter 2 (VAVDD) is enabled when EN goes high. When CTRL goes high, boost converter 1 starts with a reduced switch current limit and 10 ms later the inverting buck-boost converter (VNEG) starts with its default value of –2.4 V. The typical start-up sequence is shown in Figure 16. The two boost converters operate independently and boost converter 1 (VPOS) does not require boost converter 2 (VAVDD) to be in regulation in order for it to start.

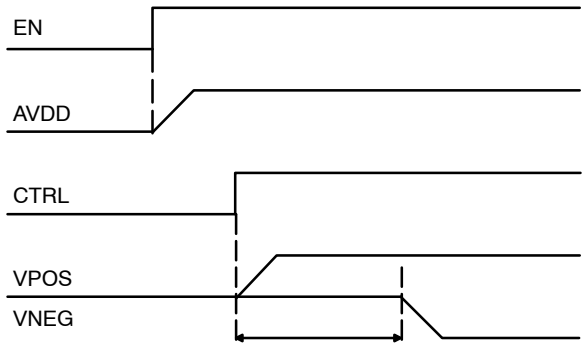


Figure 16. Start-Up Sequence

9. TEST1, TEST2

This is a test pin for characteristic verification to use internal evaluation. Floating is preferable.

10. Short Circuits During Operation

The device is protected against short circuits of VPOS and VNEG to ground and short circuit of these two outputs to each other. During normal operation an error condition is detected if VPOS falls below 90% for longer than 3 ms or VNEG is pulled above the programmed nominal output by 500 mV for longer than 3 ms. In either case the device goes into shutdown and the outputs are disconnected from the input. This state is latched, and to resume normal operation, VI has to cycle below the undervoltage lockout threshold, or CTRL has to toggle LOW and then HIGH.

11. Thermal Shutdown

The LV52400 device enters thermal shutdown if its junction temperature exceeds 145°C (typical). During thermal shutdown none of the device's functions are available. The thermal design which does not work this function is needed by affect concern of damage or reliability. If it becomes under 115°C (typical), the switching operation is resumed with normal operation. However, the register setting will be initialized as re-started.

12. Undervoltage Lockout

The device features an undervoltage lockout function that disables it when the input supply voltage is too low for proper operation.

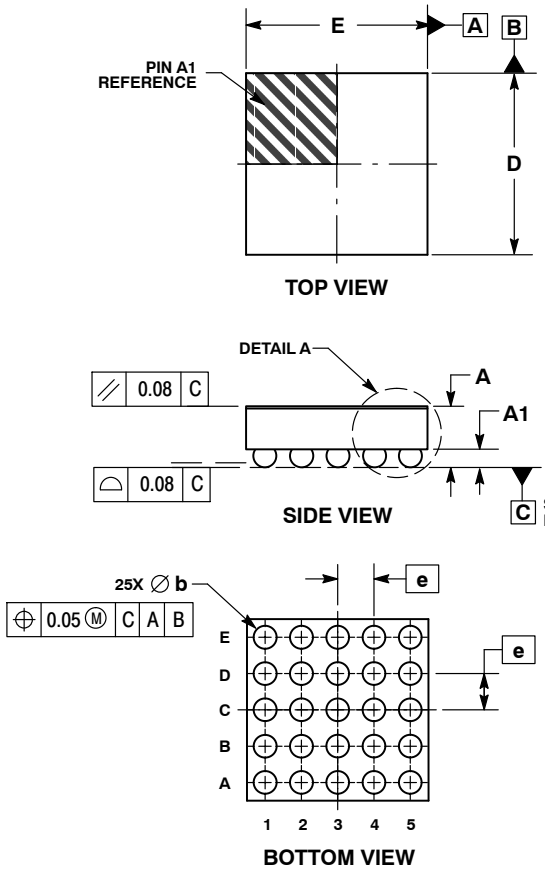
The recommended minimum input supply voltage for full-performance is 2.9V. The device continues to operate with input supply voltages below 2.9 V, however, full performance is not guaranteed.

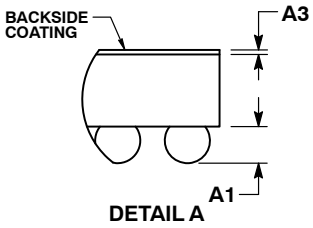
13. Operation with VIN ≈ VPOS (Diode Mode)

The LV52400 device features a "diode mode" that enables it to regulate its VPOS output even when the input supply voltage is close to VPOS (that is, too high for normal boost operation). When operating in diode mode the VPOS boost converter's high-side switch is disabled and its body diode used as the rectifier.

PACKAGE DIMENSIONS

WLCSP25 1.97x1.97x0.65
CASE 567UY
ISSUE O

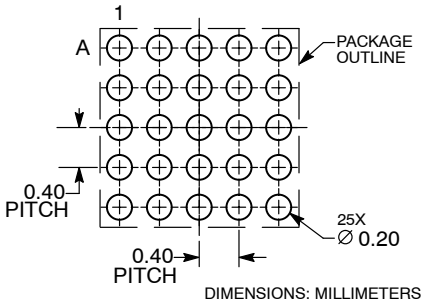




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	0.675
A1	0.16	0.21	0.26
A3		0.25 REF	
b	0.21	0.26	0.31
D	1.92	1.97	2.02
E	1.92	1.97	2.02
e		0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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