LV8316HA

12 V Single-phase BLDC Motor Driver with Speed Control

ON Semiconductor®

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TSSOP−14
EXPOSED PAD
CASE 948AW

Overview

The LV8316HA is a driver for a 12 V class single−phase BLDC motor, which controls motor rotational speed with the built−in closed loop speed controller. Its target speed can be set by input PWM duty cycle. The speed curve setting can be stored to the internal nonvolatile memory (NVM). In addition, lead−angle can also be adjusted by the configuration saved in the internal NVM. Thus, it can drive various kinds of motors at high efficiency and low noise.

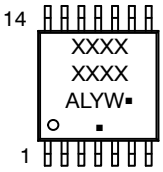
Features

- PI Closed Loop Speed Control Function
- Single−phase Full Wave Driver
- Embedded Power FETs, Iomax: 2.0 A (Peak)
- PWM Duty Cycle Input (25 Hz to 100 KHz)
- Soft Start−up Function
- PWM Soft Switching Phase Transitions
- Soft PWM Duty Cycle Transitions (Changing the Target Speed Gradually)
- Built−in Current Limit Function and Over Current Protection Function
- Built−in Thermal Protection Function
- Built−in Locked Rotor Protection and Automatic Recovery Function
- FG or RD Signal Output Selectable
- Dynamic Lead Angle Adjustment with Respect to Input Duty Cycle
- Embedded EEPROM as NVM
- Parameter Setting to the NVM (by ON Semiconductor or the Certified Programming Service Vendor)
- Pb−Free and Halogen Free

Typical Applications

- Desktop PC Cooling Fan
- Server Cooling Fan
- Refrigerator Circulation Fan
- Appliance Cooling Fan
- Power Supply Unit Cooling Fan

MARKING DIAGRAM



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
LV8316HAGR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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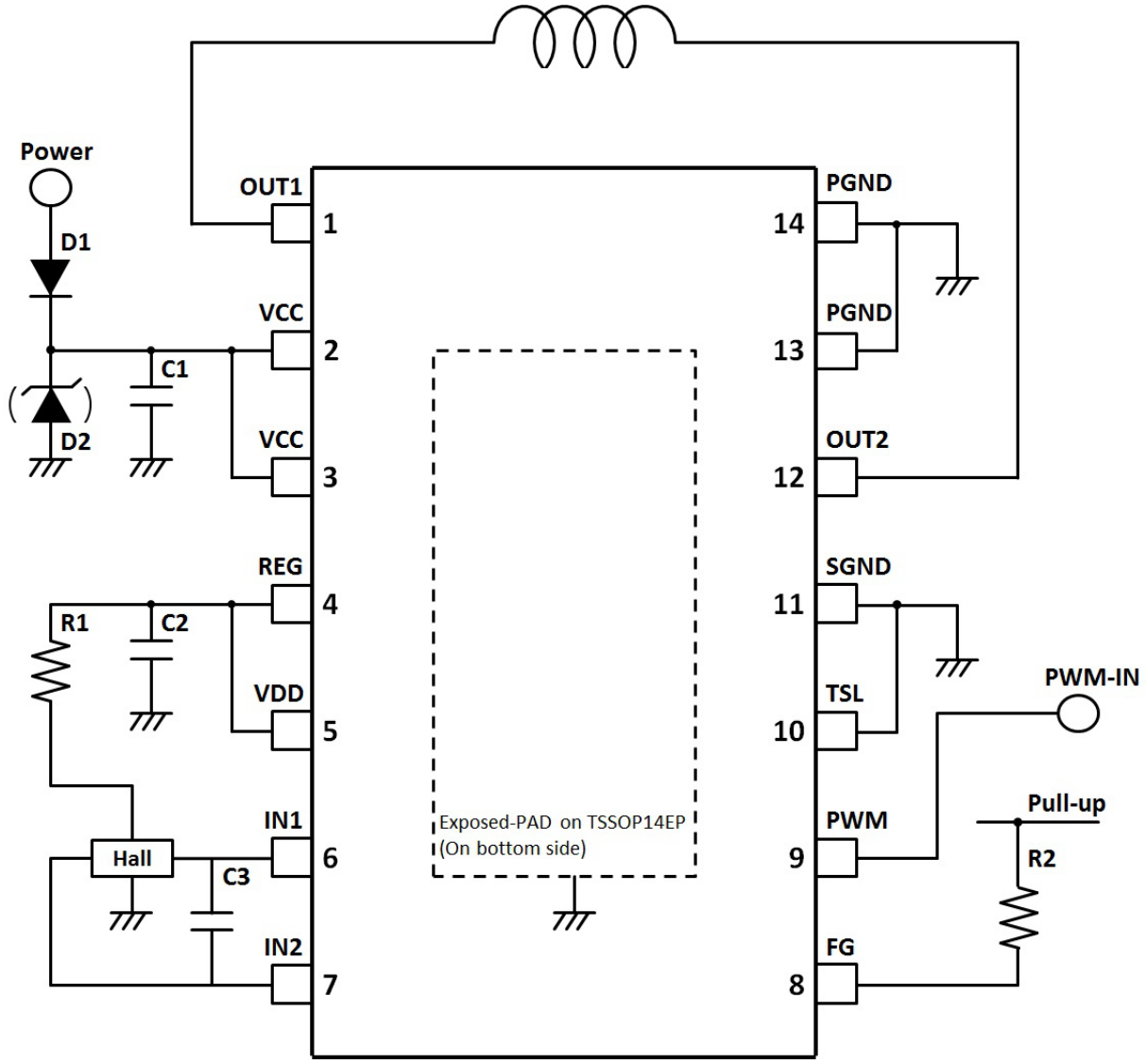


Figure 1. Application Diagram

Table 1. EXAMPLE COMPONENT VALUE

Device	Qty	Description	Value	Tol	Footprint	Manufacture	Manufacture Part Number
D1	1	Anti−reverse connection diode	−	−			
D2	1	Anti−abnormal boost Zener diode	−	−			
C1	1	VCC bypass condenser	10 μF 50 V	10%			
C2	1	REG bypass condenser	1 μF 25 V	10%			
C3	1	Filter of system noise	0.1 μF 50 V	10%			
R1	1	Current limiter resistor for Hall	2 kΩ	5%			
R2	1	FG pull−up resistor	10 kΩ	5%			
T1	1	Hall element	−	−			

APPLICATION DIAGRAM

Please refer to Table 7 “PIN DESCRIPTION” as well.

VCC, SGND and PGND (VCC, SGND, PGND)

Since PGND line has to tolerate a surge current, separate it from the SGND pin as far away as possible and connect it point−to−point to the ground side of the capacitor (C1) between VCC and PGND.

The Zener diode (D2) is mandatory to prevent the IC break down if the supply voltage exceeds the absolute maximum ratings due to the kickback voltage.

Hall−Sensor Input Pins (IN1, IN2)

Differential output signals of the hall sensor are to be interfaced at IN1 and IN2. It is recommended that the capacitor (C3) is connected between both pins to filter system noise. When a Hall IC is used, the output of the Hall IC must be connected to the IN1 pin. On the other hand, the IN2 pin must be kept in the middle level of the Hall IC power supply voltage.

Command Input Pin (PWM)

This pin reads the duty cycle of the PWM pulse which controls rotational speed. The PWM input signal level is supported from 2.8 V to 5.5 V. DC voltage cannot control the rotational speed. When the pin is not used, it must be connected to ground. The minimum pulse width is 100 ns.

Current Limiter Resistor for Hall (R1)

Hall signal amplitude depends on the ratio between R1 value and Hall resistance value “Rh”. Hall bias level “VH” is calculated as below.

VH = VREG*(Rh/(Rh+R1))

The higher the VH value is, the larger the Hall signal amplitude is. But it should be considered with Hall sensor specification and Hall bias current.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VCC_{MAX}	VCC1/VCC2 pin	20	V
Maximum output voltage	V_{OUTMAX}	OUT1/OUT2 pin	20	V
Maximum output current (Note 1)	I_{OUTMAX}	OUT1/OUT2 pin	2.0	A
REG pin maximum output current	I_{REGMAX}	REG pin	20	mA
IN1/IN2 pin maximum input voltage	V_{INMAX}	IN1/IN2 pin	5.5	V
PWM pin maximum input voltage	V_{PWMMAX}	PWM pin	5.5	V
FG pin withstanding voltage	V_{FGMAX}	FG pin	20	V
Allowable power dissipation (Note 2)	Pd_{MAX}	LV8316HA	0.93	W
Operating temperature	T_{OP}		−40 to +105	°C
Storage temperature	T_{STG}		−55 to +150	°C
Maximum junction temperature	Tjmax		150	°C
Moisture Sensitivity Level (MSL) (Note 3)	MSL		1	−
Lead Temperature Soldering Pb−Free Versions (30s or less) (Note 4)	T_{SLD}		255	°C
ESD Human body Model : HBM (Note 5)	ESD_{HBM}		±2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $IOUT_{MAX}$ is the peak value of the motor supply current.
2. Specified circuit board: Toroidal shaped, the diameter is 23mm, inside diameter is 11mm and thickness is 0.8mm, glass epoxy 2−layer board which has 1 oz internal power and ground plane and 1/2 oz copper traces on top and bottom of the board. Please refer to Thermal Test Conditions on page 31.
3. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J−STD−020A
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D http://www.onsemi.com/pub_link/Collateral/SOLDERRM−D.PDF
5. ESD Human Body Model is based on JEDEC standard: JESD22−A114

Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	133.2	°C/W
Thermal Resistance, Junction−to−Case (Top) (Note 2)	$R_{\Psi JT}$	40	°C/W

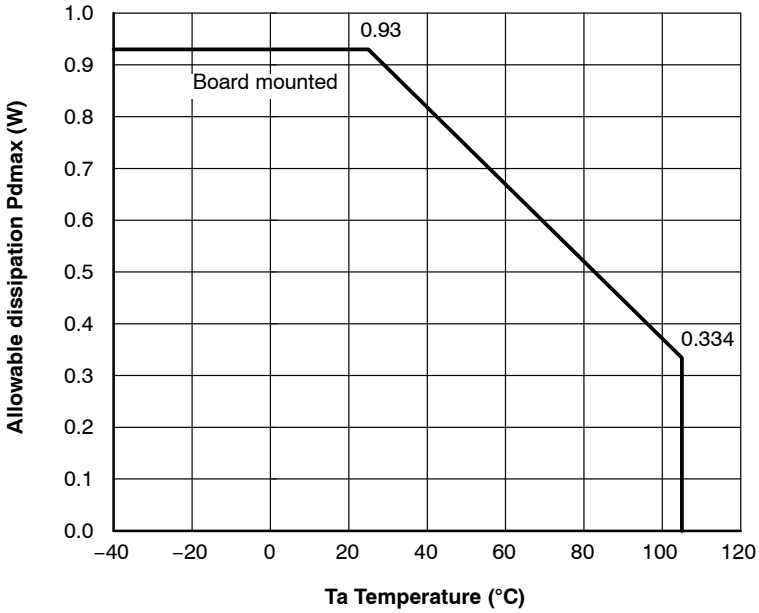


Figure 2. Power Dissipation vs. Ambient Temperature Characteristic

Table 4. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Conditions	Ratings	Unit
VCC supply voltage	VCC_{TYP}	VCC1/VCC2 pin	12	V
VCC operating supply voltage range1	VCC_{OP1}	VCC1/VCC2 pin	6.0 to 16	V
VCC operating supply voltage range2 (Note 6)	VCC_{OP2}	VCC1/VCC2 pin	3.9 to 6.0	V
PWM input frequency range	F_{PWM}	PWM pin	25 to 100k	Hz
PWM minimum input low/high pulse width	T_{WPWM}	PWM pin	100	ns
IN1 input voltage range	V_{IN1}	IN1 pin	0 to VREG	V
IN2 input voltage range	V_{IN2}	IN2 pin	0.3 to 0.55*VREG	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. When the VCC voltage is below 6.0 V, a motor keeps rotation until to 3.9 V, normally. However there are possibility to change the electric characteristics due to low VCC.

Table 5. ELECTRICAL CHARACTERISTICS T_A = 25°C, VCC_{OP} = 12 V unless otherwise noted.

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Circuit current	ICC		3.9	12	20	mA
OUT1/OUT2 High−side on−resistance	R_{OH-ON}	I_O = 1.0 A		0.28	0.5	Ω
OUT1/OUT2 Low−side on−resistance	R_{OL-ON}	I_O = 1.0 A		0.28	0.5	Ω
OUT1/OUT2 PWM output frequency	f_{PWMO}		45.6	48	50.4	kHz
PWM pin low level input voltage	V_{PWML}		0		0.7	V
PWM pin high level input voltage	V_{PWMH}		2.8		5.5	V
PWM input resolution	Δ_{PWM}			8		Bit
FG pin low level output voltage	V_{FGL}	I_{FG} = 5 mA		0.15	0.3	V
FG pin leak current	I_{FGLK}				1	μA
REG pin output voltage	V_{REG}		4.7	5.0	5.3	V
Lock−detection time1 (Note 7)	T_{LD1}	Under rotation	0.27	0.3	0.33	S
Lock−detection time2 (Note 8)	T_{LD2}	Start−up	0.63	0.7	0.77	S
Lock−Stop release time1 from 1st to 4th off time	T_{LRoff1}		3.1	3.5	3.9	S
Lock−Restart on time	T_{LRon}		0.63	0.7	0.77	S
Lock−Restart time ratio1	R_{LR1}	T_{LRoff1} / T_{LRon}		5		−
Lock−Stop release time2 (Note 9) as from 5th off time	T_{LRoff2}		12.5	14	15.5	S
Lock−Restart time ratio2 (Note 9) as from 5th off time	R_{LR2}	T_{LRoff2} / T_{LRon}		20		−
Thermal shutdown protection detection temperature	T_{TSD}	(Design Target)	150	180		°C
Thermal shutdown protection detection hysteresis	ΔT_{TSD}	(Design Target)		40		°C
Over current detection current	I_{OVC}			2.5		A
Current limiter	I_{CL}		1.8	2.0	2.2	A
REG pin output voltage load regulation	ΔVregld	IREG = −10 mA			50	mV
Hall input bias current	Ihin	IN1, IN2 = 0 V		0	1	μA
Hall input sensitivity	ΔVhin		40			mV
PWM input bias current	Ipwmin	VDD = 5.5 V, PWM = 0 V	14	28	42	μA
UVLO detection voltage	Vuvdet	VCC voltage	3.1	3.4	3.6	V
UVLO release voltage	Vuvrls	VCC voltage	3.3	3.6	3.9	V
UVLO hysteresis voltage	ΔVuv		0.1	0.2	0.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. When a motor rotates with below 50 rpm (phase change period over 0.3 s), lock protection will works.
8. When a motor can't rotate for 0.7 s after start−up, lock protection will work.
9. When the locked rotor state continues for long time, lock stop period changes as from 5th off time.

BLOCK DIAGRAM

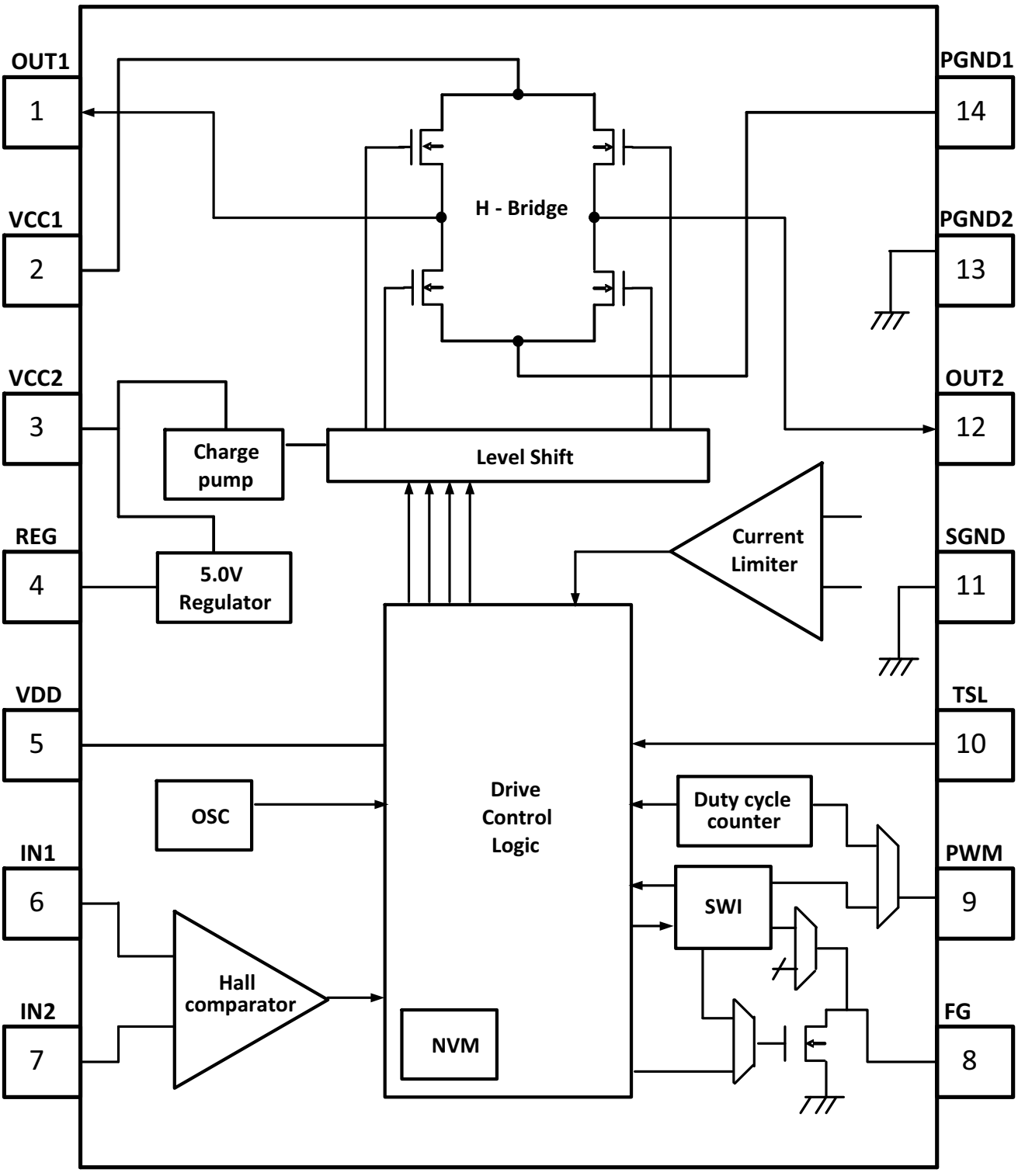
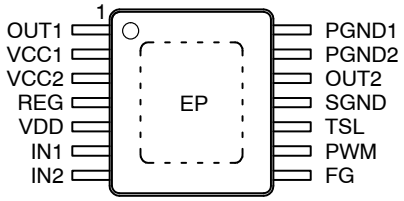


Figure 3. Block Diagram

PIN ASSIGNMENT



(Top View)

Table 6. PIN DESCRIPTION

Pin No.	Pin Name	Description	Equivalent Circuit
1	OUT1	Motor drive output pin. This pin is connected from drain of the built−in power MOSFET.	Figure 4
2	VCC1	Power supply pin for built−in power MOSFET.	Figure 5
3	VCC2	Power supply for internal circuit, ex. pre−driver, charge−pump.	
4	REG	5.0 V regulator output pin. This voltage acts a power source for oscillator, protection circuits, various adjustment circuits and so on. The maximum load current of REG is 20 mA. Don't exceed it.	Figure 6
5	VDD	Power supply pin for logic circuit. This pin should be connected to REG pin normally in use.	Figure 7
6	IN1	Hall sensor signal input pin. The differential outputs of the Hall element are connected to IN1 and IN2 each.	Figure 8
7	IN2		Figure 9
8	FG	The FG (frequency generator) frequency output controls a motor's electrical rotational speed (FG output synchronizes with the Hall sensor signal). This pin can be RD (rotation detection) function by bit setting of Reg. 0x010C "TACHSEL". The FG pin is an open drain output. Recommended pull up resistor should be 1 kW to 100 kW. Leave the pin open when not in use. Parameter setting through the communication, is performed by the pin use.	Figure 10
9	PWM	Rotational control signal input pin. The type of input signal is the rectangular waveform. The rotational speed is controlled by duty−cycle of the pulse and is proportional to the duty−cycle ratio. Parameter setting through the communication is performed by this pin.	Figure 11
10	TSL	Communication input selection and internal test mode pin. When short to GND, FG pin is serial in/out. When short to REG, PWM pin is serial in and FG pin is for serial out.	Figure 12
11	SGND	Internal circuit GND pin.	Figure 5
12	OUT2	Motor drive output pin. This pin is connected to the drain of the built−in power MOSFET.	Figure 4
13,14	PGND1 PGND2	Power GND pin. This pin has to tolerate surge current.	Figure 5

EQUIVALENT CIRCUIT

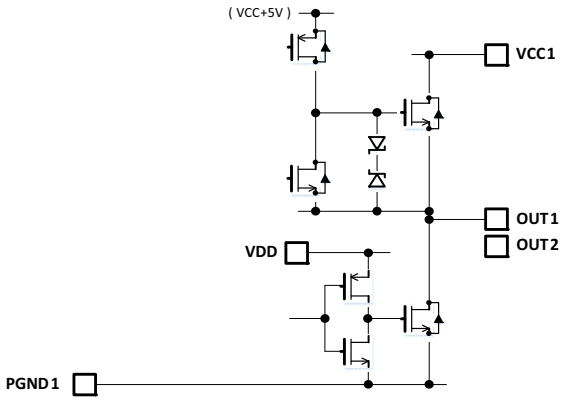


Figure 4. OUT1 and OUT2 Equivalent Circuit

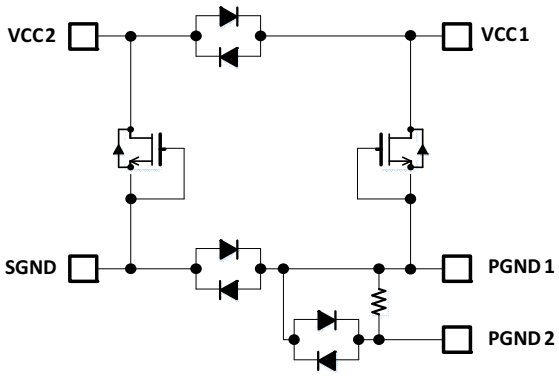


Figure 5. VCC1,2/PGND1,2/SGND Equivalent Circuit

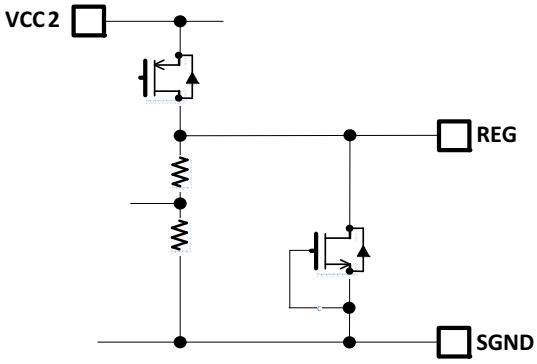


Figure 6. REG Equivalent Circuit

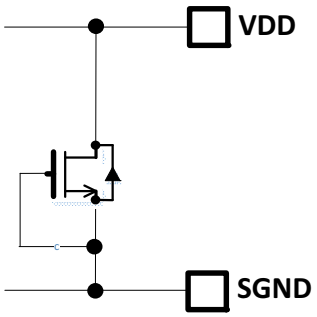


Figure 7. VDD Equivalent Circuit

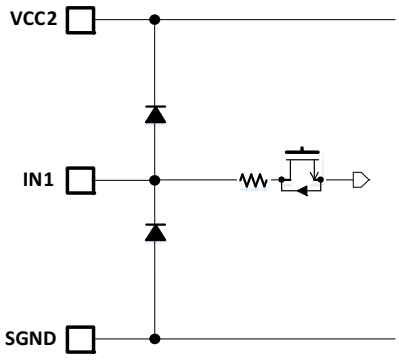


Figure 8. IN1 Equivalent Circuit

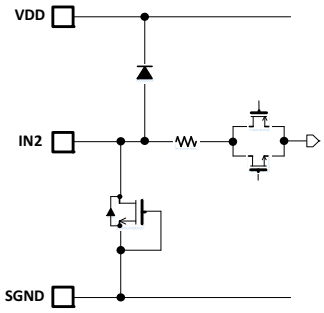


Figure 9. IN2 Equivalent Circuit

EQUIVALENT CIRCUIT (continued)

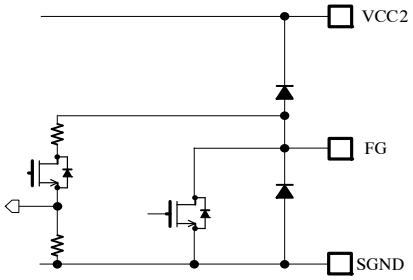


Figure 10. FG Equivalent Circuit

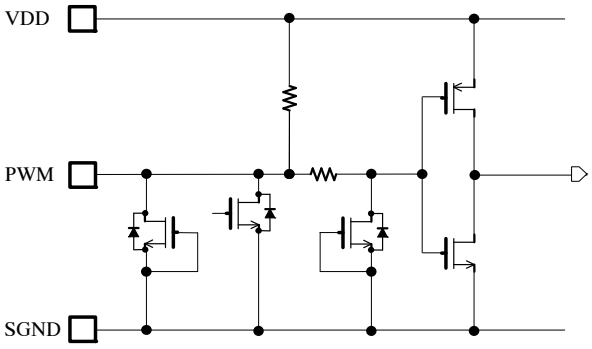


Figure 11. PWM Equivalent Circuit

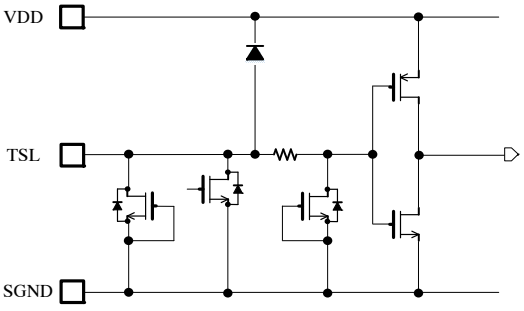


Figure 12. TSL Equivalent Circuit

OPERATION DESCRIPTION

The LV8316HA has various functions to be controlled by built−in registers to optimize. Refer the Register map and description page for the detail.

Start−up Condition

When VCC is input, the LV8316HA is active. To input the speed control signal to PWM pin, the state of the driver moves to drive mode and starts motor rotation. The IC outputs commutation timing is decided by Hall signal. When a motor rotation starts, soft start function gradually increases output duty−cycle to reduce the unnecessary rush current. After the soft start function, the IC goes to steady rotation mode in which can control a constant speed by input signal of PWM pin.

Soft Start

When the speed control signal is input to PWM pin, the IC drives a motor while performing the soft start mode. In this mode, the output duty−cycle gradually increase with a predetermined slope which is started from 4% of output duty−cycle.

The driver monitors output duty−cycle and rotational speed as the soft start release conditions which are adjustable by register setting. The soft start mode is completed when output duty−cycle or rotational speed achieves to release condition or takes a certain period (Figure 13). Also, this mode is continued until 8 FG pulses come.

If the release condition, output duty−cycle or rotational speed specified by the speed control signal is achieved in the soft start mode, the soft start mode is finished and the IC moves to the steady rotation mode. If the rotational speed does not achieve the target speed specified by speed control signal after the soft start completion, IC increases the output duty according to the slope of steady rotational mode. The output frequency at the soft start mode is 48 kHz.

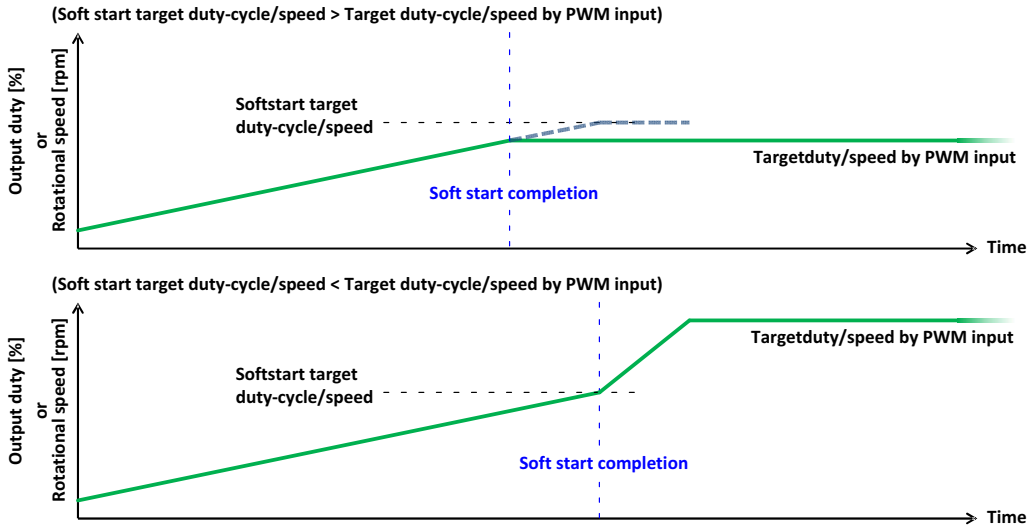


Figure 13. Soft Start Sequence Image

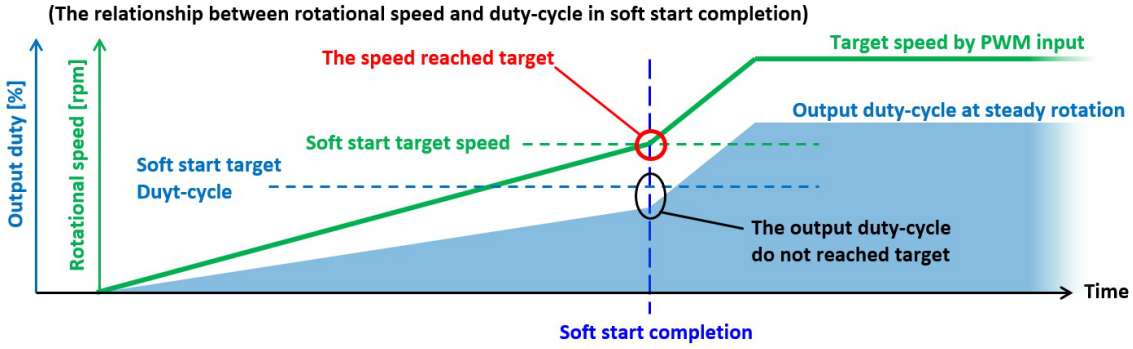


Figure 14. Simplified Image of Soft Start Completion Condition

(example: Ideal case of rotational speed reached)

The release condition and release time of the soft start mode are set individually by following registers:
“RELLEV” (Address 0x0108 D [4])
“ENDPWM” (Address 0x0108 D [3])
“INCTIM” (Address 0x0108 D [2:0])
“RELLEV” and “ENDPWM” set the release conditions showed in Table 7.

Table 7. SOFT START RELEASE CONDITION SETTING

RELLEV	ENDPWM	Release Condition
0	0	97% of target rpm or 80% duty
1	0	500 rpm ot 80% duty
0	1	97% of target rpm or 24% duty
1	1	500 rpm or 24% duty

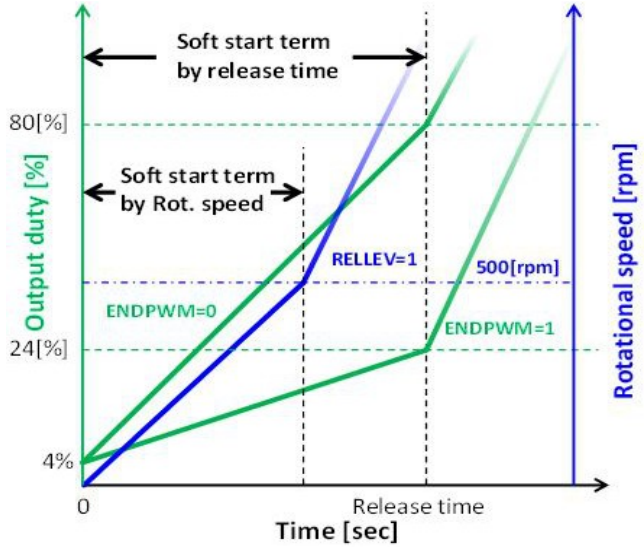


Figure 15. Soft Start Setting Image

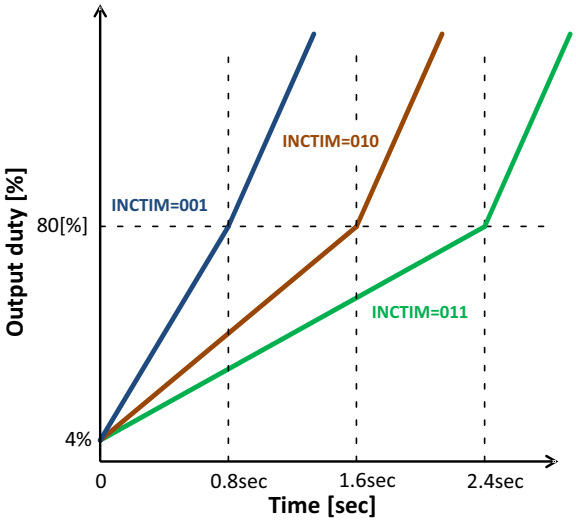


Figure 16. Example: Soft Start Release Time Image

As the green curve in Figure 15 shows, the output duty−cycle in the soft start mode starts from 4% of the output duty. Then the output duty is increased to the release condition linearly. After the soft start satisfies the release condition, the LV8316HA goes to the steady rotation mode. The blue curve in Figure 15 shows that the LV8316HA also monitors the rotational speed whose thresholds 500 rpm or 97% of the target rotational speed.

"INCTIM" decides the period of the soft start as shown in Table 8. The time is changed by the "ENDPWM" setting. Figure 16 shows the relationship between release time and output duty in case of "ENDPWM = 0".

Table 8. SOFT START RELEASE TIME SETTING

INCTIM			Release Time (s)	
[2]	[1]	[0]	ENDPWM = 0 (Release condition duty = 80%)	ENDPWM = 1 (Release condition duty = 24%
0	0	0	0.15	0.002
0	0	1	0.76	0.48
0	1	0	1.51	0.96
0	1	1	2.28	1.50
1	0	0	3.04	2.00
1	0	1	4.56	3.00
1	1	0	7.60	5.00
1	1	1	15.2	10.0

Steady Rotation and Speed Control

The driver mode moves to the steady rotation mode after soft start completion. In this mode, the rotational speed is controlled by the speed control signal of PWM pin. The rotational speed is changed with a predetermined slope by changing PWM speed control signal.

When motor is stopped completely, the motor restarts from soft start mode and goes to target rotational speed in steady rotational mode.

The input frequency range of the speed control signal is 25 Hz−100 kHz. The rotational speed is controlled by duty−cycle of the signal. The output frequency is fixed to 48 kHz and it is not related to the speed control signal frequency. The relationship between the duty−cycle of the speed control signal and the rotational speed are shown in Figure 17.

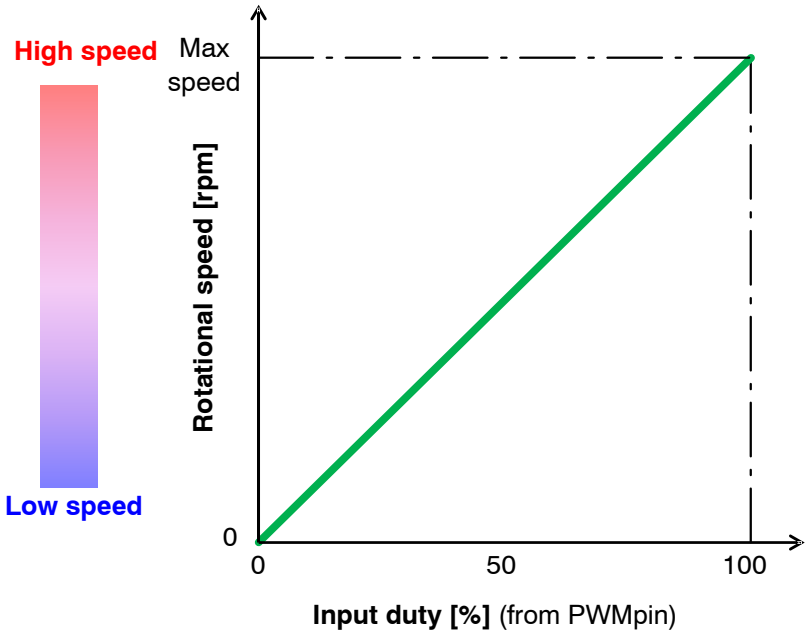


Figure 17. Speed Control Image

As for the speed control, maximum and minimum speed can be adjusted individually as Figure 18.

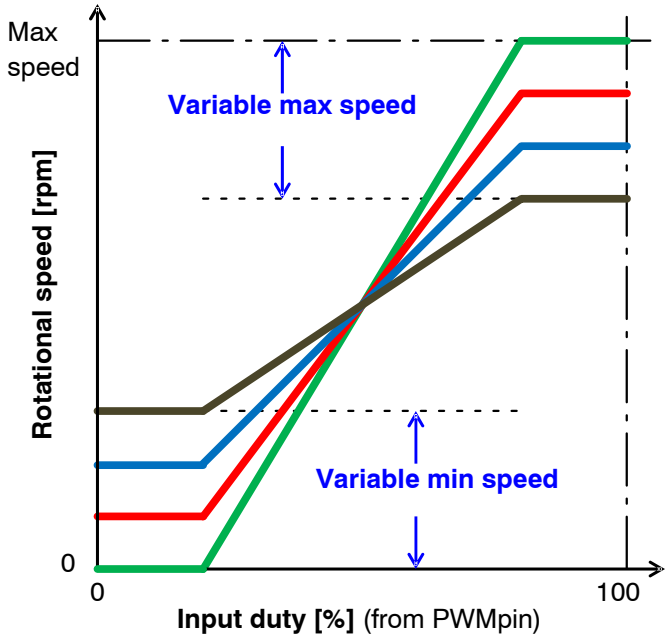


Figure 18. Max/Min Speed Setting Image

The min speed is set by “TAG_L” (Address 0x0100 D [7:0]) and the max speed is set by “TAG_H” (Address 0x0101 D [7:0]). Table 9 and Table 10 show the value of them. Note that don’t set max speed less than min speed.

Table 9. MINIMUM ROTATIONAL SPEED SETTING TABLE FOR TAG_L

Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM
0x00	0	0x20	610	0x40	930	0x60	1380	0x80	2020	0xA0	3050	0xC0	4650	0xE0	7300
0x01	300	0x21	620	0x41	940	0x61	1400	0x81	2040	0xA1	3100	0xC1	4700	0xE1	7400
0x02	310	0x22	630	0x42	950	0x62	1420	0x82	2060	0xA2	3150	0xC2	4750	0xE2	7500
0x03	320	0x23	640	0x43	960	0x63	1440	0x83	2080	0xA3	3200	0xC3	4800	0xE3	7600
0x04	330	0x24	650	0x44	970	0x64	1460	0x84	2100	0xA4	3250	0xC4	4850	0xE4	7700
0x05	340	0x25	660	0x45	980	0x65	1480	0x85	2120	0xA5	3300	0xC5	4900	0xE5	7800
0x06	350	0x26	670	0x46	990	0x66	1500	0x86	2140	0xA6	3350	0xC6	4950	0xE6	7900
0x07	360	0x27	680	0x47	1000	0x67	1520	0x87	2160	0xA7	3400	0xC7	5000	0xE7	8000
0x08	370	0x28	690	0x48	1010	0x68	1540	0x88	2180	0xA8	3450	0xC8	5050	0xE8	8100
0x09	380	0x29	700	0x49	1020	0x69	1560	0x89	2200	0xA9	3500	0xC9	5100	0xE9	8200
0x0A	390	0x2A	710	0x4A	1030	0x6A	1580	0x8A	2220	0xAA	3550	0xCA	5150	0xEA	8300
0x0B	400	0x2B	720	0x4B	1040	0x6B	1600	0x8B	2240	0xAB	3600	0xCB	5200	0xEB	8400
0x0C	410	0x2C	730	0x4C	1050	0x6C	1620	0x8C	2260	0xAC	3650	0xCC	5300	0xEC	8500
0x0D	420	0x2D	740	0x4D	1060	0x6D	1640	0x8D	2280	0xAD	3700	0xCD	5400	0xED	8600
0x0E	430	0x2E	750	0x4E	1070	0x6E	1660	0x8E	2300	0xAE	3750	0xCE	5500	0xEE	8700
0x0F	440	0x2F	760	0x4F	1080	0x6F	1680	0x8F	2320	0xAF	3800	0xCF	5600	0xEF	8800
0x10	450	0x30	770	0x50	1090	0x70	1700	0x90	2340	0xB0	3850	0xD0	5700	0xF0	8900
0x11	460	0x31	780	0x51	1100	0x71	1720	0x91	2360	0xB1	3900	0xD1	5800	0xF1	9000
0x12	470	0x32	790	0x52	1110	0x72	1740	0x92	2380	0xB2	3950	0xD2	5900	0xF2	9100
0x13	480	0x33	800	0x53	1120	0x73	1760	0x93	2400	0xB3	4000	0xD3	6000	0xF3	9200
0x14	490	0x34	810	0x54	1140	0x74	1780	0x94	2450	0xB4	4050	0xD4	6100	0xF4	9300
0x15	500	0x35	820	0x55	1160	0x75	1800	0x95	2500	0xB5	4100	0xD5	6200	0xF5	9400
0x16	510	0x36	830	0x56	1180	0x76	1820	0x96	2550	0xB6	4150	0xD6	6300	0xF6	9500
0x17	520	0x37	840	0x57	1200	0x77	1840	0x97	2600	0xB7	4200	0xD7	6400	0xF7	9600
0x18	530	0x38	850	0x58	1220	0x78	1860	0x98	2650	0xB8	4250	0xD8	6500	0xF8	9700
0x19	540	0x39	860	0x59	1240	0x79	1880	0x99	2700	0xB9	4300	0xD9	6600	0xF9	9800
0x1A	550	0x3A	870	0x5A	1260	0x7A	1900	0x9A	2750	0xBA	4350	0xDA	6700	0xFA	9900
0x1B	560	0x3B	880	0x5B	1280	0x7B	1920	0x9B	2800	0xBB	4400	0xDB	6800	0xFB	10000
0x1C	570	0x3C	890	0x5C	1300	0x7C	1940	0x9C	2850	0xBC	4450	0xDC	6900	0xFC	10100
0x1D	580	0x3D	900	0x5D	1320	0x7D	1960	0x9D	2900	0xBD	4500	0xDD	7000	0xFD	10200
0x1E	590	0x3E	910	0x5E	1340	0x7E	1980	0x9E	2950	0xBE	4550	0xDE	7100	0xFE	10300
0x1F	600	0x3F	920	0x5F	1360	0x7F	2000	0x9F	3000	0xBF	4600	0xDF	7200	0xFF	10400

Table 10. MAXIMUM ROTATIONAL SPEED SETTING TABLE FOR TAG_H

Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM	Register	RPM
0x00	300	0x20	940	0x40	2040	0x60	4700	0x80	10600	0xA0	17000	0xC0	23400	0xE0	29800
0x01	320	0x21	960	0x41	2080	0x61	4800	0x81	10800	0xA1	17200	0xC1	23600	0xE1	30000
0x02	340	0x22	980	0x42	2120	0x62	4900	0x82	11000	0xA2	17400	0xC2	23800	0xE2	30200
0x03	360	0x23	1000	0x43	2160	0x63	5000	0x83	11200	0xA3	17600	0xC3	24000	0xE3	30400
0x04	380	0x24	1020	0x44	2200	0x64	5100	0x84	11400	0xA4	17800	0xC4	24200	0xE4	30600
0x05	400	0x25	1040	0x45	2240	0x65	5200	0x85	11600	0xA5	18000	0xC5	24400	0xE5	30800
0x06	420	0x26	1060	0x46	2280	0x66	5400	0x86	11800	0xA6	18200	0xC6	24600	0xE6	31000
0x07	440	0x27	1080	0x47	2320	0x67	5600	0x87	12000	0xA7	18400	0xC7	24800	0xE7	31200
0x08	460	0x28	1100	0x48	2360	0x68	5800	0x88	12200	0xA8	18600	0xC8	25000	0xE8	31400
0x09	480	0x29	1120	0x49	2400	0x69	6000	0x89	12400	0xA9	18800	0xC9	25200	0xE9	31600
0x0A	500	0x2A	1160	0x4A	2500	0x6A	6200	0x8A	12600	0xAA	19000	0xCA	25400	0xEA	31800
0x0B	520	0x2B	1200	0x4B	2600	0x6B	6400	0x8B	12800	0xAB	19200	0xCB	25600	0xEB	32000
0x0C	540	0x2C	1240	0x4C	2700	0x6C	6600	0x8C	13000	0xAC	19400	0xCC	25800	0xEC	32200
0x0D	560	0x2D	1280	0x4D	2800	0x6D	6800	0x8D	13200	0xAD	19600	0xCD	26000	0xED	32400
0x0E	580	0x2E	1320	0x4E	2900	0x6E	7000	0x8E	13400	0xAE	19800	0xCE	26200	0xEE	32600
0x0F	600	0x2F	1360	0x4F	3000	0x6F	7200	0x8F	13600	0xAF	20000	0xCF	26400	0xEF	32800
0x10	620	0x30	1400	0x50	3100	0x70	7400	0x90	13800	0xB0	20200	0xD0	26600	0xF0	33000
0x11	640	0x31	1440	0x51	3200	0x71	7600	0x91	14000	0xB1	20400	0xD1	26800	0xF1	33200
0x12	660	0x32	1480	0x52	3300	0x72	7800	0x92	14200	0xB2	20600	0xD2	27000	0xF2	33400
0x13	680	0x33	1520	0x53	3400	0x73	8000	0x93	14400	0xB3	20800	0xD3	27200	0xF3	33600
0x14	700	0x34	1560	0x54	3500	0x74	8200	0x94	14600	0xB4	21000	0xD4	27400	0xF4	33800
0x15	720	0x35	1600	0x55	3600	0x75	8400	0x95	14800	0xB5	21200	0xD5	27600	0xF5	34000
0x16	740	0x36	1640	0x56	3700	0x76	8600	0x96	15000	0xB6	21400	0xD6	27800	0xF6	34200
0x17	760	0x37	1680	0x57	3800	0x77	8800	0x97	15200	0xB7	21600	0xD7	28000	0xF7	34400
0x18	780	0x38	1720	0x58	3900	0x78	9000	0x98	15400	0xB8	21800	0xD8	28200	0xF8	34600
0x19	800	0x39	1760	0x59	4000	0x79	9200	0x99	15600	0xB9	22000	0xD9	28400	0xF9	34800
0x1A	820	0x3A	1800	0x5A	4100	0x7A	9400	0x9A	15800	0xBA	22200	0xDA	28600	0xFA	35000
0x1B	840	0x3B	1840	0x5B	4200	0x7B	9600	0x9B	16000	0xBB	22400	0xDB	28800	0xFB	35200
0x1C	860	0x3C	1880	0x5C	4300	0x7C	9800	0x9C	16200	0xBC	22600	0xDC	29000	0xFC	35400
0x1D	880	0x3D	1920	0x5D	4400	0x7D	10000	0x9D	16400	0xBD	22800	0xDD	29200	0xFD	35600
0x1E	900	0x3E	1960	0x5E	4500	0x7E	10200	0x9E	16600	0xBE	23000	0xDE	29400	0xFE	35800
0x1F	920	0x3F	2000	0x5F	4600	0x7F	10400	0x9F	16800	0xBF	23200	0xDF	29600	0xFF	36000

If the maximum speed of the motor is more than 1.25 times the maximum target speed set by TAG_H, the soft switching before the commutation change works as synchronous drive in the full−speed (output full−duty) mode. This operation contributes to drive the motor in higher speed because the drive current sustains by it.

The range of PWM input duty−cycle can be set by the registers “DUTY_L” (Address 0x0102 D [7:0]) and “DUTY_H” (Address 0x0103 D [7:0]) whose ranges are 0 to 100% and the resolutions are 100 / 256. Note that do not set “DUTY_H” less than “DUTY_L”

Figure 19. Input duty−cycle setting image shows the relationship between input (PWM) duty cycle and output (Motor) speed. The speed registers define the start and end points of the speed curve and the values in between are interpolated linearly.

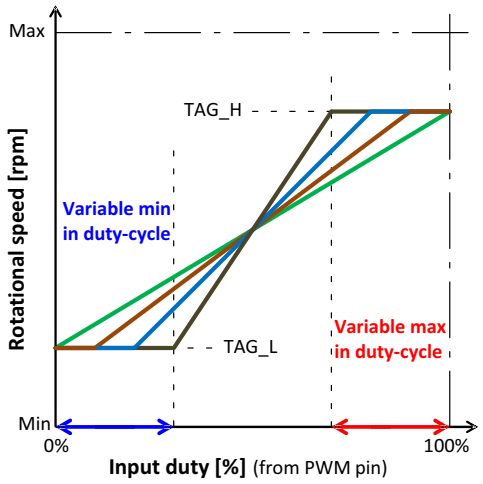


Figure 19. Input Duty−cycle Setting Image

Besides, the speed at the max/min duty cycle can be selectable as Figure 20.

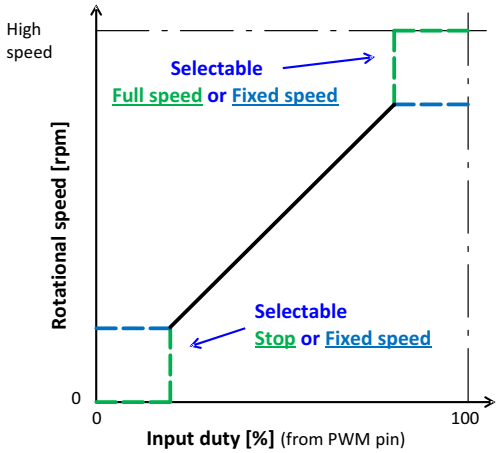


Figure 20. Max/Min Speed Setting Image

About the behavior at minimum duty input, “DUTY_S” (Address 0x0109 D [3:0]) provides several options. The “DUTY_S” sets the threshold duty the motor speed goes to 0 rpm. It is calculated by following Equation 1, except for the case of “DUTY_S” = 15.

The min. input duty = 500 × DUTY_S ⁄ 255 (eq. 1).

If “DUTY_S”=15, the threshold duty equals to the value of “DUTY_L”. Table 11 shows the summary of “DUTY_S”.

Table 11. THE SETTING OF DUTY_S

DUTY_S	Motor Stop Duty Setting (%)
0	0
1	1.9
2	3.9
3	5.8
4	7.8
5	9.8
6	11.7
7	13.7
8	15.6
9	17.6

Table 11. THE SETTING OF DUTY_S

10	19.6
11	21.5
12	23.5
13	25.4
14	27.4
15	The value of DUTY_L

Figure 21 shows the speed curves with “DUTY_S”. The motor speed keeps the speed of “TAG_L” from the duty of “DUTY_L” to the duty of “DUTY_S”, and it is 0 rpm under the duty of “DUTY_S”. Hence, in case of “DUTY_S” = 0, the motor speed keeps the speed of “TAG_L” at input duty 0% and the motor doesn’t stop.

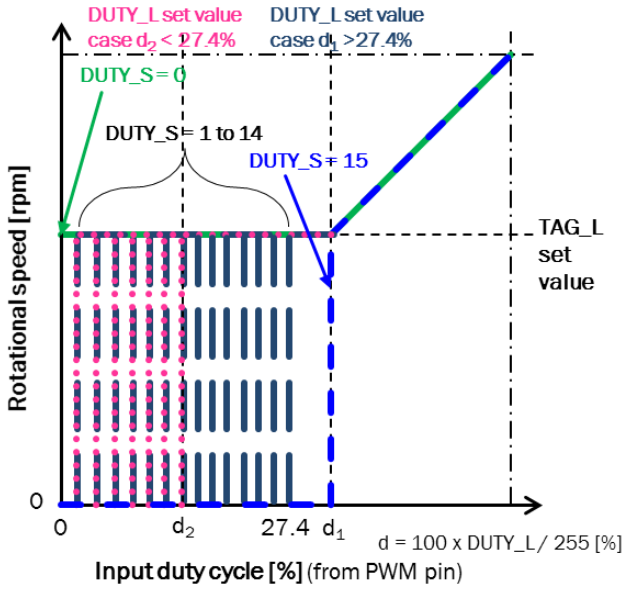


Figure 21. Min Speed Function Setting Image

To restart the motor rotation, the input duty should be set higher than “DUTY_S” + 1.6%.

If the input duty of “DUTY_L” is smaller than 5 times of “DUTY_S”, the threshold equals to “DUTY_L”.

On the other hand, about the behavior at maximum duty input, “FULL” (Address 0x0109 D [2]) provides 2 options. One is to keep the speed specified by “TAG_H” and another is to go to 100% full speed as shown in Figure 22.

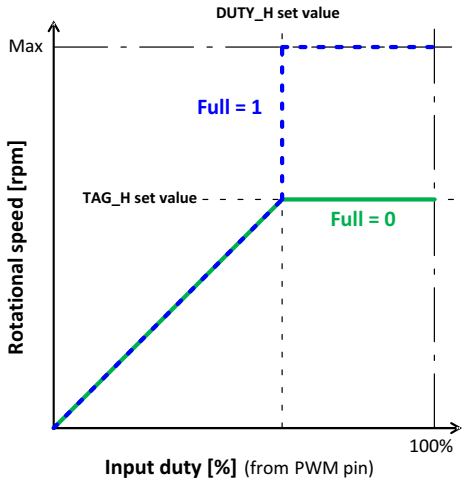


Figure 22. Max Speed Function Setting Image

Output Waveform

The output pulse signal is 0 – VCC and it is changed by modulated special PWM waveform before and after commutation change to suppress the influence of the kickback current at the commutation change. This state is shown in Figure 23 as a schematic view. Hence, input voltage waveform to motor becomes trapezoid signal so that the influence of the kickback current is reduced by suppressing the steep voltage change at the commutation change. This PWM signal before and after commutation change is called a soft switch whose period is adjustable by register setting according with a motor property.

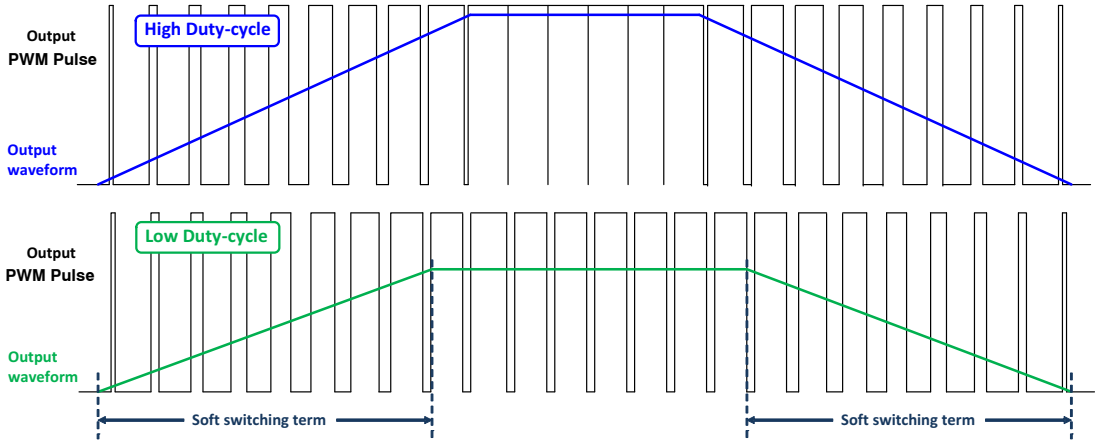


Figure 23. Output Waveform Image

Soft Switch Setting

The LV8316HA can adjust soft switch width. It is expressed by the ratio of one commutation output width, the one commutation width of “L” (Length) and the soft switch time of “S” (Soft switch) can express it as follows.

$$\text{Soft switch width [\%]} = \frac{S}{L} \times 100$$

Figure 24 shows the soft switch image.

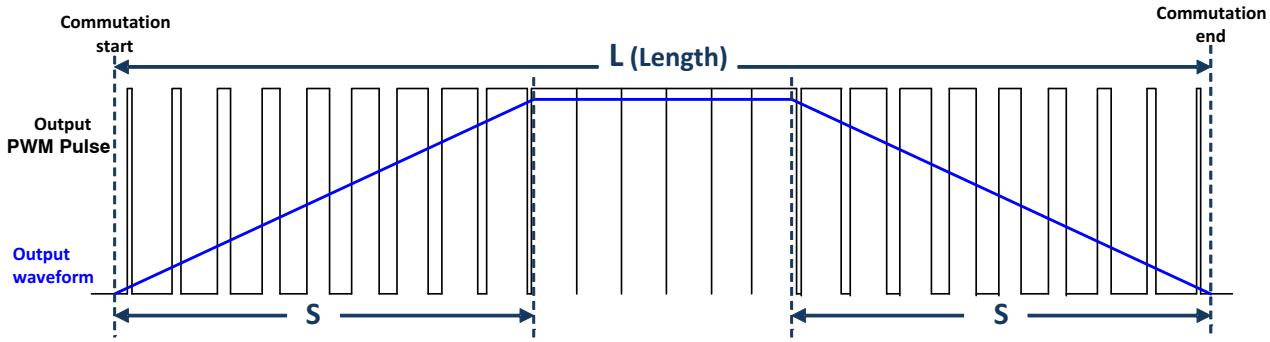


Figure 24. L(Length) and S(Soft switch) Image

SSWHIGH (Address 0x0106 D [7:4]) and SSWLOW (Address 0x0106 D [3:0]) can set the width at max rotational speed (TAG_H) and at min rotational speed (TAG_L) individually. Each register has 4bits and Table 12 shows the adjustable value.

Table 12. SOFT SWITCH WIDTH ADJUSTMENT

Register	S/L Ratio	Register	S/L Ratio
0000	2.9%	1000	26.4%
0001	5.9%	1001	29.3%
0010	8.8%	1010	32.2%
0011	11.7%	1011	35.2%
0100	14.6%	1100	38.1%
0101	17.6%	1101	41.0%
0110	20.5%	1110	43.9%
0111	23.4%	1111	46.9%

Once “SSWHIGH” and “SSWLOW” is set, the soft switch width in other speed settings is interpolated linearly. These relationships are shown in Figure 25.

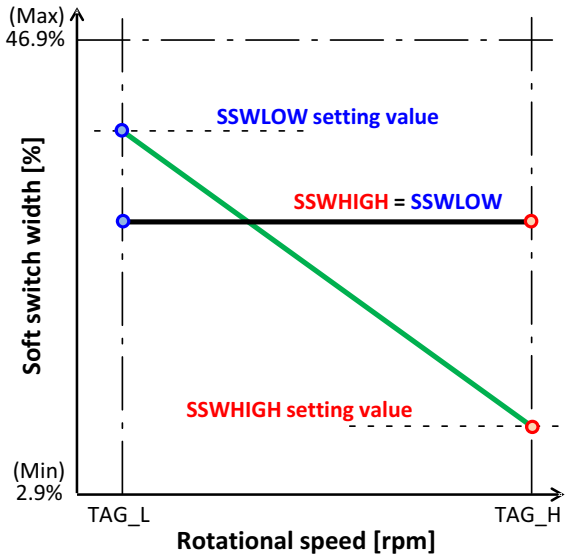


Figure 25. The relationship between soft sw and speed

FG Output

FG signal output is decided by the Hall signal cross point. The relationship between motor speed and FG frequency represents the following equation.

$$f_{FG}[Hz] = N \times 60 \times \frac{p}{2}$$

Where N: Motor speed [rpm]
p: Number of Pole

Figure 26 shows the timing chart of the hall sensor output and the FG output.

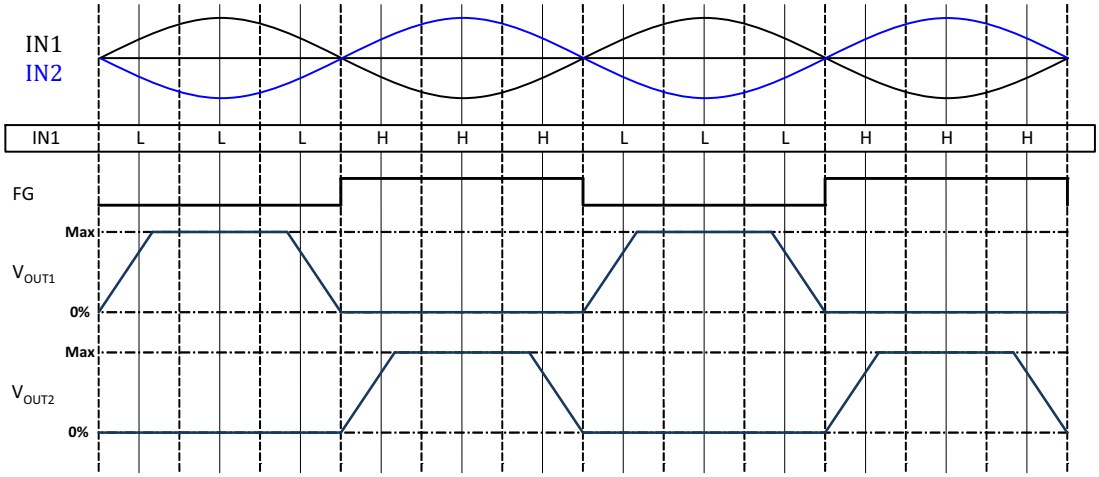


Figure 26. Timing Chart of Output

Lead Angle Setting

In the output, the delay is generated between output voltage and output current because of an influence of the motor coils. This delay generates the torque which doesn't contribute to the motor rotation and deteriorates the rotational efficiency. It is generally increased in proportion to the rotational speed.

Due to the earlier commutation than the Hall sensor signals, the LV8316HA can cancel the delay of the output current. This phase advance is named the "Lead−angle". An example is shown in Figure 27.

In Figure 27, when commutation is driven by Hall sensor, the output voltage V_{OUT1} of trapezoidal wave and the output current I_{OUT1} of sinusoidal wave are expressed in black each. On the other hand, red lines are with adjusted lead−angle and it is the most optimum commutation timing.

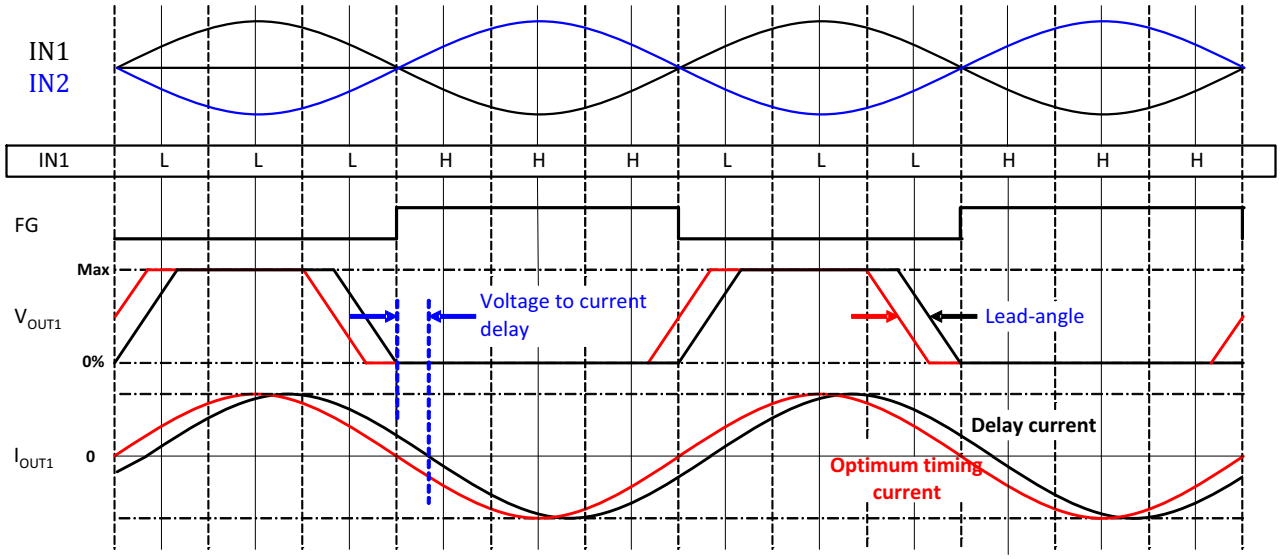


Figure 27. The Relationship between the Lead−angle and the Delay of Output Current

The relationship between rotational speed and lead−angle is shown in Figure 28. The optimum lead−angle will change according to a motor so that it is necessary for a real motor to optimize lead−angle. To support various lead−angle curves, the max speed of lead−angle and the min speed of lead angle can be set individually by registers.

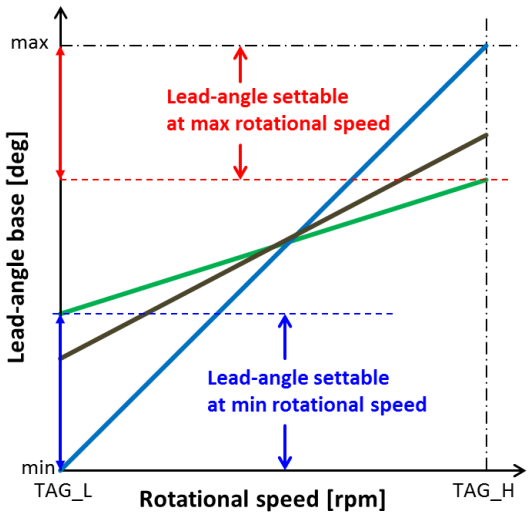


Figure 28. Lead−angle Curve Image

PROTECTIONS

The LV8316HA has the following protection functions

- TSD (Thermal Shut Down)
- UVLO (Under Voltage Lock Out)
- Lock protection
- CLM (Current Limiter)
- OCP (Over Current Protection)

When the TSD or Lock protection works, all of the internal FETs are turned off. On the other hand, when UVLO or CLM works, the output PWM is off and become re−circulation state which is the mode to consume the coil power by lower Transistors grounding.

Each function is explained below and refer to application note AND9737 to see the detail.

Thermal Shutdown Protection (TSD)

When IC's junction temperature rises to 180°C, TSD will work and turns off high−side and low−side MOSFET. Therefore, OUT1 and OUT2 pins become high impedance and coil current is shut off. Afterwards, it falls under 140°C, TSD will be cleared and motor starts to rotate.

Under Voltage Lock Out (UVLO)

When VCC voltage goes to low level (3.4 V), UVLO will work and it stops the motor. It is cleared when VCC voltage recovers over 3.6 V.

Lock Detection and Lock Protection

If motor is locked, heat is continuous generated because IC keeps to turn on electricity of a motor.

On the other hand, when the lock protection works, heat is not generated because IC turns off an electricity of the motor.

In case of motor lock in the motor rotation state, if the FG edge is not detected more than 0.3 s (50rpm condition), IC judges the status as a "motor lock" and protection function will work (Figure 29).

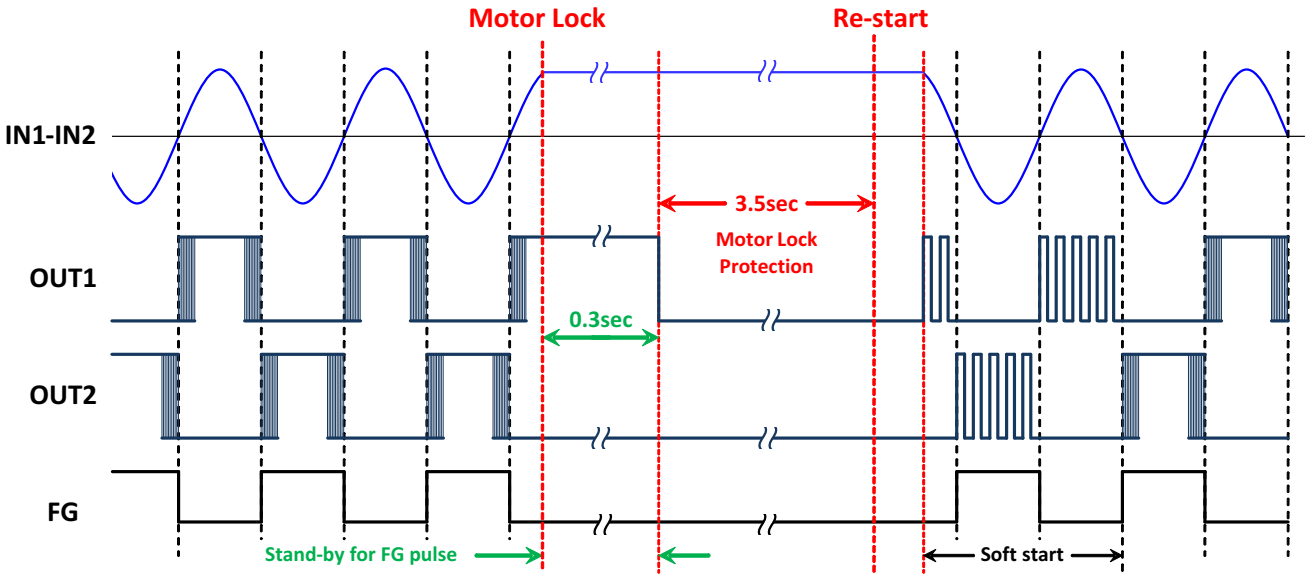


Figure 29. Timing Chart of the Lock Protection

It takes 3.5s for Lock protection period (1st to 4th protection time) equals to the total of lock detect time and the alignment time. The protection vs stand by period is approx. 1:5 (from 1st to 4th protection time).

After 5th protection time, the lock protection period becomes 14s and the protection vs stand by period is approx. 1:20 (after 5th protection time).

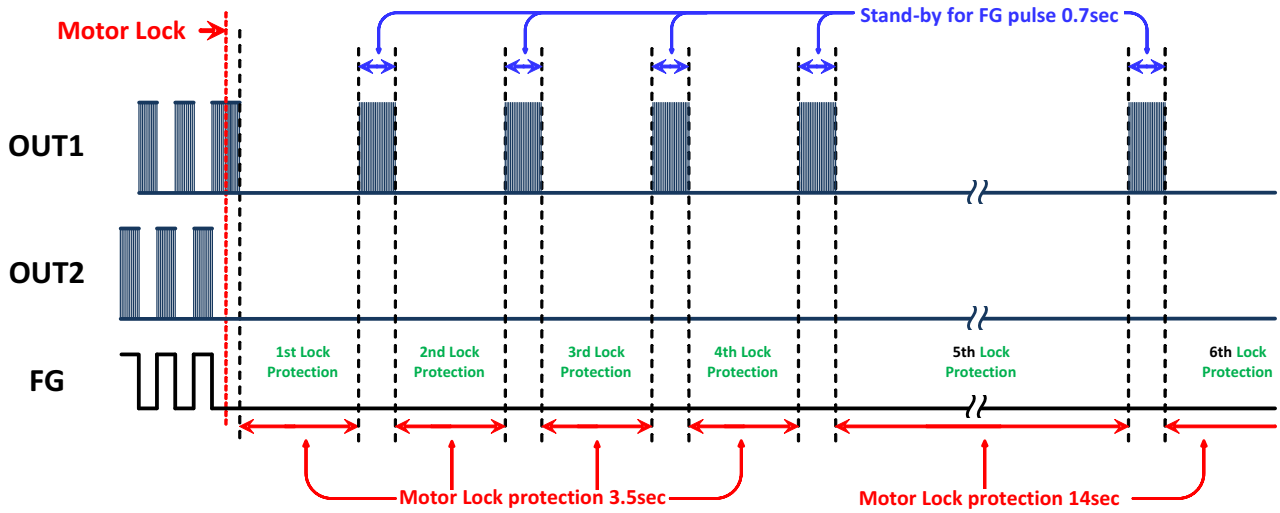


Figure 30. The Relationship between Protection Time and Number of Times Protection

Current Limiter (CLM)

When the coil current becomes large, CLM will work and shuts down the coil current. The threshold current is 2.0 A.

Overcurrent Protection (OCP)

If the coil current becomes larger than 2.5 A even if CL is working, OCP will work and motor rotation is stopped.

NONVOLATILE MEMORY

The IC has internal nonvolatile memory which can store various setting. No resistance for setting is needed like the conventional models. In addition, PCB design becomes simpler.

List below is main configurable items.

- Max/Min rotational speed.
- Max/Min input duty−cycle.
- Lead−angle
- Soft start
- Speed control slope

Program/Erase operation to the memory is performed through a built−in register. Please notice that the number of program/erase times that can be allowed is limited to 10 times.

SERIAL INTERFACE

The LV8316HA allows communication via USART (Universal Synchronous Asynchronous Receiver Transmitter). Various parameter registers can be accessed through USART communication. In addition, register values can be saved to internal nonvolatile memory so that they are available after startup without any communication as Figure 31 shows.

In this document, the CPU or MPU which controls the communication is called “master”, and the LV8316HA is called “slave”. Basically, USART is one to one communication and doesn’t support parallel access to the multiple devices. Please turn on the only one target device and turn off the other devices in that case.

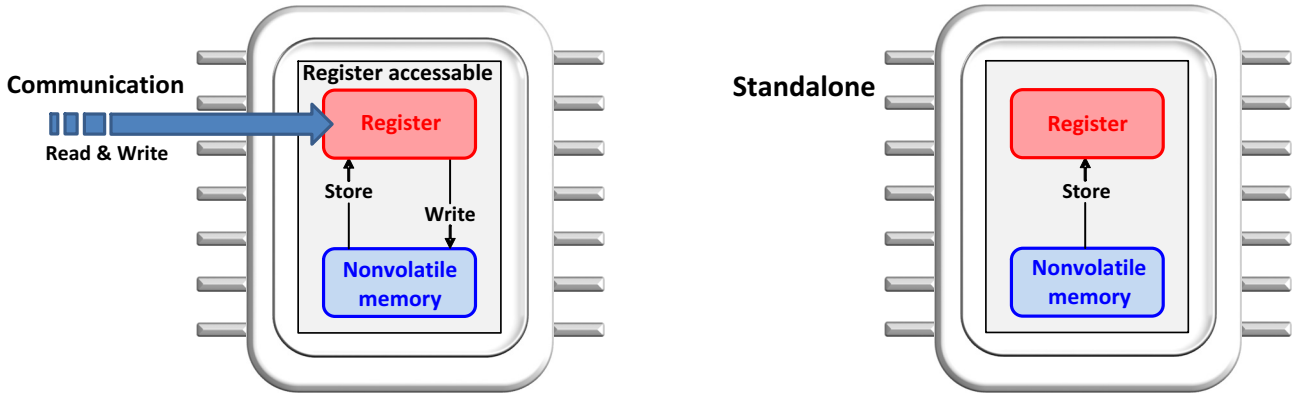


Figure 31. Image of Internal Register and Nonvolatile Memory

Connection

The IC provides 2 USART modes, a single wire mode and a dual wire mode. In single wire mode, the FG pin is used for both in− and output. In dual wire mode, the FG pin is used as output and the PWM pin is used as input. The state of the TSL pin defines the USART mode as shown in Table 13.

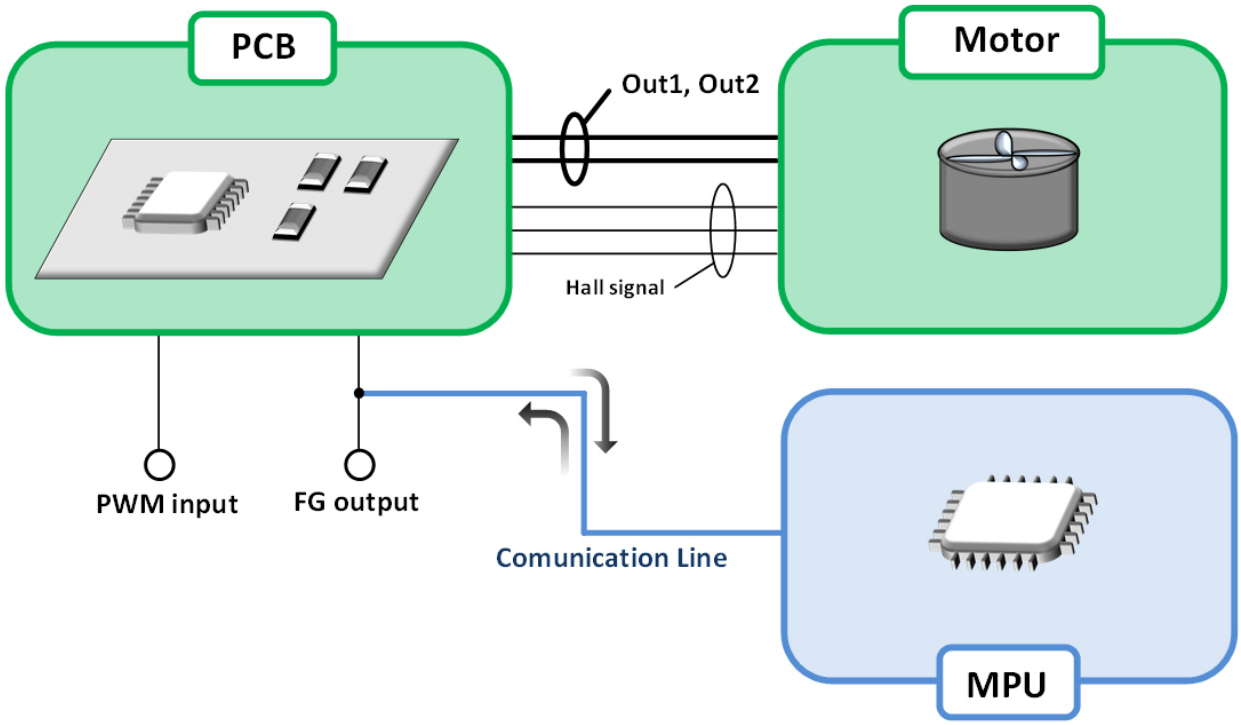


Figure 32. Connection Image in Single wire USART

Table 13. I/O PIN CONDITION IN USART MODE

	Single Wire Mode	Dual Wire Mode
TSL pin	Pull down (GND)	Pull−up (VDD)
Communication Pin	FG pin (For Read and Write)	PWM pin (For Write) FG pin (For Read)

Normally, the communication line should be High−Impedance, however it should be pulled “Low” as needed during communication or data transfer. Therefore the communication pin of the bus master (MCU) must be an open−drain output. Please refer the Application note AND9761 for the detail.

Communication Protocol

About the detail of protocol, please see the Application note AND9761.

REGISTER MAP

Register MAP

Internal register map is shown in below. The register can classify four kinds in below.

- Read only
- Read/Write, A save to nonvolatile memory is possible.
- Read/Write, A save to nonvolatile memory is impossible
- Write only, A save to nonvolatile memory is impossible.

Table 14. REG. MAP 1 (Address 0x0000 – 0x0114)

Address	Key	Initial	Register							
			D7	D6	D5	D4	D3	D2	D1	D0
0x0000	Free	0xAA	1	0	1	0	1	0	1	0
0x0001		0x55	0	1	0	1	0	1	0	1
0x0002		0x00					0	REG_EN	RECALC_EN	RELOAD_EN
0x0003		0x00								RELOAD
0x0004		0x00								RECALC
0x0005		0x78	Identification number							
0x0100	Free	0x00	TAG_L[7:0]							
0x0101		0x00	TAG_H[7:0]							
0x0102		0x00	DUTY_L[7]	DUTY_L[6:0]						
0x0103		0x80	DUTY_H[7]	DUTY_H[6:0]						
0x0104		0x00	DLDEG_L[7:0]							
0x0105		0x00	DLDEG_H[7:0]							
0x0106		0x00	SSWHIGH[3:0]				SSWLOW[3:0]			
0x0107		0x00					0	PWMIN_INV	DRVMODE[1:0]	
0x0108		0x00	DWNSET	FULL	SS_SW_SEL	RELLEV	ENDPWM	INCTIM[2:0]		
0x0109		0x00					DUTY_S[3:0]			
0x010A		0x00							DTIME[1]	DTIME[0]
0x010B		0x00				0	CL_SKIP	CL_ASYNC	OCP_LAT_CLR	STEPSEL
0x010C		0x00							TACHSEL[1]	TACHSEL[0]
0x010D		0x00							PWMAV[1:0]	
0x010E		0x00					0	0	OCP_MASK[1:0]	
0x010F		0x00			0	0	0	0	ON_INTERNAL	0
0x0110		0x00					LOCK_ FAULT	0	0	0
0x0111		0x00	MSKDEG_TP[3:0]				0	0	0	0
0x0112		0x04	RESERVED							
0x0113		0x00	IX[3:0]				0	IG[2:0]		
0x0114		0x00	0	PX[2:0]			0	PG[2:0]		

Table 15. REG. MAP 2 (Address 0x0219)

Address	Key	Initial	Register							
			D7	D6	D5	D4	D3	D2	D1	D0
0x0219	Free	0x00		SWI_ERR[6:0]						

Table 16. REG. MAP 3 (Address 0x0400 – 0x0407)

Address	Key	Initial	Register							
			D7	D6	D5	D4	D3	D2	D1	D0
0x0400	REG_EN=1	0x00	0	DATASEL	YFINC_EN	VPP_REFSEL[1:0]		YFOPMODE[2:0]		
0x0401		0x00								0
0x0402		0x00						VPP_REG_EN	0	EN_FTP
0x0403		0x10	0	0	YF_PE_BUSY	1				OP_FTP
0x0404		0x46	PRG_LNGT							
0x0405		0x1E	ERS_LNGT							
0x0406		0x00	BYTESEL[7:0]							
0x0407		0x00					BYTESEL[11:8]			

The registers in the black cells do not exist. Therefore, these registers cannot be written and the read values are always zero. The registers expressed by numeric value (0 or 1) must be written the same value.

There are some register addresses which contain both the bits stored NVM and not stored NVM. Confirm the bit characteristics to save the data to NVM.

The registers for the driver settings are mainly placed in “Address 0x0100−0x0114 (Table 1)” and the registers for control of the internal nonvolatile memory (NVM) are placed in “Address 0x0400−0x0407 (Table 3)”. To control NVM by the registers placed in “Address 0x0400−0x0407, the setting REG_EN (Address 0x0002, D [2]) = 1 is needed.

The “Key” shows the condition to access to the registers. When “Key” is “Free”, it is possible to access the target registers without any special settings. However, when “Key” is “REG_EN = 1”, REG_EN should be set to 1 at first, then write / read the target registers.

*Because REG_EN returns to 0 when power supply shuts down at once, all communication must be continued without power supply shuts down.

REGISTER DESCRIPTION

Table 17. REGISTER ADDRESS 0x0000−0x0005 Register Description 1

Function	Address	Bits	Register Name	Description
Fixed register 1	0x0000	[7:0]	−	Data of 0xAA are stored. (Read only)
Fixed register 2	0x0001	[7:0]	−	Data of 0x55 are stored. (Read only)
Register enable	0x0002	[2]	REG_EN	This register is key to access Address 0x0400−0x0407.
Enable re−calculation	0x0002	[1]	RECALC_EN	This register enable re−calculation of Speed/Lead Angle/Soft SW setting. 0 : Disable 1 : Enable
Register re−loading (memory to register)	0x0002	[0]	RELOAD_EN	Re−reading is performed of memory data to registers. −A function becomes effective in RELOAD_EN = 1 −Re−reading is carried out in RELOAD = 1. RELOAD=1 is effective in RELOAD_EN=1.
	0x0003	[0]	RELOAD	
Trigger of re−calculation	0x0004	[0]	RECALC	When this bit set 1, re−calculation of Speed/Lead Angle/Soft SW setting is executed and the setting change is implemented.
Device ID	0x0005	[7:0]	ID_NUMBER	Data of device ID are stored. (Read only)

Table 18. REGISTER ADDRESS 0x0100−0x0114 Register Description 2

Function	Address	Bits	Register Name	Description
Minimum speed setting	0x0100	[7:0]	TAG_L	These registers set minimum/maximum rotational speed. 0000 0000: 0/300rpm (Min / Max) 1111 1111: 10400/36000rpm (Min / Max) *The details refers to a clause of “ROTATIONAL SPEED CURVE SETTING”.
Maximum speed setting	0x0101	[7:0]	TAG_H	
Minimum input duty cycle setting	0x0102	[7:0]	DUTY_L	These registers set minimum input duty−cycle. 0000 0000: Duty 0% 1111 1111: Duty 100% (The maximum of the memory setting is 49.8%)
Maximum input duty cycle setting	0x0103	[7:0]	DUTY_H	These registers set maximum input duty−cycle. 0000 0000: Duty 0% 1111 1111: Duty 100% (The minimum of the memory setting is 50.2%)
Lead−angle setting at minimum speed	0x0104	[7:0]	DLDEG_L	These registers adjust lead−angle in rotational speed by TAG_L setting. 000 0000: 0 degree, 111 1111 : −22.225deg (DLDEG_L[7] = 0) 000 0000: 0 degree, 111 1111 : +22.225deg (DLDEG_L[7] = 1)
Lead−angle setting at maximum speed	0x0105	[7:0]	DLDEG_H	These registers adjust lead−angle in rotational speed by TAG_H setting 000 0000: 0 degree, 111 1111 : −22.225deg (DLDEG_H[7] = 0) 000 0000: 0 degree, 111 1111 : +22.225deg (DLDEG_H[7] = 1)
Soft switch width setting at maximum speed	0x0106	[7:4]	SSWHIGH	Soft switch width is set at rotational speed of TAG_H setting. 0000: 2.9% equivalency of one commutation period. 1111: 46.9% equivalency of one commutation period.
Soft switch width setting at minimum speed	0x0106	[3:0]	SSWLOW	Soft switch width is set at rotational speed of TAG_L setting. 0000: 2.9% equivalency of one commutation period. 1111: 46.9% equivalency of one commutation period.
Speed control slope invert	0x0107	[2]	PWMIN_INV	Control slope polarity for input duty−cycle is changed. 0: Normal mode (Low duty−cycle is low speed rotation) 1: Invert mode (Low duty−cycle is high speed rotation)
Sync/Async drive select	0x0107	[1:0]	DRVMODE	These registers select synchronous / asynchronous drive. 00: High−side switching is PWM. Low−side switching is asynchronous 01: High−side switching is PWM. Low−side switching is synchronous 10: High−side switching is asynchronous. Low−side switching is PWM. 11: High−side switching is synchronous. Low−side switching is PWM.

Table 18. REGISTER ADDRESS 0x0100−0x0114 Register Description 2

Function	Address	Bits	Register Name	Description
Sync−drive stop mode (deceleration)	0x0108	[7]	DWNSET	This register selects drive modes when sudden decrease of speed* was detected. *When receives control less than 80% of existing speed. 0: Normal (Synchronization drives are always maintained) 1: It is changed to asynchronous drive in speed decrease
Maximum speed setting 2	0x0108	[6]	FULL	Set when input over than DUTY_H was received. 0: It is fixed by TAG_H setting 1: It is fixed full speed, which is specified by PWM duty−cycle 100% with soft switch.
Soft switch mask time select	0x0108	[5]	SS_SW_SEL	Set soft switch period in soft start mode. 0:Rise 2.5ms, Fall 5 ms 1: Rise 1.25ms, Fall 2.5 ms
Soft start release condition	0x0108	[4]	RELLEV	This register selects rotational speed of soft start release condition. 0: When rotational speed arrives at 97% equivalency target speed. 1: When rotational speed arrives at 500rpm.
Soft start release condition	0x0108	[3]	ENDPWM	This register selects max output duty−cycle of soft start release condition. 0: Max output duty−cycle is 24% 1: Max output duty−cycle is 80%
Soft start release time	0x0108	[2:0]	INCTIM	Time until the release condition of Soft start is decided.
Minimum speed setting 2 (Note 10)	0x0109	[3:0]	DUTY_S[3:0]	These registers set the various speed when input duty−cycle is less than DUTY_L.
Dead Time setting	0x010A	[1:0]	DTIME	Dead time width select in synchronous rectification drive. 00: 125ns 01: 250ns 10: 500ns 11: 0ns
Disable period of motor current in CL	0x010B	[3]	CL_SKIP	This register sets disable period of motor current when CL is active. 0 : only for corresponding PWM pulse 1 : for corresponding and next PWM pulse
Disable motor synchronous rectification in CL	0x010B	[2]	CL_ASYNC	This register disables motor synchronous rectification when CL is active. 0 : Synchronous rectification is not disable when CL is active 1 : Synchronous rectification is disable until detecting Hall signal or motor stop signal when CL is active. After detecting Hall signal or motor stop, synchronous rectification is enabled.
Condition to enter Lock Protection mode in OCP active	0x010B	[1]	OCP_LAT_CLR	This register selects the status when OCP is happened. 0 : When OCP is happened, the motor stops until next power on sequence. 1 : When OCP is happened, the IC goes to “Lock Protection mode”
Speed control slope setting	0x010B	[0]	STEPSEL	This register sets control slope, when rotational speed change occurs by the speed control signal. (The amount is prescribed in the time per the 1FG pulse) 0: 1/4 of the existing speed, or +−2047rpm (Small one is chosen) 1: 1/8 of the existing speed, or +−1023rpm (Small one is chosen)
FG/RD select	0x010C	[1:0]	TACHSEL	These registers select FG pin function. 00: FG output 01: RD output (Rotation is Low, Locked motor is High) 10: FG output 11: RD output (Rotation is High Locked motor is Low)

Table 18. REGISTER ADDRESS 0x0100−0x0114 Register Description 2

Function	Address	Bits	Register Name	Description
Input PWM average setting	0x010D	[1:0]	PWMAV	Average number of times to perform when input PWM signal is read is set. 00: 0 times (Do not averaging) 01: 4 periods are averaged. 10: 8 periods are averaged. 11: 16 periods are averaged.
Mask time for reverse recovery time setting	0x010E	[1:0]	OCP_MASK	Masking time to ignore the reverse recovery time for both high−side and low−side Power FET is set. 00: 0.5us 01: 1.0us 10: 2.0us 11: 4.0us
OVP function enable	0x010F	[1]	IGNR_FAULT _$\overline{\text{OVP}}$	This register selects enable or disable of the OVP function. 0: OPV function enable 1: OVP function disable
Lock protection enable	0x0110	[3]	LOCK_FAULT	This register selects enable or disable of the lock protection function. 0: Lock protection enable 1: Lock protection disable
OFF time setting (TOP)	0x0111	[7:4]	MSKDEG_TP	The TOP shows commutation initiation time. These registers set OFF time at commutation initiation. Time or degree are selected in MSB 1bit, the OFF width section is set in lower 3bit. [7] and [3] 0: Degree 1: Time [6:4] and [2:0] 000: 0deg or 0s 001: 0.35deg or 2.0us 010: 0.70deg or 4.0us 011: 1.05deg or 10.0us 100: 2.10deg or 14.0us 101: 3.50deg or 20.0us 110: 4.90deg or 28.0us 111: 7.00deg or 40.0us
Feedback Gain Adjustment 1	0x0113	[7:4]	IX	Integral gain coarse 0000: 1x 0001: 2x 0010: 4x 0011: 8x 0100: 16x 0101: 32x 0110: 64x 0111: CUT 1000: 1x 1001: 1/2x 1010: 1/4x 1011: 1/8x 1100: 1/16x 1101: 1/32x 1110: 1/64x 1111: CUT

Table 18. REGISTER ADDRESS 0x0100−0x0114 Register Description 2

Function	Address	Bits	Register Name	Description
Feedback Gain Adjustment 2	0x0113	[2:0]	IG	Integral gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x
Feedback Gain Adjustment 3	0x0114	[6:4]	PX	Proportional gain coarse 000: 1x 001: 2x 010: 4x 011: 8x 100: 16x 101: 32x 110: 64x 111: CUT
Feedback Gain Adjustment 4	0x0114	[2:0]	PG	Proportional gain fine 000: 1x 001: 7/8x 010: 6/8x 011: 5/8x 100: 4/8x 101: 3/8x 110: 2/8x 111: 1/8x

10. The details refer to Application Note “AND9737/D”

Table 19. REGISTER ADDRESS 0x0219 Register Description

Function	Address	Bits	Register Name	Description
Communication error status (Note 11)	0x0219	[6:0]	SWI_ERR	Communication error status store to these registers. (Read only) The details refers to a clause of “COMMUNICATION ERROR”.

11. The details refer to Application note AND9737.

Table 20. REGISTER ADDRESS 0x0400−0x0407 Register Description

Function	Address	Bits	Register Name	Description
Register selection for reloaded data from NVM	0x0400	[6]	DATA_SEL	NVM input data multiplexer control. 0 Distributed normal bit 1 : NVM input data register
Memory write setting 1	0x0400	[5]	YFINC_EN	Select BYTE_SEL value auto−increment function. Need to be 0 for this part. 0: Disable 1: Enable
Memory write setting 2 (Note 12)	0x0400	[4:3]	VPP_REFSEL	Set VPP regulator voltage for NVM Program/Erase. This bit is available when VPP_REG_EN=1. 00 : 6.3V for NVM Program 01 : 3.9V for NVM Program verify 10 : 9.0V for NVM Erase 11 : 3.0V for NVM Erase verify
Memory write setting 3	0x0400	[2:0]	YFOPEMODE	Select nonvolatile memory operation mode. 000: Read 010: Erase 011: Erase verify 100: Program 101: Program verify Other than the above: use prohibition
Memory write setting 4 (Note 12)	0x0402	[2]	VPP_REG_EN	This register sets the internal regulator in NVM Program/Erase 0: Turn off the internal regulator in case of using external power supply 1: Turn on the internal regulator for NVM Program/Erase.
Memory write setting 5	0x0402	[0]	EN_FTP	Enable to access nonvolatile memory. 0: Disable 1: Enable
Memory status	0x0403	[5]	YF_PE_BUSY	Status bit for nonvolatile memory. (Read only) 0: Operation finished. Ready. 1: Operation on−going. Busy.
Memory access trigger	0x0403	[0]	OP_FTP	Control of the operation of nonvolatile memory 0: Stand−by 1: Execute
Memory write setting 6	0x0404	[7:0]	PRG_LNGT	Set the Program time to nonvolatile memory.
Memory write setting 7	0x0405	[7:0]	ERS_LNGT	Set the Erase time to nonvolatile memory.
Memory write setting 8	0x0406	[7:0]	BYTESEL	Select the byte of Write/Erase to nonvolatile memory.
	0x0407	[3:0]		

12. This function is not guaranteed for LV8316HA. Don't use it for NVM operation.

COMMUNICTION ERROR

The Communication error is reported in the Register (Address 0x0219). Table 21 shows the error report functions.

Table 21. ERROR REPORT DESCRIPTION

Address		Reg.	Name	Content	State after Error		
[15:8]	[7:0]				Mode	Communication	Transferred Data
0x02	0x19	D[6]	R/W Field Data Error	Non−zero value is written in the D[5:1] in R/W Field	Wait for the data from the master	Enable	In write mode ; Nullified In read mode ; No action
		D[5]	Time out Error	The delay between the fields in “Communication mode” is longer than 3 fields	“Standby”	Terminated	−−−
		D[4]	Check−Sum Error	Check−Sum value is wrong in write mode	“Error”	Terminated	Nullified
		D[3]	Data Length Field parity Error	The parity in “Data Length Field” is wrong	“Error”	Terminated	Nullified
		D[2]	R/W Field parity Error	The parity in “R/W Field” is wrong	“Error”	Terminated	Nullified
		D[1]	Header Error	Header input is not correct	“Error”	Terminated	Nullified
		D[0]	Framing Error	The signal pin is “Low” state in Stop bits	“Error”	Terminated	Nullified

“Time out Error” posts “1” in the D [5] of Reg. 0x0219 and the slave goes to “Standby mode”.

If the data length is long and the “Time out Error” is happened during the Register write, the data with the correct “Check−Sum” transferred before the “Time out Error” is stored in register, then the slave goes to “Standby mode”.

“Check−Sum Error” posts “1” in the D [4] of Reg. 0x0219. If it happens in write mode, the slave goes to “Error mode”, the communication is terminated and the transferred data is discarded. If the “Check−Sum Error” is happened, the data with the correct “Check−Sum” transferred before “Check−Sum Error” is stored in register, then the slave goes to “Error mode”.

Other errors, except for “R/W Field Data Error” also write “1” in the specified register and the slave goes to “Error mode” as well. To recover from “Error mode”, the communication pin should be kept “High” for longer than the times corresponding to 4 “Fields”, then the slave goes to “Standby mode” automatically despite of the status of error register.

Each error register keeps the error state until the master reads the error register. For example, the “Check−Sum Error” occurs first, and the slave goes to “Standby mode” through 4 “Fields” delay, then it goes to “Communication mode” again and “Framing Error” occurs. In this case, the master doesn’t read any error registers, hence, D [4] and D [0] post “1”. After reading D [4] and D [0] of Reg.0x0219, these are cleared to “0”. The notice is to clear the error, to read Reg.0x0219 as a 1 byte. If you read multiple registers including Reg.0x0219, the error is not cleared.

The recommendation is to read the error register after every operation to confirm whether the communication completes successfully.

Figure 33 shows the state diagram and refer the application note AND9761 as well about the communication.

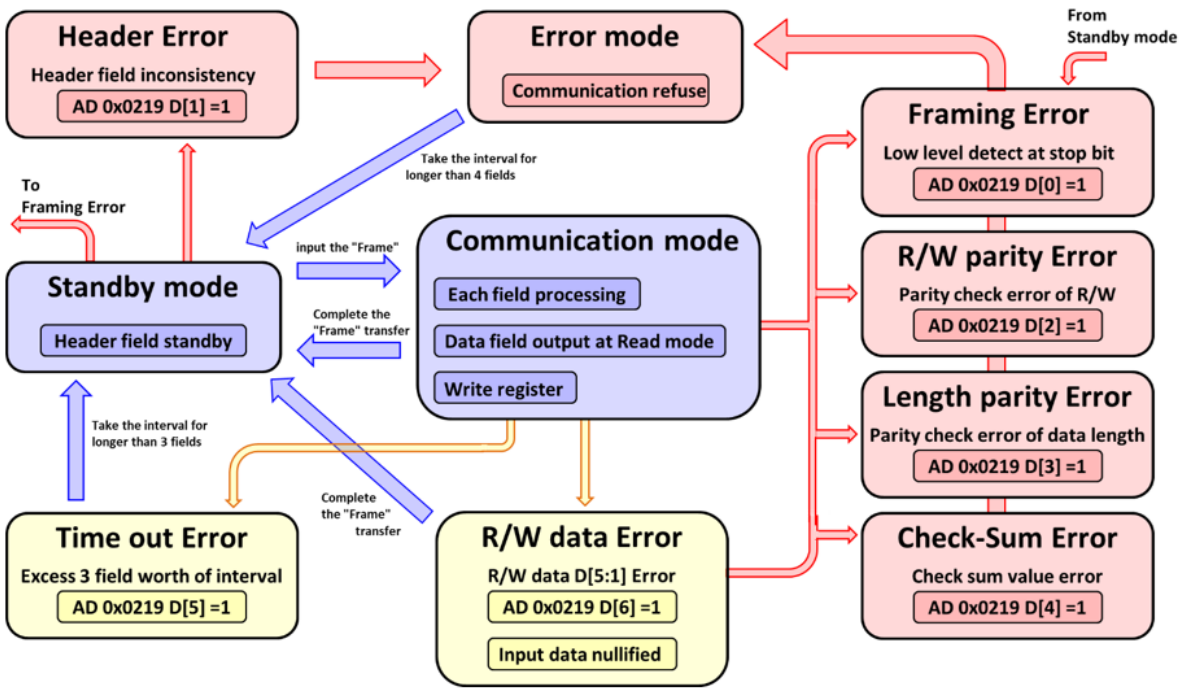


Figure 33. State Transition Diagram of Each Error

PCB GUIDELINES

Thermal Test Conditions

Specified circuit board: Toroidal shaped, the diameter is 23 mm, inside diameter is 11 mm and thickness is 0.8 mm, glass epoxy 2−layer board which has 1 oz internal power and ground plane and 1/2 oz copper traces on top and bottom of the board.

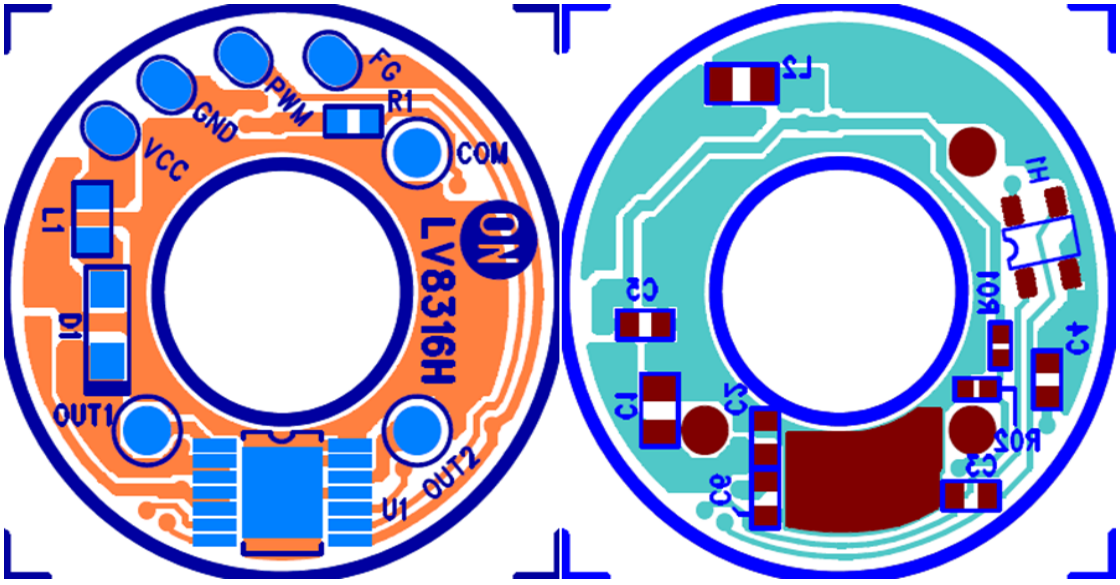


Figure 34. State Transition Diagram of Each Error

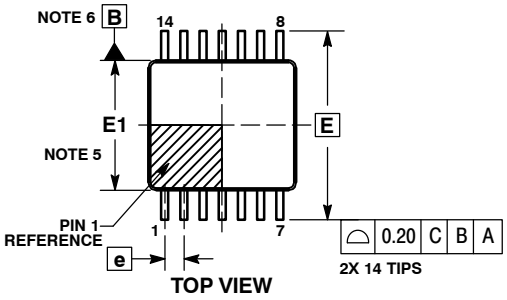
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

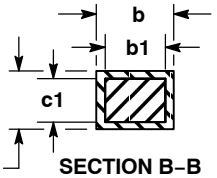
TSSOP−14 EP
CASE 948AW
ISSUE C

DATE 09 OCT 2012

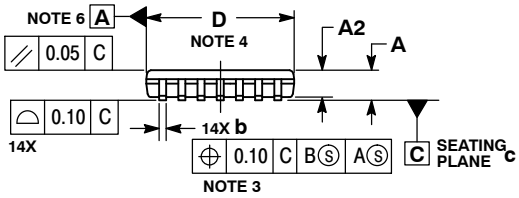
SCALE 1:1



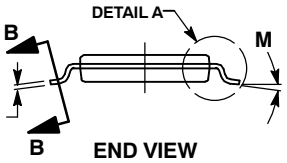
TOP VIEW



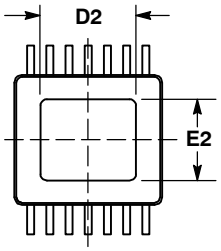
SECTION B−B
NOTE 8



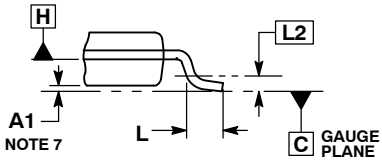
SIDE VIEW



END VIEW



BOTTOM VIEW

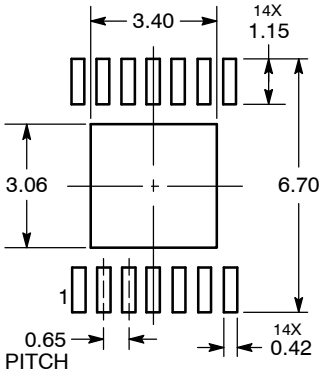


DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

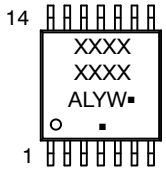
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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NEW STANDARD:		
DESCRIPTION:	TSSOP−14 EP, 5.0X4.4	PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY J. KREMMER.	12 JAN 2012
A	CHANGED DATUM SCHEME FOR GD&T. REQ. BY J. KREMMER.	26 JAN 2012
B	CHANGED DIMENSION D2 TO 3.09 MIN & 3.35 MAX. REQ. BY J. KREMMER.	02 MAR 2012
C	UPDATED EXPOSED PAD DIMENSIONS. REQ. BY J. KREMMER.	09 OCT 2012

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