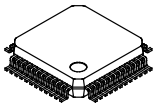
LV89031

Product Preview

Multi-purpose BLDC Pre-driver, For Automotive

ON Semiconductor®

http://onsemi.com



SQFP48 (7mmx7mm)

ORDERING INFORMATION

Ordering Code:
LV89031UWR2G

Package
SPQFP48
(Pb-Free / Halogen Free)

Shipping (Qty / packing)
2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Overview

The LV89031 is a 3-phase BLDC/PMSM pre-driver with integrated BEMF (Back ElectroMotive Force) sensing and logic level FET compatibility. The wide operating voltage range and AEC-Q100 qualification make this device ideal for automotive applications. Six gate drivers provide 400mA (typ) gate current to external power bridges allowing use of low-resistance power FETs as well as logic level FETs. All FETs are protected against overcurrent, short-circuit, over-temperature and gate undervoltage. Three independent low-side source pins allow multiple shunt measurement.

The device also includes a programmable linear regulator, a fast current-sense amplifier and a window watchdog for microcontroller support. An SPI interface allows for real time parameter setup and diagnostics. Critical system parameters can be programmed into non-volatile OTP memory.

Junction temperature tolerance up to 175°C and control via wide level WAKE and PWM signals make the LV89031 an ideal motor pre-driver for automotive applications such as engine cooling fans, fuel, oil, and hydraulic pumps.

Features

- Full drive power from 8V to 28V supply voltage with transient tolerance from 4.5V to 40V.
- Extended voltage range from 6V to 33V using logic-level mode.
- Up to TBDkHz motor PWM with individual six gate control or Drive-3 mode with integrated programmable dead-time.
- 2% accurate 5V/3.3V linear regulator for external loads up to 50mA.
- Extensive system protection features including:
  - Drain-Source short detection.
  - Overcurrent shutoff.
  - Low gate voltage warning.
  - Overtemperature warning and shutoff.
  - Over/under voltage protection.
- SPI interface for parameter setup and diagnostic access, dynamic access to dead-time, amplifier gain, and short circuit levels
- Non-volatile (OTP) memory for storing critical system parameters.
- Wide voltage enable line and PWM interface.
- Integrated window watchdog timer function.
- AEC-Q100 qualified and PPAP capable.
- Thermally efficient exposed die 48 pin QFP package for transient operation up to 175°C.

Typical Applications

- Automotive Fuel, Oil, Water or Hydraulic Pumps.
- Automotive Actuators.
- Automotive HVAC and cooling Fans.
- Battery operated Hand Power tools.
- White Goods.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

INTERNAL EQUIVALENT BLOCK DIAGRAM AND APPLICATION CIRCUIT

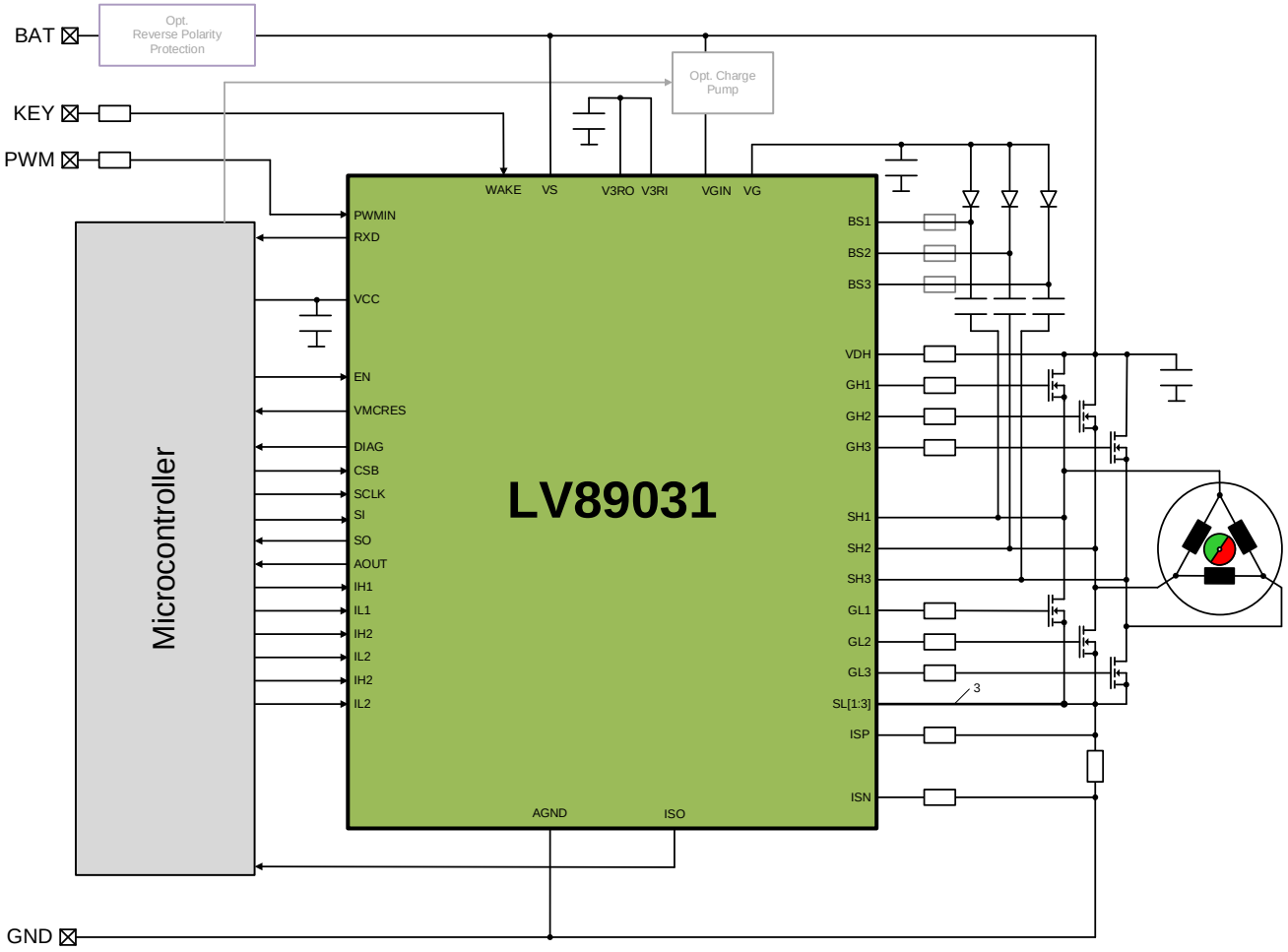


Figure 1: Typical Application Diagram

PIN ASSIGNMENT

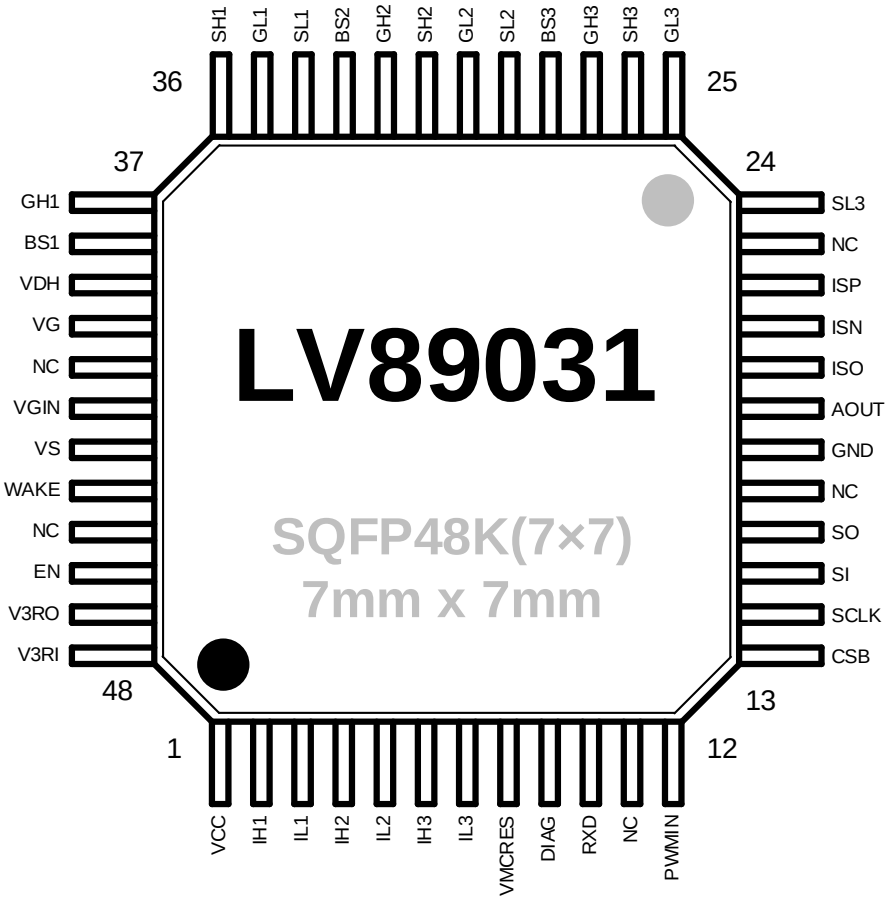


Figure 2: LV89031 Pinout

PIN ASSIGNMENTS & PIN DESCRIPTION

Name	No.	Description
VCC	1	5V or 3.3V linear regulator output. (Selected by SPI register setting) Can provide up to 50mA.
IH1	2	Active high, 3.3V digital control input to activate GH1.
IL1	3	Active low, 3.3V digital control input to activate GL1.
IH2	4	Active high, 3.3V digital control input to activate GH2.
IL2	5	Active low, 3.3V digital control input to activate GL2.
IH3	6	Active high, 3.3V digital control input to activate GH3.
IL3	7	Active low, 3.3V digital control input to activate GL3.
VMCRES	8	Open drain reset output for the microcontroller. Goes low for VCC undervoltage fault, optionally for watchdog reset and thermal shutdown .
DIAG	9	Open drain error or diagnostic output to be connected to microcontroller interrupt line. DIAG functionality is defined by internal register settings.
RXD	10	Active high, open drain PWM data output to microcontroller.
NC	11	
PWMIN	12	VS level PWM input pin for wake on PWM functionality. Digital level of PWMIN is applied to RXD.
CSB	13	Active low, 3.3V digital SPI interface chip selection pin
SCLK	14	3.3V SPI Interface Clock input pin. SI Data is latched during the rising edge.
SI	15	3.3V SPI Interface Serial data input pin.
SO	16	SPI Interface Serial data output pin. High level is pulled to VCC.
NC	17	
GND	18	Ground pin
AOUT	19	Output for various internal analog signals, such as: motor phase voltage M[1-3], supply voltage VDH, gate voltage VG. Actual signal is selected via SPI register. Scaled to 2V full scale range.
ISO	20	Output pin for current sense amplifier. Connect to AD converter input of the microcontroller for current sensing. Gain, reference, and overcurrent threshold is programmable via SPI register. Full scale range = 3V.
ISN	21	Shunt resistance reference pin. Connect this pin through TBD resistor to the GND side of the Shunt resistor with Kelvin leads.
ISP	22	Motor current sense pin. Connect this through TBD resistor pin to top side of shunt resistor with Kelvin leads.
NC	23	
SL3	24	Low side source connection of the power stage. Return path for gate current of GL3. Connect to source of FET controlled by SL3 or to common source of the power stage.
GL3	25	Gate driver output for low side FETs. Switches between VG and SL3. Use optional gate resistor for signal shaping.
SH3	26	Connection for the motor phase terminal controlled by GH3 and GL3. Return path for high-side drivers and input for back EMF sensing.
GH3	27	Gate driver output for high side FETs. Switches between BS3 and SH3. Use optional gate resistor for signal shaping.
BS3	28	Supply pin for high side driver GH3. Needs a bootstrap capacitor to SH3 and a diode to VG.
SL2	29	Low side source connection of the power stage. Return path for gate current of GL2. Connect to source of FET controlled by SL2 or to common source of the power stage.
GL2	30	Gate driver output for low side FETs. Switches between VG and SL2. Use optional gate resistor for signal shaping.
SH2	31	Connection for the motor phase terminal controlled by GH2 and GL2. Return path for high-side drivers and input for back EMF sensing.
GH2	32	Gate driver output for high side FETs. Switches between BS2 and SH2. Use optional gate resistor for signal shaping.
BS2	33	Supply pin for high side driver GH2. Needs a bootstrap capacitor to SH2 and a diode to VG.
SL1	34	Low side source connection of the power stage. Return path for gate current of GL1. Connect to source of FET controlled by SL1 or to common source of the power stage.

Name	No.	Description
GL1	35	Gate driver output for low side FETs. Switches between VG and SL1. Use optional gate resistor for signal shaping.
SH1	36	Connection for the motor phase terminal controlled by GH1 and GL1. Return path for high-side drivers and input for back EMF sensing.
GH1	37	Gate driver output for high side FETs. Switches between BS1 and SH1. Use optional gate resistor for signal shaping.
BS1	38	Supply pin for high side driver GH3. Needs a bootstrap capacitor to SH1 and a diode to VG.
VDH	39	Sense input for supply voltage and short circuit detection of high side power Fets. Connect through TBDkOhm resistor to common drain of the power bridge.
VG	40	Power supply pin for low-side gate drive GL[1-3] directly and GH[1-3] through bootstrap circuit. Connect decoupling capacitor between VG and GND.
NC	41	
VGIN	42	Gate supply input. Normally shorted to VS. Insert a chargepump circuit between VS and VGIN if low voltage operation is required.
VS	43	Power supply pin.
WAKE	44	WAKE up pin for internal power supply. “H” => Operating mode, “L” or “Open” => Sleep mode.
NC	45	
EN	46	Active high digital input. A high on EN will activate the outputs. EN can be used as a hold input to allow an external microcontroller to keep the IC operating even if WAKE is low. A falling edge on EN clears the error flags.
V3RO	47	Internal regulator output pin. Connect capacitor between this pin and GND.
V3RI	48	Internal regulator feedback pin (Control circuit and Logic power supply). Connect to V3RO pin. No external loads allowed.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Parameter	Pins	Ratings	Unit
Supply voltage	VS, VDH, VGIN	-0.3 to 40	V
Gate voltage to GND	VG	-0.3 to 40	V
Bootstrap to GND	BS[1-3]	-0.3 to 40	V
Bootstrap to SH[1-3]	BS[1-3]	-0.3 to 40	V
Logic power supply	V3RI, V3RO	-0.3 to 3.6	V
5V regulator voltage	VCC	-0.3 to 5.5	V
VS level signal voltage	WAKE, PWM	-0.3 to 40	V
Digital inputs	CSB,EN,SCLK,SI,IH[1-3],IL[1-3]	-0.3 to 40	V
Open drain voltage	VMCRES, RXD, DIAG	-0.3 to 40	V
Digital output voltage	SO	-0.3 to V_{VCC}+0.3	V
Current sense input	ISP, ISN	-3 to V_{V3RI}+0.3	V
Analog output	ISO, AOUT	-0.3 to V_{V3RO}+0.3	V
High-side output to GND	GH[1-3]	-3 to 40	V
Motor phase	SH[1-3]	-3 to 40	V
Low-side output to GND	GL[1-3]	-3 to 40	V
Low-side source pin to GND	SL[1-3]]	-3 to 40	V
Voltage between HS gate and phase	GH[n] to SH[n] for n={1,2,3}	-0.3 to 20	V
Allowable Power SQFP48K	at 70 °C	2430	W
Thermal resistance	JA = Junction Ambient	33	°C/W
(JESD51-7)	JC = Junction Case	2	°C/W
Storage temperature		-55 to 150	°C
Junction temperature		-40 to 150	°C
	(Note 2)	150 to 175	°C

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Operation outside the Operating Junction temperature is not guaranteed. Operation above 150C should not be considered without a written agreement from ON Semiconductor Engineering staff.

ELECTRICAL CHARACTERISTICS

Valid at a junction temperature range from -40℃ to 150℃, for supply Voltage 8.0V≦VS≦25V unless otherwise specified. Typical values at 25°C and VS=13.5V unless specified otherwise. (Note 3)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VS supply voltage range		Normal mode	8	13.5	25	V
		Logic level mode	6		33	V
		Full logic functionality, driver stage off. (t< 400ms) (Note 4)	4.5		40	V
VS supply current		Standby mode		30		mA
		Sleep mode at 25ºC		20	TBD	μA
WAKE input voltage		Low level	0		1.3	V
		High level	2.7		VS	V
WAKE pulldown resistor				100		kΩ
PWMIN switching levels		Low level	0		40%	VS
		High level	60%		100%	VS
PWMIN pulldown resistor				100		kΩ
PWMIN frequency range			0		30	kHz
INTERNAL REGULATOR						
V3RO output voltage			3.135	3.3	3.465	V
VCC CONSTANT VOLTAGE OUTPUT						
Output voltage 5V		REGSEL=1	-2%	5.00	+2%	V
Output voltage 3.3V		REGSEL=0	-2%	3.3	+2%	V
		VS = 4.5V, I_{VCC}=50mA	3.0			V
Voltage regulation					50	mV
Load regulation		Io=-5mA to -25mA			50	mV
Output current limit			50		TBD	mA
GATE DRIVERS						
Low-side Rdson to SL[1-3]		“L” level Io=10mA		6	15	Ω
Low-side Rdson to SH[1-3]		“H” level Io=-10mA		12	22	Ω
High-side Rdson to SH[1-3]		“L” level Io=10mA		6	15	Ω
High-side Rdson to BS[1-3]		“H” level Io=-10mA		12	22	Ω
Propagation delay ON		50% IHx to 20% GHx. Cload = 0nF			120	nS
Propagation delay OFF		50% IHx to 80% GHx. Cload = 0nF			120	nS
Propagation delay ON Difference SH[1-3],SL[1-3]			-20		20	nS
Propagation delay OFF Diff erence SH[1-3],SL[1-3]			-20		20	nS
GATE VOLTAGE OUTPUT (VG)						
VG output voltage		Normal mode, IVG < 40mA	7.0	11.0	12.0	V
		Logic level mode	5	6	7	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
		VS = 6V, IVG < 30mA	5			
VG current limit			40		TBD	mA
BEMF DETECTION						
BEMF divider ratio				1/16		
BEMF divider mismatch			-2		2	%
BEMF divider settling time (20% - 80% FSR)				TBD		µs
VDH divider ratio				1/32		
VDH divider mismatch			-2		2	%
VDH divider settling time (20% - 80% FSR)				TBD	2	µs
Thermal voltage		Tj = 155deg	690	705	710720	mV
Thermal slope		(Note 5)		-2		mV/°C
AOUT full scale range			TBD		2	V
AOUT output resistance		I_{AOUT} =+-100uA			200	Ω
AOUT output current			-100		100	µA
CURRENT SENSING (ISP, ISN, ISO)						
IP, IN input current			-50		50	µA
Input offset voltage		GAIN = 7.5	TBD		TBD	mV
Reference voltage ISO		OCVR = 0	1.425	1.5	1.575	V
		OCVR = 1		0.2		V
Gain		OCGAIN = 00		7.5		
		OCGAIN = 01		15		
		OCGAIN = 10		22.5		
		OCGAIN = 11		30		
Common mode range			-0.2	1	2	V
ISN, ISP differential voltage			-200		200	mV
ISO full scale range			0.1		3	V
Amplifier settling time (20% - 80% FSR)		Gain = 15, 0.25V<V_{ISO}<3V			1000	ns
ISO output resistance*		I_{ISO}=+-100uA			200	Ω
ISO output current			-100		100	µA
Overcurrent voltage level V_{ISP}-V_{ISN}		OCDL = 00		200		mV
		OCDL = 01		150		mV
		OCDL = 1x		100		mV
ACTIVE HIGH DIGITAL INPUTS (EN, SCL, SI, IH[1-3])						
High-level input voltage			80%			V3RI
Low-level input voltage					20%	V3RI
Pull-down resistance				100		KΩ
ACTIVE LOW DIGITAL INPUTS (CSB, IL[1-3])						
High-level input voltage			80%			V3RI

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Low-level input voltage					20%	V3RI
Pull-up resistance to VCC				30		KΩ
DIGITAL OUTPUTS (SO)						
Output voltage		Io=-1mA	V_{VCC} -0.2			V
		Io=1mA			0.2	V
OPEN DRAIN OUTPUTS (VMCRES, DIAG, RXD)						
Output voltage		Io=1mA			0.2	V
Input leakage current					10	μA
WARNING AND PROTECTION						
Thermal warning (Note 5) (Junction temperature)		TSTS=0	125			°C
		TSTS=1	150			°C
		Hysteresis		25		°C
Thermal shutdown (Note 5) (Junction temperature)		TSTS=0	150			°C
		TSTS=1	175			°C
		Hysteresis		25		°C
VS voltage warning		Over-voltage	16	17	18	V
		Under-voltage	7	7.5	8	V
VDH voltage warning		Over-voltage	25	26.5	28	V
VG under-voltage			5	6	7	V
		Logic level mode	3.5	4	4.5	V
VCC under-voltage		REGSEL = 0	2.3		2.7	V
		REGSEL = 1	3.8		4.2	V
V3IO under-voltage					2.7	V
Detection filter time						μs
WATCHDOG						
WD first open window		WDWT[2:0] typical values	3.2		409.6	ms
WD closed window time		WDWT[2:0] typical values	0.8		102.4	ms
WD open window time		WDWT[2:0] typical values	1.6		204.8	ms
WD reset duration				400		μs
SPI INTERFACE						
SPI clock frequency					4.5	MHz

3.Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions

4. Valid for limited time duration of 400ms (Load dump)

5. Not tested in production. Verified during qualification only.

DETAILED FUNCTIONAL DESCRIPTON

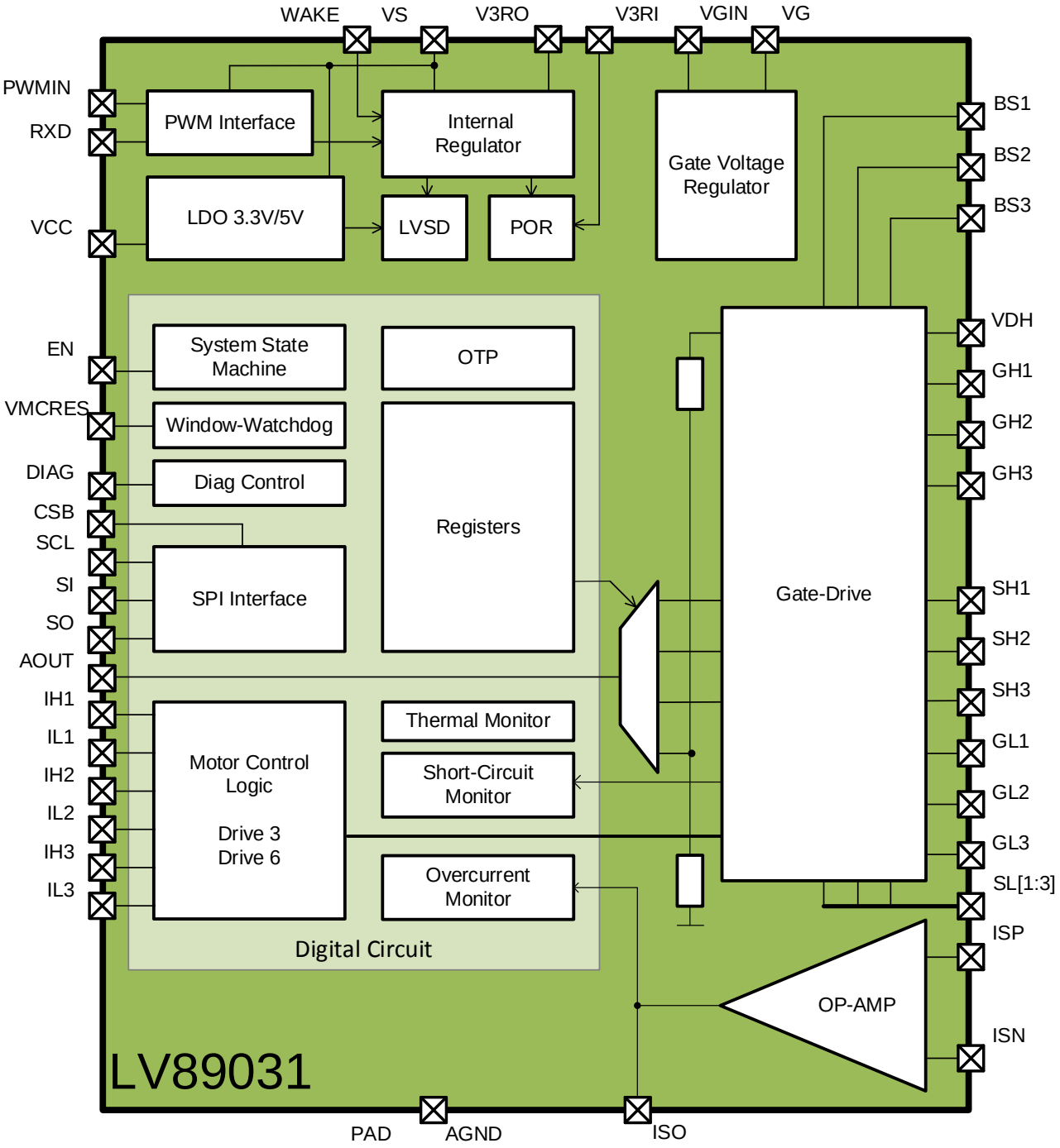


Figure 3: Block Diagram

Chip Activation, System States and Shutdown (EN, WAKE)

Once the supply voltage VS rises above 4.5V(min) the the LV89031 enters Sleep Mode. In Sleep mode system states are controlled with pin WAKE.

Table 1) Operation Modes

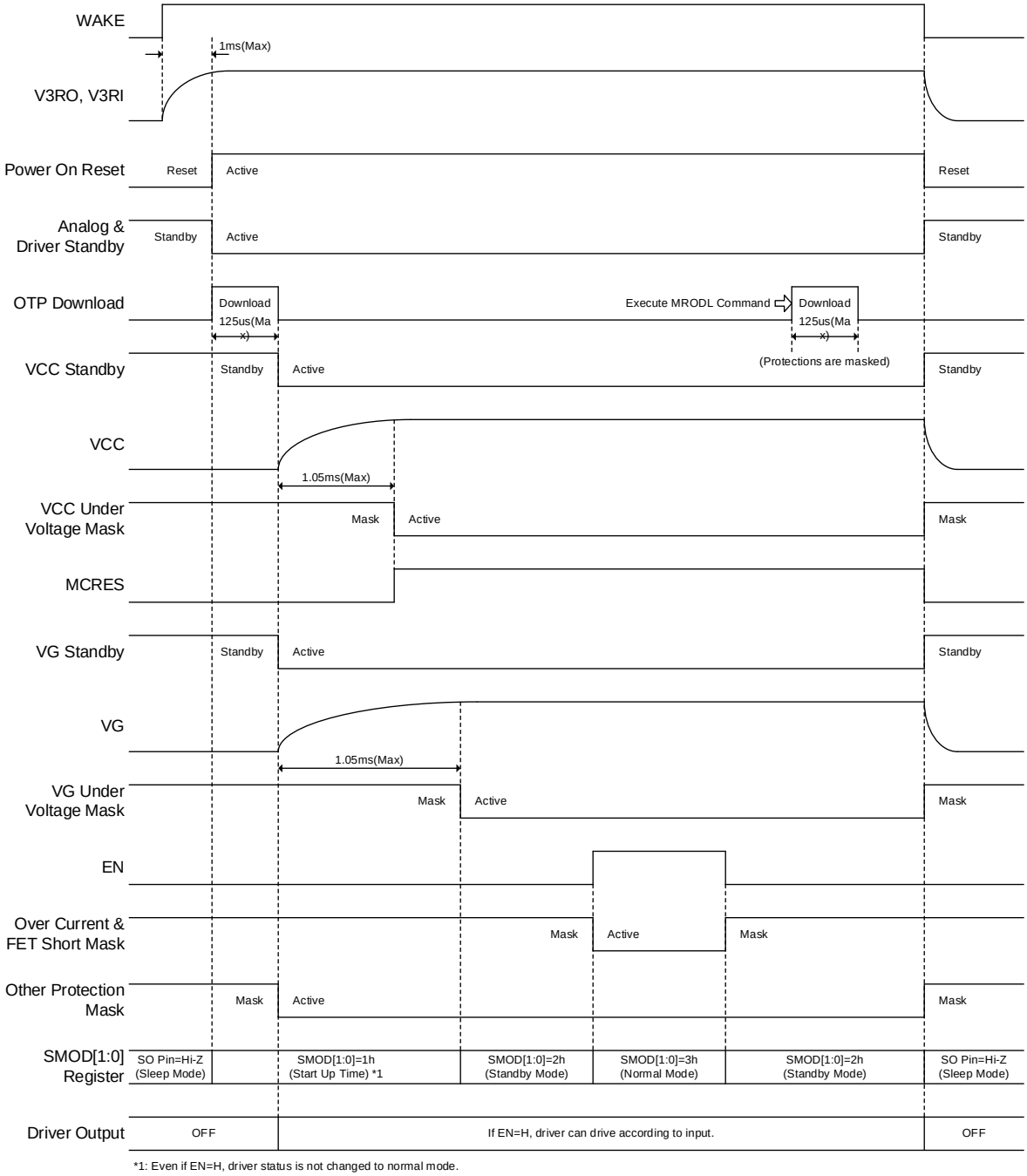
Mode	WAKE	EN	V3RO	Logic	VCC	VG	SPI	drivers
Sleep	L	×	Disable	Reset	Disable	Disable	Disable	High-Z
Standby	H	L	Enable	Active	Enable	Enable	Enable	Low
Normal	x	H	Enable	Active	Enable	Enable	Enable	Active

A high level on WAKE >2.5V(max) activates the IC from sleep mode and enables the internal linear regulator at V3RO. Once the voltage on V3RO as sensed on V3RI has passed the power on reset (POR) threshold the system oscillator starts, and after 3.2us(typ) releases the internal digital reset. OTP register contents are loaded into the system registers defining the power on state of the LV89031 and the VCC regulator voltage.

VCC is powering up next, holding the CPU reset line VMCRES low until VCC passes its undervoltage level . During the entire wake-up sequence of TBD ms(typ) DIAG is masked for VG undervoltage. After wake-up is complete, the IC enters Standby mode and DIAG is activated to display internal errors. During Standby mode full SPI access is possible.

Note that if the CPU watchdog was enabled via OTP, a VMCRES low will be asserted after 410ms(typ) unless the watchdog is being triggered properly. See section A high on EN takes the LV89031 from Standby to Normal mode. Normal mode allows motor control and the IC accepts control inputs via the motor control pins IH[1-3], IL[1-3]. A low on EN disables the motor stage regardless of the PWM input and returns the part back to Standby mode.

The IC is shut down by taking WAKE below 1.3V(min) if EN is low. If EN is high, a low on WAKE will be ignored until the uC pulls EN low.



*1: Even if EN=H, driver status is not changed to normal mode.

Figure 4: Powerup and Shutdown Timing

Operating Voltage Range
Normal operation with full functionality is guaranteed from 8V to 2?V. The device will operate from 4.5V to 40V with limited performance:

Shutdown: VS < 4.5V
The IC will be off. Gate drivers < VS.

Undervoltage: 4.5V < VS < 6V
VS undervoltage warning will be flagged. VG undervoltage warning may be asserted. If VCC is programmed to provide 3.3V to the microcontroller, it will be supplied. If motor operation is required during Undervoltage see section below.

Low Voltage: 6V < VS < 8V
VS undervoltage warning will be flagged. VG undervoltage warning may be asserted. VCC will provide power to the microcontroller. The motor can operate but may be in low gate enhancement mode if standard level Fets are used. If full enhancement is required see section below.

Normal: 8V < VS < 16V
Normal operation.

High Voltage: Operation16V < VS < 25V
Normal operation. VS overvoltage warning will be flagged.

Overvoltage: 25V < VS < 40V
VDH overvoltage warning will be flagged. The driver stage can be programmed to let the motor freewheel to protect the boostrap circuitry at BS[1-3] from overstress. This works if the motor is not operating in field weakening.

In case of active braking, or field weakening operation, the microcontroller will have to react to a VDH overvoltage warning by either disabling the driver stage or activating all low side Fets to brake the motor. The maximum allowable VS level for motor operation is 40V - V_{VGmax} = 28V or 33V depending on the state of register VGVSEL. For additional protection add zener diodes to the bootstrap pins as shown in Figure TBD.

Motor operation during undervoltage
An undervoltage chargepump is not included into the LV89031 to save cost. If undervoltage operation of the motor is desired either an external chargepump must be inserted between VS and VGIN, or it is possible to use the device in logic level mode by setting MRCONF0[1]. In the latter case logic level Fets must be used for the inverter stage.

System Power Supplies
Three power supplies are integrated into the LV89031, all are supplied by VS:

- An internal 3.3V regulator which provides power to the digital and interface section.
- A linear regulator to provide 5V or 3.3V for external loads such as a microcontroller.
- The VG regulator for the gate voltages of the inverter stage.

Internal Regulator (V3RO, V3RI)
The internal regulator provides 3.3V at V3RO and takes its feedback from V3RI. V3RO and V3RI need to be connected externally and bypassed to GND for stability. This regulator may be used for pullup resistors on the open drain outputs, but the load should not exceeding 1mA.

LDO 3.3/5V (VCC)
VCC becomes active during Standby mode and can be configured via registers to provide 5V or 3.3V. VMCRES low is asserted if the output voltage drops below the threshold levels. VCC may power external loads up to 50mA(max) and must be bypassed to GND with an external capacitor. The voltage level is programmed in register VCVSEL with OTP backup.

Gate Voltage Regulator (VGIN,VG)
The gate voltage regulator is supplied by VGIN and regulates to either 11V(typ) or 6V(typ) at VG. The voltage level is programmed in register VGVSEL with OTP backup.

VG provides the drive voltage for the low-side drivers GL[1-3] directly and for the high side drivers VGH[1-3] through the bootstrap circuitry. The output is current limited to 40mA(min). C_{VG} The output at VG should be bypassed with a capacitor C_{VG} to GND which should be at least TBD times the maximum gate charge of the power Fets.

Motor Contol Inputs
Once the LV89031 is in standby mode with the supplies running a microcontroller can facilitate motor control via the inputs EN, IL[1-3], IH[1-3]. All are VS compatible. Additionally a supply level compatible level shifter can bring a high voltage control such as a PWM signal or a crash indicator to microcontroller supply level.

PWM Interface (PWMIN, RX)
The PWM interface translates a VS level signal with a threshold of 50%(typ) VS to a digital signal appearing at RX. This signal can be used for input PWM translation or for CRASH signal communication from outside the application to the microcontroller.

Drive Enable (EN)
Taking EN high enables the output drivers GH[1-3] and GL[1-3] for control by the microcontroller, taking EN low disables them by switching all of them to the sources of the corresponding external FETs. In addition, a high on EN will override a low on WAKE allowing the microcontroller to keep the motor running even after the WAKE line has gone low.

Motor Control (IL[1-3] IH[1-3])
The individual motor phases are controlled by inputs IL[1-3] and IH[1-3]. IH[1-3] are active high, while IL[1-3] are active low allowing for parallel control with only three PWM outputs using internal dead time. To control the driver stage GH[1-3] and GL[1-3] EN has to be “high”. The LV89031 will insert an adjustable dead time during output transitions to prevent short circuiting the FETs. Two drive modes exist:

Drive 6 Mode
In drive 6 mode each input independently controls it's corresponding output requiring 6 independent PWM channels in the microcontroller. A "high" on IH1 will result in a "high" on GH1. A "high" on IL1 will result in a "low" on GL1, and so forth. Trying to force a short by driving IH1 high and IL1 low will be ignored by the logic of the LV89031.

Input		Output	
IH[1-3]	IL[1-3]	GH[1-3]	GL[1-3]
L	L	L	H
L	H	L	L
H	L	L	L
H	H	H	L

Table 2) Drive 6 Mode

Drive 3 Mode
This mode is suitable for small microcontrollers which do not have 6 dedicated PWM control lines. IL[1-3] serve as enable signals for the phase drivers GH[1-3] and GL[1-3] while IH[1- 3] serve as their PWM inputs. Connect the microcontroller's PWM line to IH[1-3] and the phase select lines to the individual IL inputs 1-3 respectively.

Input		Output	
IH[1-3]	IL[1-3]	GH[1-3]	GL[1-3]
L	L	L	L
L	H	L	H
H	L	L	L
H	H	H	L

Table 3) Drive 3 Mode

Gate Drive
The gate drive circuit of the LV89031 includes 3 half-bridge drivers which control six external N-Channel Fet's. The high side gate drivers GH[1-3] switch their gate connection either to corresponding BS[1-3] pin or the respective phase connection SH[1-3]. The low-side gate drivers GL[1-3] are switched from VG to the corresponding source connection SL[1-3]. Both high and low side switches are hard switching, but saturate around 400mA/550mA(typ) for pullup/down currents. Slope control has to be implemented with gate resistors.

"Break before Make"
Current shoot-through protection of the bridge-drivers is implemented by ignoring inputs at IH[n] and IL[n] that would result in turning on of both high-and low-side FET at the same time. In addition a dead-time counter is implemented that begins counting after one driver has been turned off, and blocks the turning-on of the complementary driver for a programmable time t_{FDTI} from (typ) 200ns < t_{FDTI} < 3.2us (typ).

Dead-time counter
The dead-time counter uses a fixed minimum dead-time which can be programmed into 4bit parameter FDTILIM. The dead-time is never allowed to fall below that value. A dynamic dead time register FDTI allows dead time variation during motor operation. This register is uploaded at the beginning of every dead time measurement. Flag MRFDTIF is high when a dead time value has been written to register FDTI but was not uploaded to the counter, yet. Two consecutive writes to FDTI before a counter upload are flagged as an SPI error by setting bit SACF in the SPI status register GSDAT.

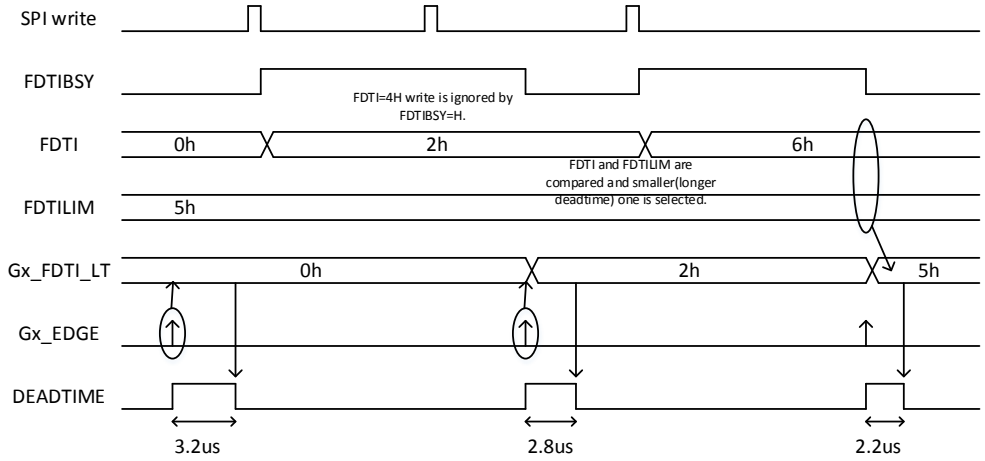


Figure 5) Dead Time Programming

Short Protection

To protect against FET shorts the drain-source voltage of the active external power fets is monitored. The drain source voltage of the high side Fets is monitored between VDH and the corresponding source SH[1-3]. While the low side Fets are monitored between SH[1-3] and SL[1-3]. After activation of the FET the short detection is masked for time t_{FSFT} to allow for signal settling. If after the masking time the voltage across the FET exceeds V_{FSDL} during debounce time t_{FSDT} a fet short error is flagged. For details see "**System Errors and Warnings"** on page 15.

4 bit register FSDL selects the short-circuit shutoff voltage between 1.6V > V_{FSLD} > 100mV(typ). The masking time can be between 0.8us < t_{FSF} < 3.2us(typ) as defined by register FSFT, and the debounce time is between 3.2us < t_{FSDT} < 12.8us(typ) as selected by FSDT. This register is dynamic and can be changed during motor operation.

Logic Level Mode

When using logic level Fets it may be difficult to keep the Fets off during phase switching transients. In this case it may be preferable to omit gate resistors at the gate drivers and place them in the bootstrap path instead. There they will slow the turning on of the high-side drivers, but will not interfere with their turn-off current.

Current Sensing and Overcurrent Shutoff

Single shunt current sensing can be implemented with the integrated high speed sense amplifier. It amplifies the voltage across ISP – ISN with a programmable gain defined by register CSGAIN to be 7.5, 15, 22 or 30. Access to this register is dynamic, allowing gain adjustment during motor operation. The offset is determined by CSOFEN relative to an internal reference which can be either 200mV(typ) for single ended sensing, or 1.5V(typ) for sensing current in both directions. The output of the current sense amplifier appears on ISO with a full scale range of 3V.

Overcurrent Shutoff

A parallel path implements fast overcurrent shutoff of the driver stage. Overcurrent shutoff is triggered if the voltage across ISP - ISN exceeds a programmable level of 100, 150 or 200mV(typ) - as defined by register OCDL. In overcurrent shutoff all gate drivers are driven low, turning the power FETs high-impedance and letting the motor freewheel – this reaction is maskeable. For more information on masking and recovery see section "**System Errors and Warnings"** on page 16. To suppress switching transients from causing an overcurrent fault a masking time 0.2us < t_{OCMASK} < 3.2us can be programmed into register OCMASK.

Temperature Sensing

The LV89031 monitors internal junction temperature T_j. The voltage representing this temperature (V_{PTAT}) can be sampled at AOUT as described below. Thermal warnings and errors are issued if T_j exceeds the levels defined by THTSEL:

THTSEL	Thermal Warning	Thermal Shutoff
0	125°C	150°C
1	150°C	175°C

Table 4) Thermal Thresholds

A thermal error may shut off the driver stage, VG and VCC regulator and trigger microcontroller reset by taking VMCRES low. The exact failure modes and masks are described in section "S**ystem Errors and Warnings"** on page 16**.**

Back EMF and other Measurments

The LV89031 includes a multiplexer for measureing the phase voltages, the motor voltage and the IC temperature. Depending on the state of AOUTSEL the following voltages appear on AOUT:

MRAOSEL[2:0]	Pin	Formula	Comment
0	VDH	$V_{VDH} = 32 \cdot V_{AOUT}$	Motor Supply Voltage
1	SH1	$V_{SH1} = 16 \cdot V_{AOUT}$	Phase Voltage 1
2	SH2	$V_{SH2} = 16 \cdot V_{AOUT}$	Phase Voltage 2
3	SH3	$V_{SH2} = 16 \cdot V_{AOUT}$	Phase Voltage 3
4	-	$T_j = (V_{AOUT} – 995.7mV) /2mV°C$	Internal junction temperature
5	-	High Impedance	

Table 5) AOUT Selection

Watchdog

The LV89031 includes a window watchdog to monitor the microcontroller. The size of the watchdog window is defined by register WDTWT. For detailed timing information see Figure 6: Window Watchdog Timing. A write access to register MRRST during open window time resets the watchdog timer and it starts counting again. The watchdog will issue an error whenever the is written to during closed window time or the watchdog time expires. Watchdog error effects can be customized.

For detailed error behavior an masking see section “**System Errors and Warnings”** on page 16.

After a watchdog induced microcontroller reset, the error register contents of registers MRDIAG[1-2] remain conserved until an SPI read access. This helps the microcontroller identify the fault condition.

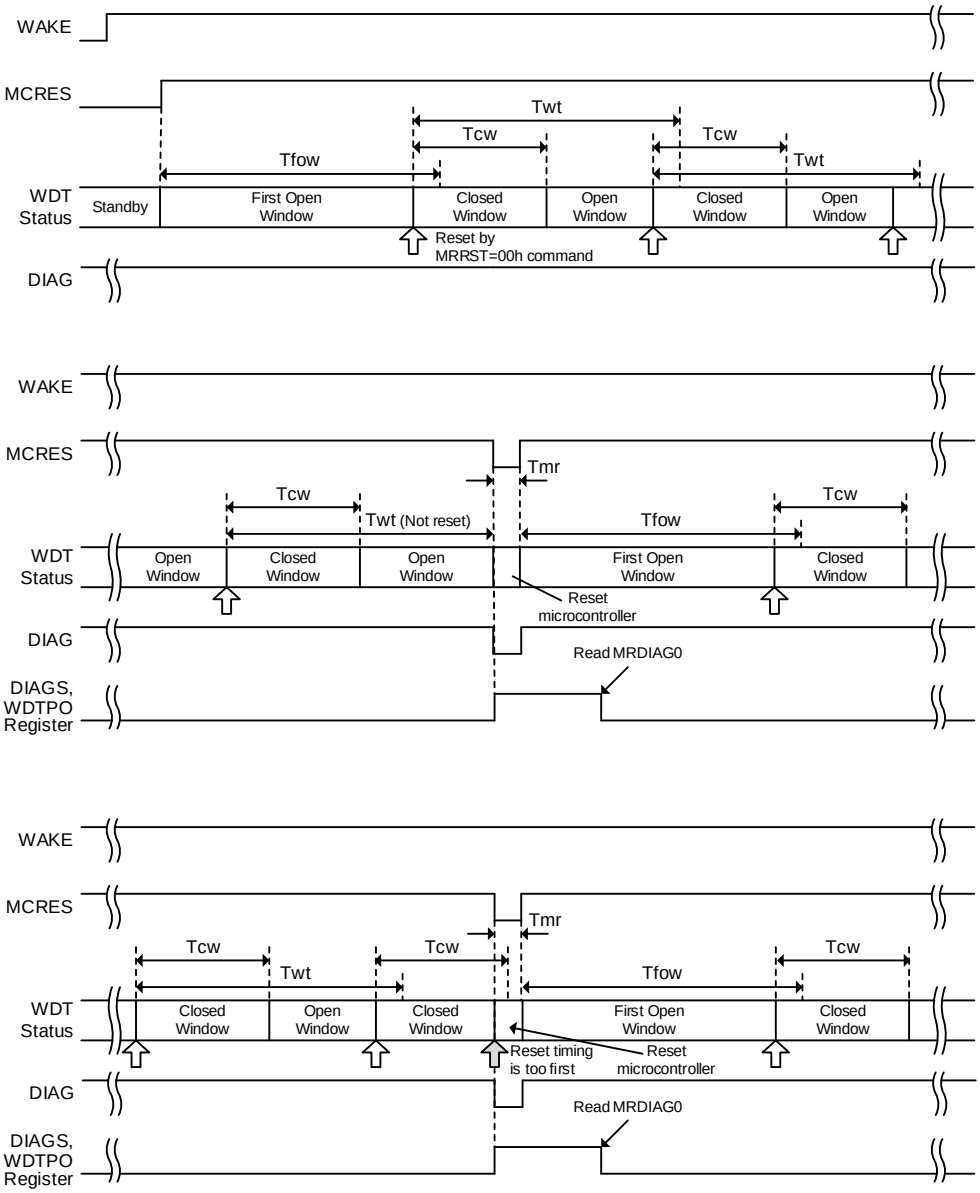


Figure 6: Window Watchdog Timing

Tj=-40 to 150°C, VS=4.5 to 40V

Symbol	Comment	Min	Typ	Max	Unit
Tfow	WDT first open window time WDTWT[2:0]=0h WDTWT[2:0]=1h : (1/2 step) WDTWT[2:0]=7h	 390.0 195.0 : 3.0	 409.6 204.8 : (1/2 step) 3.2	 431.2 215.6 : 3.4	ms
Tcw	WDT closed window time WDTWT[2:0]=0h WDTWT[2:0]=1h : (1/2 step) WDTWT[2:0]=7h	 97.4 48.7 : 0.7	 102.4 51.2 : (1/2 step) 0.8	 107.8 53.9 : 0.9	ms
Twt	WDT window time WDTWT[2:0]=0h WDTWT[2:0]=1h : (1/2 step) WDTWT[2:0]=7h	 195.0 97.4 : 1.4	 204.8 102.4 : (1/2 step) 1.6	 215.6 107.8 : 1.7	ms
Tmr	WDT microcontroller reset time	333	400	422	us

Table 6) Window Watchdog Timing Options

System Errors and Warnings

System erros and warnings are always flagged in their corresponding register MRDIAG0 and MRDIAG1 and their presence is indicated in SPI status register GSDAT. The LV89031 gives great flexibility in modifying the error response. Error response definition can be backed up into OTP.

All system errors and warnings can cause a transition on DIAG. The polarity of this transition is selected in bit DIAGPOL. DIAG should be connected to an interrupt input of the microcontroller. Errors that can cause serious damage such as short-circuit and overcurrent may be latched by enabling the corresponding latch bit in MRCONF10. In this case the LV89031 will keep the output stage disabled until the latch is cleared by one of the following actions:

- Power on reset.
- EN low.
- SPI write of FFh to MRRST.

Table 7) System Error and Warning Response Matrix

Error	*Reaction Setting Options*					*Reaction*				*Recovery Condition*	*Protection Enabled*
	Setup Register	**Mask DIAG**	**Report on DIAG**	**Auto Recover**	**Latch Off**	**VG**	**DRV**	**VCC**	**MC RES**		
VS Under Voltage	VSUVPS [1:0]	Yes	Yes	Yes	No	ON	(1)	ON	H	VS voltage recovers	After OTP download
VS Over Voltage	VSOVPS [1:0]	Yes	Yes	Yes	No	ON	(1)	ON	H	VS voltage recovers	After OTP download
VDH Over Voltage	VDOVPS [1:0]	Yes	Yes	Yes	No	ON	(1)	ON	H	VDH voltage recovers	After OTP download
VG Under Voltage	VGUVPS [1:0]	Yes	Yes	Yes	No	ON	(1)	ON	H	VG voltage recovers	After VG start-up time
VCC Under Voltage	-	No	No	Yes	No	ON	OFF	ON	L	VCC voltage recovers	After VCC start-up time
Over Current	OCPS [1:0]	Yes	Yes	Yes	Yes	ON	(1)	ON	H	**[Latch Off]** EN=L or execute MRRST=FFh command **[Auto Recover]** EN=L or after recovery time **[Report]** EN=L or motor current is down	EN=H (Normal mode)
FET Short	FSPS [1:0]	Yes	Yes	Yes	Yes	ON	(1)	ON	H	**[Latch Off]** EN=L or execute MRRST=FFh command **[Auto Recover]** EN=L or after recovery time **[Report]** EN=L or FET short current is down	EN=H (Normal mode)
Thermal Warning	THWPS	Yes	Yes	No	No	ON	ON	ON	H	Temperature is down	After OTP download
Thermal Shut Down	THSPS	Yes	No	Yes	No	(2)	(2)	(2)	(3)	Temperature is down	After OTP download
Watch Dog Timer	WDTPS	Yes	No	Yes	No	ON	(2)	ON	(4)	After output reset pulse from VMCRES pin	VMCRES =H

(1) Report or Ignore=ON, Latch Off or Auto Recover=OFF
(2) Ignore=ON, Auto Recover=OFF
(3) Ignore=H, Auto Recover=L
(4) Ignore=Fixed H, Auto Recover=Output L pulse

- Ignore:
  - DIAGS flag of GSDAT and MRDIAG0,1 flag are set.
- Report:
  - DIAGS flag of GSDAT and MRDIAG0,1 flag are set.
  - DIAG output is on. DIAG output is reset by recovery condition. (Not reset by MRDAIG0,1 read)
- Auto Recover:
  - DIAGS flag of GSDAT and MRDIAG0,1 flag are set.
  - DIAG output is on. Driver output is off. DIAG and driver output is reset by recovery condition. (Not reset by MRDAIG0,1 read)
- Latch Off:
  - DIAGS flag of GSDAT and MRDIAG0,1 flag are set.
  - DIAG output is on. Driver output is off. DIAG and Driver output is reset by EN=L or MRRST command. (Not reset by MRDAIG0,1 read)

DFCSEL (MRCONF0[4]):
DFCSEL=0: If error was cleared, DIAGS flag of GSDAT and MRDIAG0,1 flag are reset by MRDIAG0,1 read.
DFCSEL=1: DIAGS flag of GSDAT and MRDIAG0,1 flag are reset by recovery condition.

SPI Interface

In the LV89031 the SPI Interface is used to perform general communications for status reporting, control and programming.

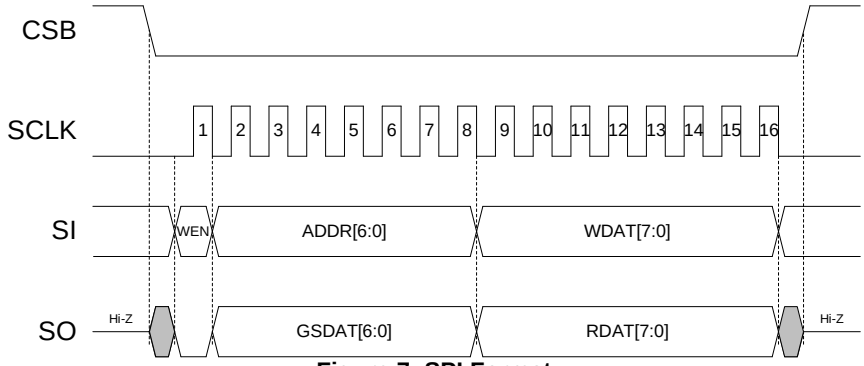


Figure 7: SPI Format

SPI communications with the LV89031 follows established industry standard practices including the use of WEN and start and stop bits as shown above. Data is transferred MSB first and both clock and data are transferred as 'true' data with the higher level indicating a logical 1 or true state.

There are two items to be especially careful of with the general communication scheme:

- Communications must be full duplex and simultaneous. It is not allowed to send one transaction and then read data on a second transaction as the status register information will be updated on the first transaction and then be out of date for the second. Some systems break transactions into separate read and write operations which is not acceptable.
- It is important the system master have the clock and data polarities and phases as shown above. Both the clock and data on some systems can be inverted for various reasons but must arrive at the LV89031 per the above drawing. Common errors include SCLK inversion such that the leading edge arrives as a downward transition rather than a rising edge, or having the data to clock phase incorrect. Data phase must be such that the data only changes during a clock falling edge and is completely stable during a clock rising edge. This means a good margin of one half a bit time exists to eliminate transmission delay hazards.

The first byte returned on all transactions is always the status register GSDAT, and contains information such as the busy flag during programming operations.

GSDAT[7:0]								
Bit 7	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**	
0	ORBEN	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]		
						0	0	Sleep mode
						0	1	Device start up time
						1	0	Standby mode
						1	1	Normal mode
	0	0	0	0	0			Normal Operation
					1			OTP download of default values
				1				Latched shutdown condition
			1					Failure Condition
		1						Last SPI access failed*
	1							OTP integrity test mode

The following SPI failures are detectable and reported collectively by a high on SECF in GSDAT[5] as general SPI failures:

- Any access to an address which is not assigned.
- The number of SCLK edges is not 16 within one word transfer.
- Any access to MRCONF, MRACS, ORCONF, ORACS while OBSY=1,(During write operations)
- Write access to MRODL register while OBSY=1, (during write operations.)
- Write access to any of the main registers after setting MSAENB=1 (Implies MRxxxx registers are locked).
- Write access to any of the OTP registers after OSAENB=1 (Implies ORxxxx registers are locked). .
- Write access attempt to a read only or locked register.
- SI signal changed at positive edge of SCLK. (Incorrect data/sclk phase setup)
- Write access to dead-time register FDTI while FDTIBSY is still high (last value has not been uploaded).

SPI Timing

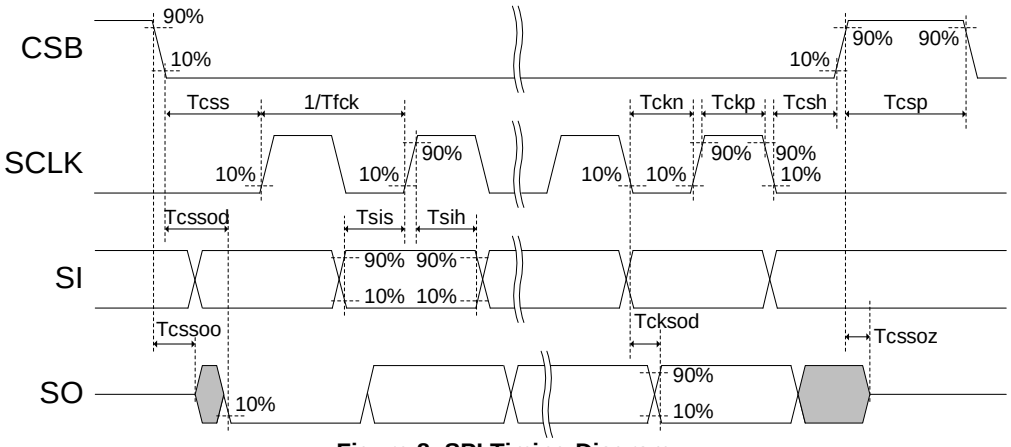


Figure 8: SPI Timing Diagram

Tj=-40 to 150°C, VS=4.5 to 40V, SO load=50pF

Symbol	Comment	Min	Typ	Max	Unit
Tfck	SCLK clock frequency			4.5	MHz
Tckp	SCLK high pulse width	90			ns
Tckn	SCLK low pulse width	90			ns
Tcss	CSB setup time	90			ns
Tcsh	CSB hold time	0			ns
Tcsp	CSB high pulse width	90			ns
Tsis	SI setup time	45			ns
Tsih	SI hold time	45			ns
Tcksod	SCLK fall edge to SO delay time			75	ns
Tcssod	CSB fall edge to SO delay time			75	ns

Tcssoo	CSB fall edge to SO data out time	0			ns
Tcssoz	CSB rise edge to SO Hi-Z out time			75	ns

SPI-Interface can be used after the data download of the OTP has been completed.

OTP Programming

….

REGISTER MAP

WENB	WTIM	ADDR[6:0]	OADR[2:0]	OTPDO[79:0]	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Always NG	Always NG	-	-	-	GSDAT	0	ORBEN	SACF	DIAGS	LATCH	OBSY	SMOD[1:0]	
OSAENB (*1)	EN=L	00h	0d	[7:0]	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
		01h	1d	[15:8]	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	
		02h	2d	[23:16]	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
Read Only	Read Only	03h	3d	[31:24]	MRCONF3	0	0	0	0	0	0	0	OSAENB
MSAENB (*1)	EN=L	04h	-	-	MRCONF4	0	WDTWT[2:0]			0	CSOFEN	AWODLEN	D3MDEN
		05h	-	-	MRCONF5	0	0	OCDL[1:0]		OCMASK[3:0]			
		06h	-	-	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	
		07h	-	-	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			
Always OK		08h	-	-	MRCONF8	0	0	0	0	0	0	0	MSAENB
Always OK	Always OK	10h	-	-	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0](Default=7h)		
		11h	-	-	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	
		12h	-	-	MRFSDL	0	0	0	0	FSDL[3:0]			
		13h	-	-	MRFDTI	0	0	0	0	FDTI[3:0]			
		14h	-	-	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY
		15h	-	-	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							
	EN=L	16h	-	-	MRORB	0	0	0	0	0	0	ORBEN	ORBLV
		17h	-	-	MRODL	Write 00h: Execute OTP data download							
Read Only	Read Only	20h	-	-	MRDIAG0	0	0	0	WDTPO	THSPO	THWPO	FSPO	OCPO
		21h	-	-	MRDIAG1	0	0	0	VCUVPO	VGUVPO	VDOVPO	VSOVPO	VSUVPO
		22h	-	-	MRACK	0	1	0	1	0	1	0	1
OSAENB (*1)	EN=L	40h	0d	[7:0]	ORCONF0	ORCONF0[7:6]		THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
		41h	1d	[15:8]	ORCONF1	ORCONF1[7:5]			WDTPS	THSPS	THWPS	VGUVPS[1:0]	
		42h	2d	[23:16]	ORCONF2	ORCONF2[7:6]		VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
		43h	3d	[31:24]	ORCONF3	ORCONF3[7:1]							OSAENB

Note: SPI access to addresses not listet here will result in an SPI access failure error (SACF).

MRCONF0 (Default: 00h)

Write access only when EN = Low. OTP backup possible.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h	MRCONF0	0	0	THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL

THTSEL

Temperature warning threshold and error selection.

THTSEL=0: Thermal warning=125°C, Thermal shut down=150°C
THTSEL=1: Thermal warning=150°C, Thermal shut down=175°C

DFCSEL

Defines the condition under which the error registers are reset, by error condition removed only, or by error condition removed and subsequent SPI read access of the register in question.

DFCSEL=0: If error was cleared, DIAGS flag of GSDAT and MRDIAG0,1 flag are reset by MRDIAG0,1 read.
DFCSEL=1: DIAGS flag of GSDAT and MRDIAG0,1 flag are reset by recovery condition.

DIAGLTO

If this bit is set, only latched errors result in a transition on DIAG. Otherwise all errors (and warnings) will be flagged.

DIAGLTO=0: At the time of detecting auto recover or latch off error, DIAG output is on
DIAGLTO=1: At the time of detecting latch off error, DIAG output is on

DIAGPOL

Decides the polarity of the DIAG output.

DIAGPOL=0: At the time of detecting diagnostic error, DIAG output is L
DIAGPOL=1: At the time of detecting diagnostic error, DIAG output is H

VGVSEL

Selects if the IC is in logic level mode or normal mode which modifies the gate voltage of the drive section.

VGVSEL=0: VG normal mode (VG=11V)
VGVSEL=1: VG logic level mode (VG=6V)

VCVSEL
Selects the output voltage of VCC to be either 3.3V or 5V.

VCVSEL=0: VCC=3.3V
VCVSEL=1: VCC=5.0V

MRCONF1 (Default: 00h)
Write access only when EN = Low. OTP backup possible.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
01h	MRCONF1	0	0	0	WDTPS	THSPS	THWPS	VGUVPS[1:0]	

WDTPS
Watchdog error results in error response or is ignored.

WDTPS=0: Ignore WDT error
WDTPS=1: Emergency off and report a WDT error (Auto recover)

THSPS
Thermal shutdown error results in error response or is ignored.

THSPS=0: Ignore thermal shut down error
THSPS=1: Emergency off and report at thermal shut down error (Auto recover)

THWPS
THWPS=0: Ignore thermal warning error
THWPS=1: Report thermal warning error

VGUVPS[1:0]
VGUVPS[1:0]=0h: Ignore VG under voltage error
VGUVPS[1:0]=1h: Report VG under voltage error
VGUVPS[1:0]=2h, 3h: Emergency off and report at VG under voltage error (Auto recover)

MRCONF2 (Default: 00h)
Write access only when EN = Low. OTP backup possible.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
02h	MRCONF2	0	0	VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	

VDOVPS[1:0]
VDOVPS[1:0]=0h: Ignore VDH over voltage error
VDOVPS[1:0]=1h: Report VDH over voltage error
VDOVPS[1:0]=2h, 3h: Emergency off and report at VDH over voltage error (Auto recover)

VSOVPS[1:0]
VSOVPS[1:0]=0h: Ignore VS over voltage error
VSOVPS[1:0]=1h: Report VS over voltage error
VSOVPS[1:0]=2h, 3h: Emergency off and report at VS over voltage error (Auto recover)

VSUVPS[1:0]
VSUVPS[1:0]=0h: Ignore VS under voltage error
VSUVPS[1:0]=1h: Report VS under voltage error
VSUVPS[1:0]=2h, 3h: Emergency off and report at VS under voltage error (Auto recover)

MRCONF3 (Default: 00h)
Read Only

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
03h	MRCONF3	0	0	0	0	0	0	0	OSAENB

OSAENB
Setting this bit disables all write access to the configuration registersMRCONF0, MRCONF1 and MRCONF2 and the OTP backup register. Set to prevent system parameters from being modified.

OSAENB=0: Enable write access of MRCONF0~2 and ORCONF0~3
OSAENB=1: Disable write access of MRCONF0~2 and ORCONF0~3

MRCONF4 (Default: 00h)
Write access only when EN = Low.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
04h	MRCONF4	0	WDTWT[2:0]			0	CSOFEN	AWODLEN	D3MDEN

WDTWT[2:0]
Defines the watchdog timer window sizes.

WDTWT[2:0]=0h: Tfow=409.6ms, Tcw=102.4ms, Twt=204.8ms

WDTWT[2:0]=1h: Tfow=204.8ms, Tcw=51.2ms, Twt=102.4ms
:
: (1/2 step)
:
WDTWT[2:0]=7h: Tfow=3.2ms, Tcw=0.8ms, Twt=1.6ms

CSOFEN
Selects the offset of the current sense amplifier.

CSOFEN=0: Current sense amp offset=1.5V
CSOFEN=1: Current sense amp offset=0.2V

AWODLEN
Periodical (400ms) OTP download during EN=H.

AWODLEN=0: Not download OTP data in normal mode
AWODLEN=1: Download OTP data periodically in normal mode

D3MDEN
Chooses how the output drivers are addressed, with six PWM channels, or with three PWM channels and three enables.

D3MDEN=0: Drive 6 mode
D3MDEN=1: Drive 3 mode

MRCONF5 (Default: 00h)
Write access only when EN = Low.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
05h	MRCONF5	0	0	OCDL[1:0]		OCMASK[3:0]			

OCDL[1:0]
Defines the overcurrent detection threshold voltage between ISN and ISP.

OCDL[1:0]=0h: Over current detect level=200mV
OCDL[1:0]=1h: Over current detect level=150mV
OCDL[1:0]=2h, 3h: Over current detect level=100mV

OCMASK[3:0]
Masking time for the overcurrent detection after every output transition.

OCMASK[3:0]=0h: Over current mask time=0.2us
OCMASK[3:0]=1h: Over current mask time=0.4us
:
: (0.2us step)
:
OCMASK[3:0]=Eh: Over current mask time=3.0us
OCMASK[3:0]=Fh: Over current mask time=3.2us

MRCONF6 (Default: 00h)
Write access only when EN = Low.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
06h	MRCONF6	0	0	0	0	FSFT[1:0]		FSDT[1:0]	

FSFT[1:0]
External FET short circuit detection masking time, starts after turn-on of the FET.

FSFT[1:0]=0h: FET short masking time=0.8us
FSFT[1:0]=1h: FET short masking time=1.6us
FSFT[1:0]=2h: FET short masking time=2.4us
FSFT[1:0]=3h: FET short masking time=3.2us

FSDT[1:0]
External FET short detection debounce time. A short condition hast to remain valid during this time.

FSDT[1:0]=0h: FET short detect time=3.2us
FSDT[1:0]=1h: FET short detect time=6.4us
FSDT[1:0]=2h: FET short detect time=9.6us
FSDT[1:0]=3h: FET short detect time=12.8us

MRCONF7 (Default: 00h)
Write access only when EN = Low.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
07h	MRCONF7	FSPS[1:0]		OCPS[1:0]		FDTILIM[3:0]			

FSPS[1:0]
Short circuit error decision mask.

FSPS[1:0]=0h: Ignore FET short error
FSPS[1:0]=1h: Report FET short error
FSPS[1:0]=2h: Emergency off and report at FET short error (Auto recover)
FSPS[1:0]=3h: Emergency off and report at FET short error (Latched off)

OCPS[1:0]
Overcurrent error desicion mask.

OCPS[1:0]=0h: Ignore over current error
OCPS[1:0]=1h: Report over current error

OCPS[1:0]=2h: Emergency off and report at over current error (Auto recover)
OCPS[1:0]=3h: Emergency off and report at over current error (Latched off)

FDTILIM[3:0]
Minimum Dead time programming register.

FDTILIM[3:0]=0h: FET dead time=3.2us
FDTILIM[3:0]=1h: FET dead time=3.0us
:
: (-0.2us step)
:
FDTILIM[3:0]=Eh: FET dead time=0.4us
FDTILIM[3:0]=Fh: FET dead time=0.2us

MRCONF8 (Default: 00h)
Write access only when EN = Low.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
08h	MRCONF8	0	0	0	0	0	0	0	MSAENB

MSAENB
Setting this bit disables all write access to the configuration registers MRCONF4 to MRCONF7.

MSAENB=0: Enable write access of MRCONF4~7
MSAENB=1: Disable write access of MRCONF4~7

MRAOSEL (Default: 07h)
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
10h	MRAOSEL	0	0	0	0	0	AOUTSEL[2:0]		

AOUTSEL[2:0]
Select the internal nodes brought out on AOUT.

AOUTSEL[2:0]=0h: AOUT=Output VDH voltage level
AOUTSEL[2:0]=1h: AOUT=Output SH1 voltage level
AOUTSEL[2:0]=2h: AOUT=Output SH2 voltage level
AOUTSEL[2:0]=3h: AOUT=Output SH3 voltage level
AOUTSEL[2:0]=4h, 5h: AOUT=Output thermal monitor voltage level
AOUTSEL[2:0]=6h, 7h: AOUT=Hi-Z

MRCSG (Default: 00h)
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
11h	MRCSG	0	0	0	0	0	0	CSGAIN[1:0]	

CSGAIN[1:0]
Programs the gain of the current sense amplifier.

CSGAIN[1:0]=0h: Current sense amp gain=7.5
CSGAIN[1:0]=1h: Current sense amp gain=15
CSGAIN[1:0]=2h: Current sense amp gain=22.5
CSGAIN[1:0]=3h: Current sense amp gain=30

MRFSDL (Default: 00h)
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
12h	MRFSDL	0	0	0	0	FSDL[3:0]			

FSDL[3:0]
Defines the maximum allowable drain source voltage across a power FET.

FSDL[3:0]=0h: FET short detect level=100mV
FSDL[3:0]=1h: FET short detect level=200mV
:
: (100mV step)
:
FSDL[3:0]=Eh: FET short detect level=1500mV
FSDL[3:0]=Fh: FET short detect level=1600mV

MRFDTI (Default: 00h)
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
13h	MRFDTI	0	0	0	0	FDTI[3:0]			

FDTI[3:0]
Dead time programming register. This deadtime will be applied unless it is smaller than FDTILIM[3:0] in MRCONF7.

FDTI[3:0]=0h: FET dead time=3.2us
FDTI[3:0]=1h: FET dead time=3.0us
:
: (-0.2us step)
:
FDTI[3:0]=Eh: FET dead time=0.4us
FDTI[3:0]=Fh: FET dead time=0.2us

MRFDTIF (Default: 00h)
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
14h	MRFDTIF	0	0	0	0	0	0	0	FDTIBSY

FDTIBSY
FDTIBSY goes high after the dead-time register was written to via SPI but not uploaded into the dead-time counter. Upload happens at the beginning of every dead time measuring period (falling edge of a gate signal) and clears the FDTIBSY flag.

A write access MRFDTIF=01h also clears the FDTIBSY flag.

MRRST
Full dynamic access.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
15h	MRRST	Write 00h: Reset WDT / Write FFh: Reset latch off							

MRRST[7:0]
Write acces to this register resets the Watchdog or the Error latch.

Write MRRST[7:0]=00h: Reset WDT
Write MRRST[7:0]=FFh: Reset latch off

MRORB (Default: 00h)
Register for OTP programming integrity check. Write during EN=Low only.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
16h	MRORB	0	0	0	0	0	0	ORBEN	ORBLV

ORBEN
Setting this bit puts the device into OTP integrity check mode.

ORBEN=0: Normal
ORBEN=1: OTP bias read mode

Changes the OTP readout thresholds to high and low, to verify data integrity.

ORBLV=0: OTP low bias read mode at ORBEN=1
ORBLV=1: OTP high bias read mode at ORBEN=1

ORBLV

MRODL
Write access during EN=Low only.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
17h	MRODL	Write 00h: Execute OTP data download							

MRODL[7:0]
A write initiates an OTP data download into the main registers in standby mode. This is usally blocked but can be enabled by setting AWODLEN.

Write MRODL[7:0]=00h: Execute OTP data download

MRDIAG0
Read Only.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
20h	MRDIAG0	0	0	0	WDTPO	THSPO	THWPO	FSPO	OCPO

WDTPO
Watchdog error flag.

WDTPO=0: Normal
WDTPO=1: Detect WDT error

THSPO
Overtemperature shutoff flag.

THSPO=0: Normal
THSPO=1: Detect thermal shut down error

THWPO
Thermal warning flag.

THWPO=0: Normal
THWPO=1: Detect thermal warning error

OCPO
Overcurrent error flag.

OCPO=0: Normal
OCPO=1: Detect over current error

FSPO
FET short circuit detection flag.

FSPO=0: Normal
FSPO=1: Detect FET short error

MRDIAG1
Read Only.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
21h	MRDIAG1	0	0	0	VCUVPO	VGUVPO	VDOVPO	VSOVPO	VSUVPO

VCUVPO
VCC undervoltage flag.

VCUVPO=0: Normal
VCUVPO=1: Detect VCC under voltage error

VGUVPO
VG undervoltage flag.

VGUVPO=0: Normal
VGUVPO=1: Detect VG under voltage error

VDOVPO
VDH overvoltage flag.

VDOVPO=0: Normal
VDOVPO=1: Detect VDH over voltage error

VSOVPO
VS overvoltage flag.

VSOVPO=0: Normal
VSOVPO=1: Detect VS over voltage error

VSUVPO
VS undervoltage flag.

VSUVPO=0: Normal
VSUVPO=1: Detect VS under voltage error

MRACK
Read Only.

ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
22h	MRACK	0	1	0	1	0	1	0	1

MRACK[7:0]
For SPI data verification. A read must result in 55h.

MRACK[7:0] read data is fixed 55h

ORCONF0~3 (Default: 00h)
OTP backup for critical system registers. Programmable during EN=L only.

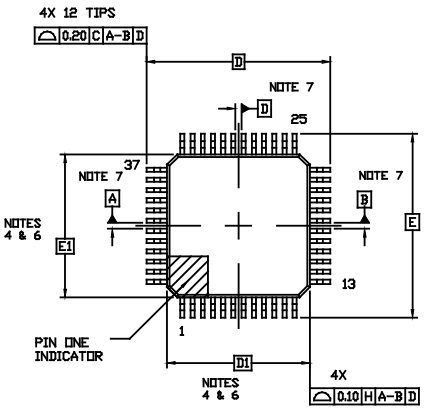
ADDR	Data Name	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
40h	ORCONF0	ORCONF0[7:6]		THTSEL	DFCSEL	DIAGLTO	DIAGPOL	VGVSEL	VCVSEL
41h	ORCONF1	ORCONF1[7:5]			WDTPS	THSPS	THWPS	VGUVPS[1:0]	
42h	ORCONF2	ORCONF2[7:6]		VDOVPS[1:0]		VSOVPS[1:0]		VSUVPS[1:0]	
43h	ORCONF3	ORCONF3[7:1]							OSAENB

ORCONF0~3
ORCONF0~3 data is transferred to MRCONF0~3 at OTP data download

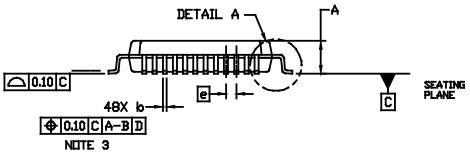
(ORCONF0[7:6], ORCONF1[7:5], ORCONF2[7:6], ORCONF3[7:1] data is not transferred to MRCONF)

PACKAGE DIMENSIONS

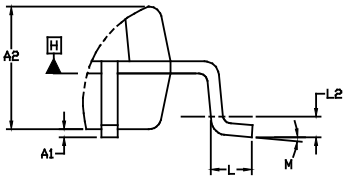
SPQFP48 7x7 / SQFP48K
CASE 131AN
ISSUE A



TOP VIEW



SIDE VIEW

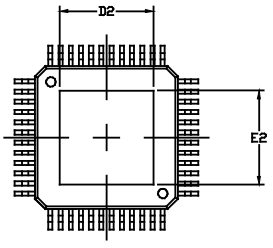


DETAIL A

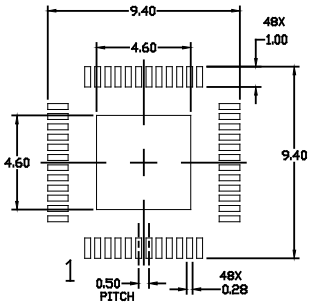
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DATUMS A-B AND D ARE DETERMINED AT DATUM PLANE H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.

	MILLIMETERS	
DIM	MIN.	MAX.
A	---	1.70
A1	0.00	0.15
A2	1.50 REF	
b	0.15	0.26
D	9.00 BSC	
D1	7.00 BSC	
D2	4.60 REF	
E	9.00 BSC	
E1	7.00 BSC	
E2	4.60 REF	
e	0.50 BSC	
L	0.30	0.70
L2	0.25 BSC	
M	0°	10°



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT