MC74LVX257

Quad 2-Channel Multiplexer with 3-State Outputs

The MC74LVX257 is an advanced high speed CMOS quad 2–channel multiplexer fabricated with silicon gate CMOS technology.

It consists of four 2–input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: t_{PD} = 4.5 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: FETs = 100; Equivalent Gates = 25
- ESD Performance:
    Human Body Model > 2000 V;
    Machine Model > 200 V
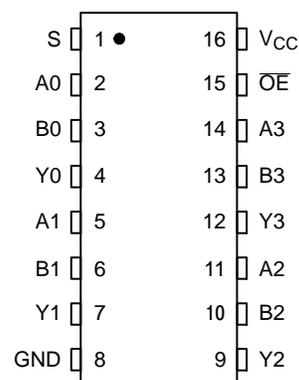- These Devices are Pb–Free and are RoHS Compliant

PIN ASSIGNMENT

S	1 ●	16	V_{CC}
A0	2	15	$\overline{OE}$
B0	3	14	A3
Y0	4	13	B3
A1	5	12	Y3
B1	6	11	A2
Y1	7	10	B2
GND	8	9	Y2

MARKING DIAGRAMS

```
16
LVX257G
o  AWLYWW
1
```
SOIC−16

```
16
LVX
257
ALYW▪
o      ▪
1
```
TSSOP−16
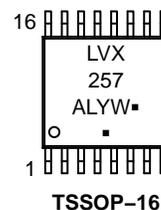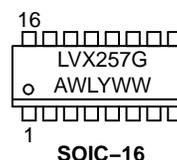
LVX257 = Specific Device Code
A   = Assembly Location
WL, L   = Wafer Lot
Y   = Year
WW, W   = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.
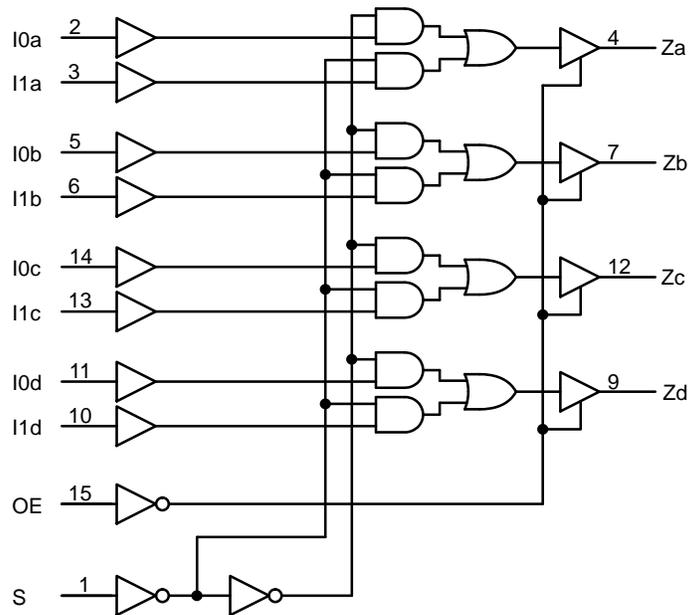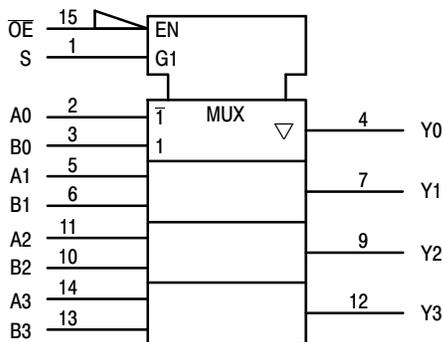
MC74LVX257

Figure 1. Expanded Logic Diagram

Figure 2. IEC Logic Symbol

FUNCTION TABLE

Inputs		Outputs
$\overline{OE}$	S	Y0 – Y3
H	X	Z
L	L	A0 – A3
L	H	B0 – B3

A0 – A3, B0 – B3 = the levels
of the respective Data–Word
Inputs.

ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX257DG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74LVX257DR2G	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74LVX257DTG	TSSOP–16 (Pb–Free)	96 Units / Rail
MC74LVX257DTR2G	TSSOP–16 (Pb–Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	Digital Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} +0.5	V
I_{IK}	Input Diode Current		−20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
P_D	Power Dissipation in Still Air	SOIC Package TSSOP	200 180	mW
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 > 2000	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 4)	±300	mA
θ_{JA}	Thermal Resistance, Junction−to−Ambient	SOIC Package TSSOP	143 164	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature Range, all Package Types		−40	85	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 3.3 V ± 0.3 V	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 3.6	0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC} 0.7 V_{CC}		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 3.6			0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC} 0.3 V_{CC}	V
V_{OH}	High–Level Output Voltage	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low–Level Output Voltage	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0	0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{OZ}	Maximum 3–State Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	3.6			±0.1		±1.0	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_{IN} = V_{CC} or GND	3.6	1.0	1.0	2.0		40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions		T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A or B to Y	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF		6.5 9.5	10.0 14.0	1.0 1.0	15.0 18.5	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF		4.5 7.5	8.0 12.0	1.0 1.0	10.0 13.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, S to Y	V_{CC} = 2.7 V	C_L = 15pF C_L = 50pF		8.0 10.5	12.0 15.5	1.0 1.0	17.0 20.0	ns
		V_{CC} = 3.3 V ± 0.3 V	C_L = 15pF C_L = 50pF		6.0 8.5	10.0 13.5	1.0 1.0	12.0 15.5	
t_{PZL}, t_{PZH}	Maximum Output Enable, Time, $\overline{OE}$ to Y	V_{CC} = 2.7 V R_L = 1 kΩ	C_L = 15pF C_L = 50pF		7.5 10.5	11.5 15.0	1.0 1.0	16.5 18.0	ns
		V_{CC} = 3.3 V ± 0.3 V R_L = 1 kΩ	C_L = 15pF C_L = 50pF		5.5 8.5	9.5 13.0	1.0 1.0	11.5 15.0	
t_{PLZ}, t_{PHZ}	Maximum Output Disable, Time, $\overline{OE}$ to Y	V_{CC} = 2.7 R_L = 1 kΩ	C_L = 50pF		13.0	17.0	1.0	18.0	ns
		V_{CC} = 3.3 V ± 0.3 V R_L = 1 kΩ	C_L = 50pF		12	17.0	1.0	18.0	
C_{IN}	Maximum Input Capacitance				4	10		10	pF
			Typical @ 25°C, V_{CC} = 3.3 V						
C_{PD}	Power Dissipation Capacitance (Note 5)		20						pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = $C_{PD} \cdot V_{CC} \cdot f_{in}$ + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption; P_D = $C_{PD} \cdot V_{CC}^2 \cdot f_{in}$ + $I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V)

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.3	−0.5	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V
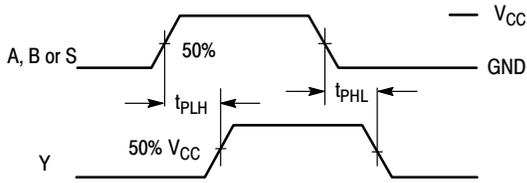
Figure 3. Switching Waveform
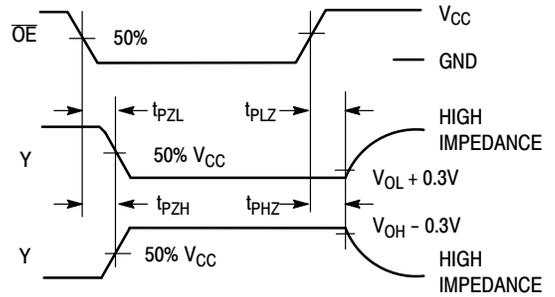
Figure 4. Switching Waveform
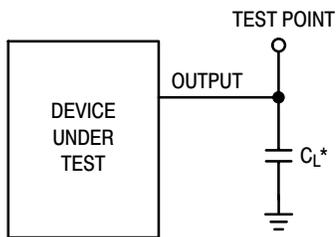
*Includes all probe and jig capacitance

Figure 5. Test Circuit

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}. CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
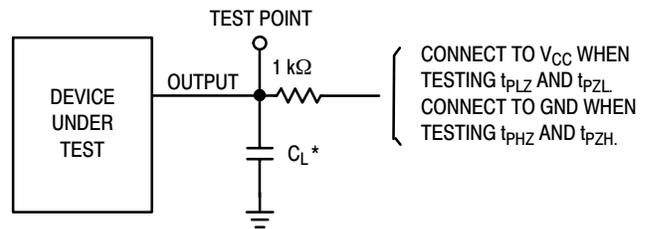
*Includes all probe and jig capacitance

Figure 6. Test Circuit
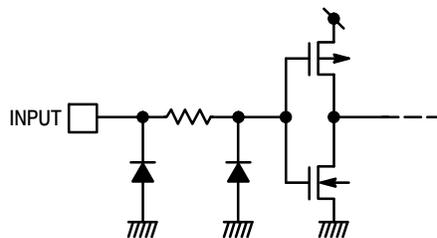
Figure 7. Input Equivalent Circuit

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PACKAGE DIMENSIONS

TSSOP–16
CASE 948F
ISSUE B
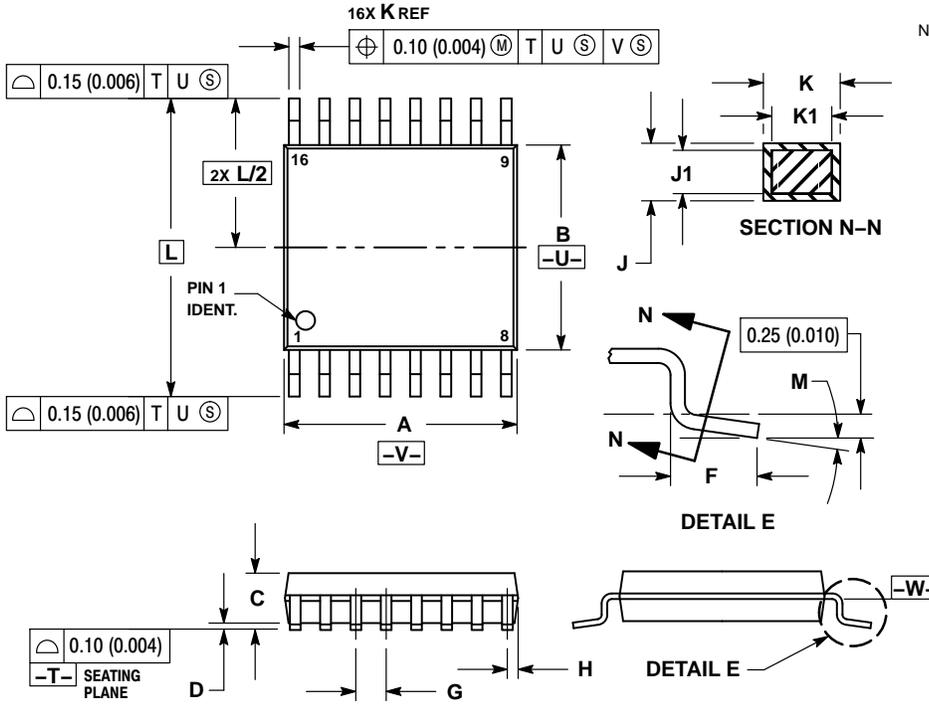
16X K REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

2X L/2

L

16 ... **9**

B
–U–

PIN 1
IDENT.

1 ... **8**

△ | 0.15 (0.006) | T | U Ⓢ

A
–V–

K
K1

J1

SECTION N–N

N

0.25 (0.010)

M

N

F

DETAIL E

C

△ | 0.10 (0.004)
–T– SEATING
PLANE

D

G

H

DETAIL E

–W–

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*
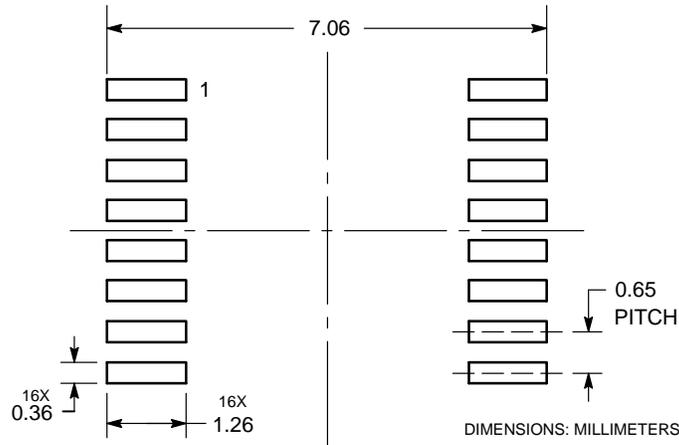
7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOIC–16
CASE 751B–05
ISSUE K
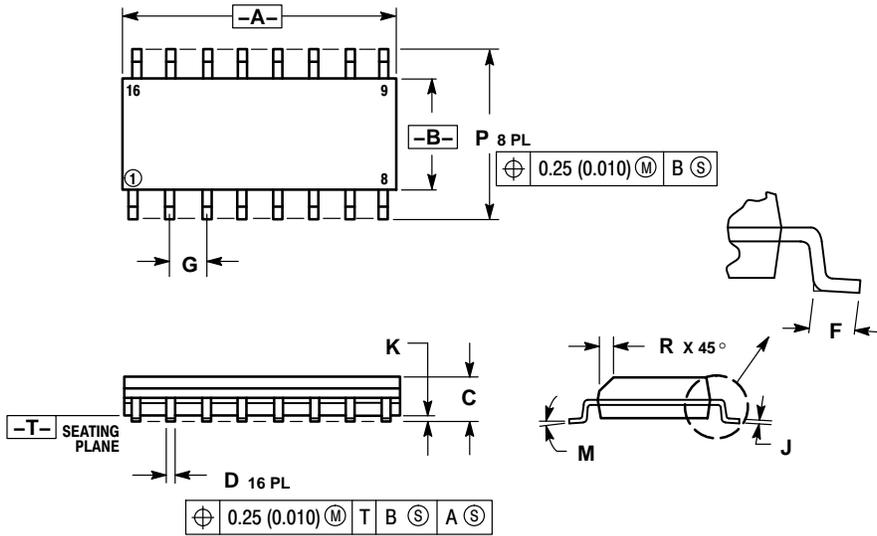
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

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MC74LVX257/D