MC74LVX595

Product Preview

8-Bit Shift Register with Output Storage Register (3-State)

The MC74LVX595 is an advanced high speed 8−bit shift register with an output storage register fabricated with silicon gate CMOS technology.

The MC74LVX595 contains an 8−bit static shift register which feeds an 8−bit storage register.

Shift operation is accomplished on the positive going transition of the Shift Clock input (SCK). The output register is loaded with the contents of the shift register on the positive going transition of the Register Clock input (RCK). Since the RCK and SCK signals are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3−state, the LVX595 can be directly connected to an 8−bit bus. This register can be used in serial−to−parallel conversion, data receivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

- High Speed: f_{max} = 100 MHz (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 1.0 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V

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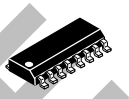
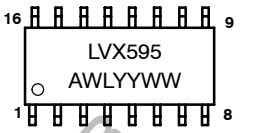
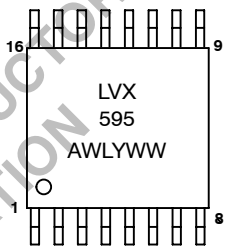
MARKING DIAGRAMS

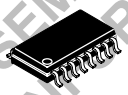


SOIC−16
D SUFFIX
CASE 751B

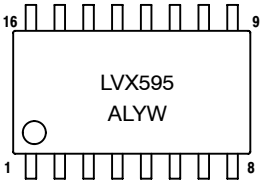


TSSOP−16
DT SUFFIX
CASE 948F





SOIC EIAJ−16
M SUFFIX
CASE 966



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74LVX595M	SO EIAJ−16	48 Units/Rail
MC74LVX595MEL	SO EIAJ−16	2000 Units/Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset ($\overline{SCLR}$)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable ($\overline{OE}$)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D→SR_A; SR_N→SR_{N+1}	U	SR_G→SR_H	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	SR_N→STR_N	*	SR_N
Storage register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents D = data (L, H) logic level ↓ = High–to–Low * = depends on Reset and Shift Clock inputs
STR = storage register contents U = remains unchanged ↑ = Low–to–High ** = depends on Register Clock input

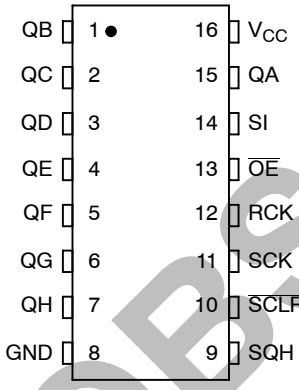


Figure 1. Pin Assignment

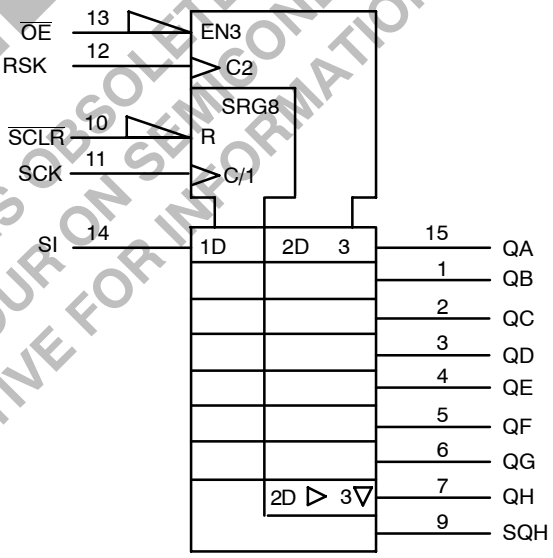


Figure 2. IEC Logic Symbol

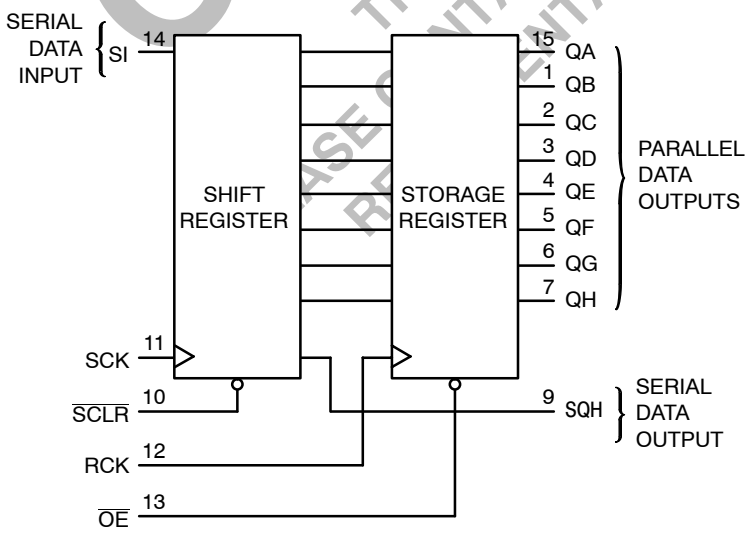


Figure 3. Logic Diagram

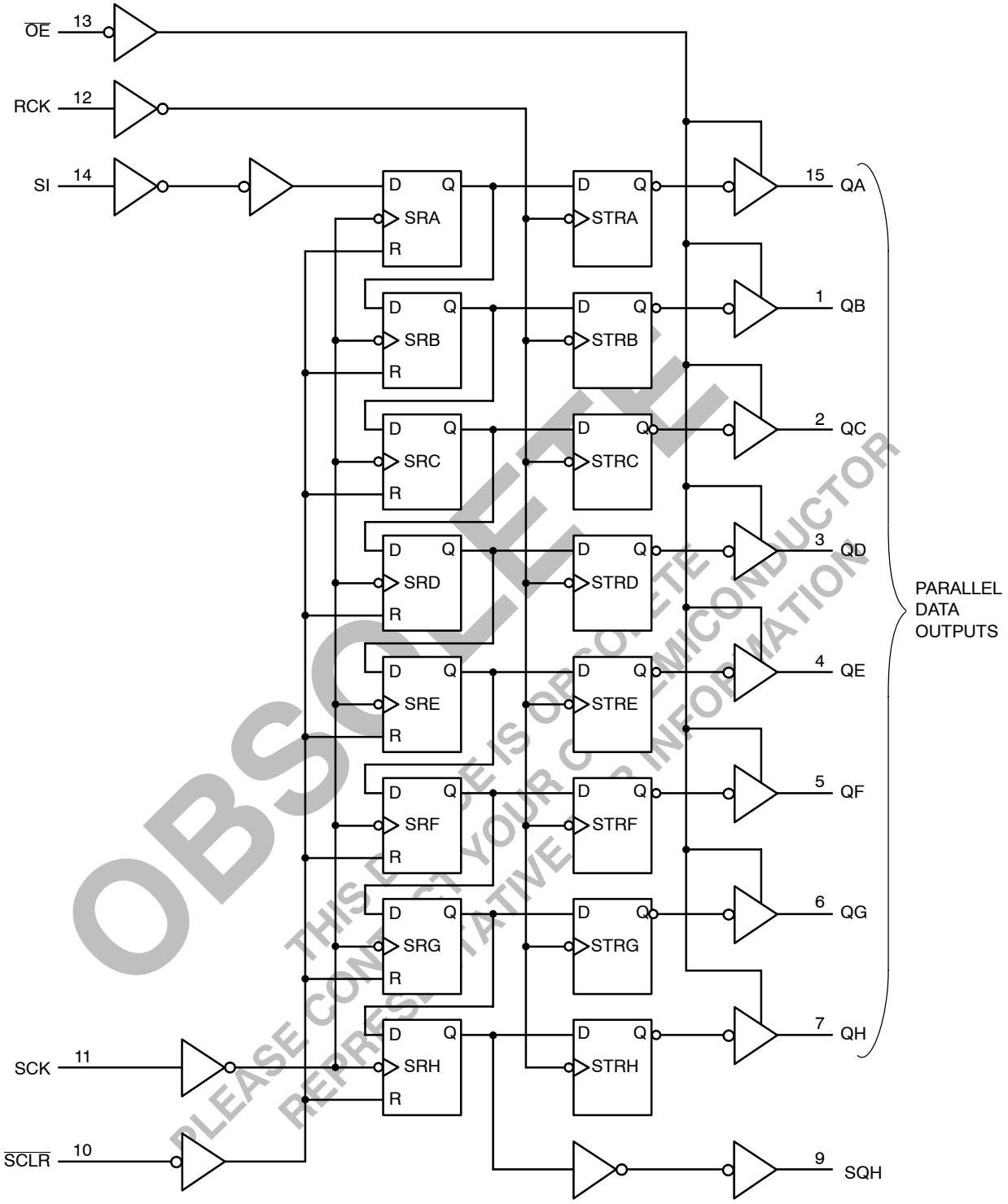


Figure 4. Expanded Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to + 7.0	V
V_{in}	DC Input Voltage	−0.5 to + 7.0	V
V_{out}	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	−20	mA
I_{OK}	Output Diode Current	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	200 180	mW
T_{stg}	Storage Temperature	−65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute−maximum−rated conditions is not implied.

†Derating — SOIC Packages: − 7.0 mW/°C from 65° to 125°C
— TSSOP Package: − 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{IN}	DC Input Voltage	0.0	5.5	V
V_{OUT}	DC Output Voltage	0.0	V_{CC}	V
T_A	Operating Temperature Range	−55	+85	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3 V ± 0.3 V	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.1 2.4			1.5 2.1 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage (V_{IN}= V_{IH} or V_{IL})	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage (V_{IN}= V_{IH} or V_{IL})	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{OZ}	3−State Output Off−State Current	V_{IN}= V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	3.6			±0.25		±2.5	μA
I_{IN}	Input Leakage Current	V_{in} = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \le 85°C$ Min	$T_A \le 85°C$ Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 2.7 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF	90 60	130 110		80 50		MHz
		V_{CC} = 3.3 V ± 0.3 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF	100 75	150 130		100 90		
t_{PLH}, t_{PHL}	Propagation Delay, SCK to SQH	V_{CC} = 2.7 V C_L = 15 pF C_L = 50 pF		11.0 13.5	14.0 17.5	1.0 1.0	16.0 19.5	ns
		V_{CC} = 3.3 V ± 0.3 V C_L = 15 pF C_L = 50 pF		8.8 11.3	12.0 15.5	1.0 1.0	13.5 17.0	
t_{PHL}	Propagation Delay, $\overline{CPLR}$ to SQH	V_{CC} = 2.7 V C_L = 15 pF C_L = 50 pF		10.0 13.0	14.0 17.5	1.0 1.0	16.0 19.5	ns
		V_{CC} = 3.3 V ± 0.3 V C_L = 15 pF C_L = 50 pF		8.4 10.9	12.0 15.5	1.0 1.0	13.5 17.0	
t_{PLH}, t_{PHL}	Propagation Delay, RCK to QA−QH	V_{CC} = 2.7 V C_L = 15 pF C_L = 50 pF		9.5 12.0	13.0 16.5	1.0 1.0	15.0 18.5	ns
		V_{CC} = 3.3 V ± 0.3 V C_L = 15 pF C_L = 50 pF		7.7 10.2	11.0 14.5	1.0 1.0	12.5 16.0	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to QA−QH	V_{CC} = 2.7 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		9.5 11.0	12.5 17.0	1.0 1.0	14.5 19.0	ns
		V_{CC} = 3.3 V ± 0.3 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		7.5 9.0	10.5 14.0	1.0 1.0	12.0 15.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to QA−QH	V_{CC} = 2.7 V C_L = 50 pF R_L = 1 kΩ		14.0	17.0	1.0	19.0	ns
		V_{CC} = 3.3 V ± 0.3 V C_L = 50 pF R_L = 1 kΩ		12.0	15.0	1.0	16.5	
C_{IN}	Input Capacitance			4	10		10	pF
C_{OUT}	Three−State Output Capacitance (Output in High−Impedance State), QA−QH			6			10	pF

		Typical @ 25°C, V_{CC} = 3.3 V	
C_{PD}	Power Dissipation Capacitance (Note 1)	87	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V

Symbol	Characteristic	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	Unit
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.8	− 1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS Input $t_r = t_f = 3.0$ ns

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to 85°C	Unit
			Typ	Limit	Limit	
t_{su}	Setup Time, SI to SCK	V_{CC} = 2.7 V		3.5	3.5	ns
		V_{CC} = 3.3 V ± 0.3 V		3.0	3.0	
$t_{su(H)}$	Setup Time, SCK to RCK	V_{CC} = 2.7 V		9.0	9..5	ns
		V_{CC} = 3.3 V ± 0.3 V		7.0	7.5	
$t_{su(L)}$	Setup Time, $\overline{SCLR}$ to RCK	V_{CC} = 2.7 V		9.0	8.5	ns
		V_{CC} = 3.3 V ± 0.3 V		7.0	7.5	
t_h	Hold Time, SI to SCK	V_{CC} = 2.7 V		2.0	2.0	ns
		V_{CC} = 3.3 V ± 0.3 V		1.0	1.0	
$t_{h(L)}$	Hold Time, $\overline{SCLR}$ to RCK	V_{CC} = 2.7 V		0	0	ns
		V_{CC} = 3.3 V ± 0.3 V		0	0	
t_{rec}	Recovery Time, $\overline{SCLR}$ to SCK	V_{CC} = 2.7 V		2.5	2.5	ns
		V_{CC} = 3.3 V ± 0.3 V		2.0	2.0	
t_w	Pulse Width, SCK or RCK	V_{CC} = 2.7 V		4.0	4.0	ns
		V_{CC} = 3.3 V ± 0.3 V		4.0	4.0	
$t_{w(L)}$	Pulse Width, $\overline{SCLR}$	V_{CC} = 2.7 V		4.0	4.0	ns
		V_{CC} = 3.3 V ± 0.3 V		4.0	4.0	

SWITCHING WAVEFORMS

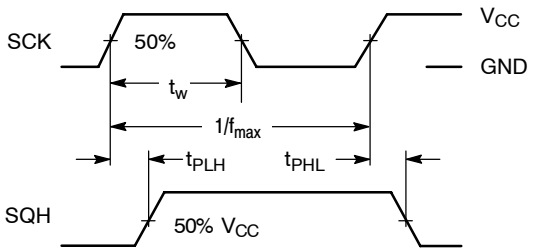


Figure 5.

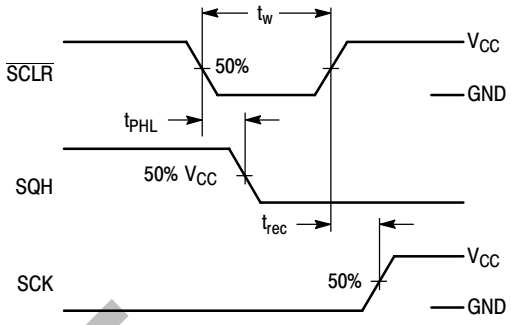
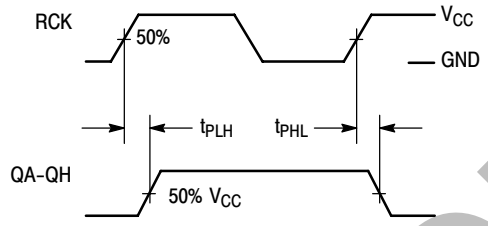


Figure 6.



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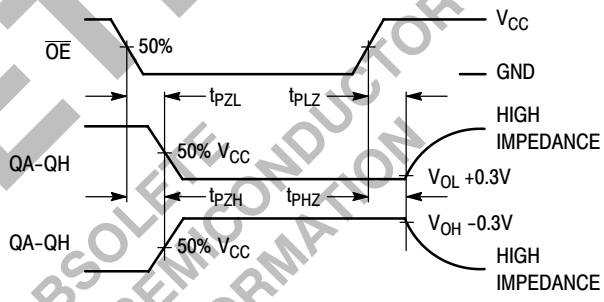


Figure 8.

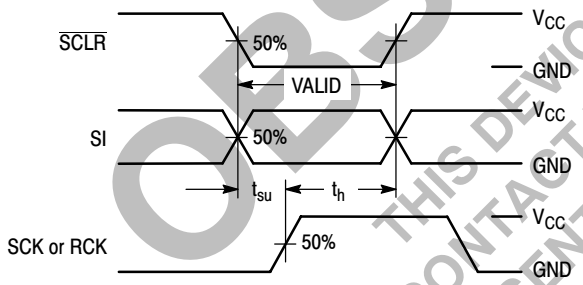


Figure 9.

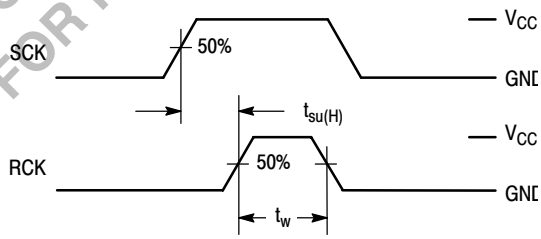
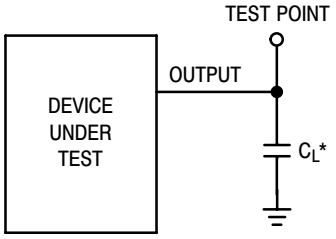


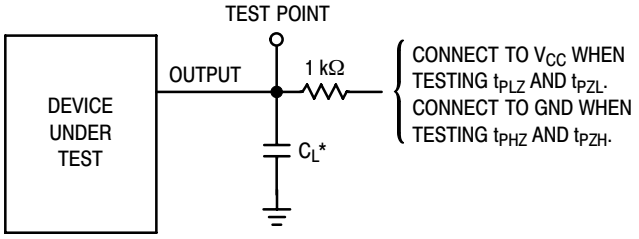
Figure 10.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 11.



*Includes all probe and jig capacitance

Figure 12.

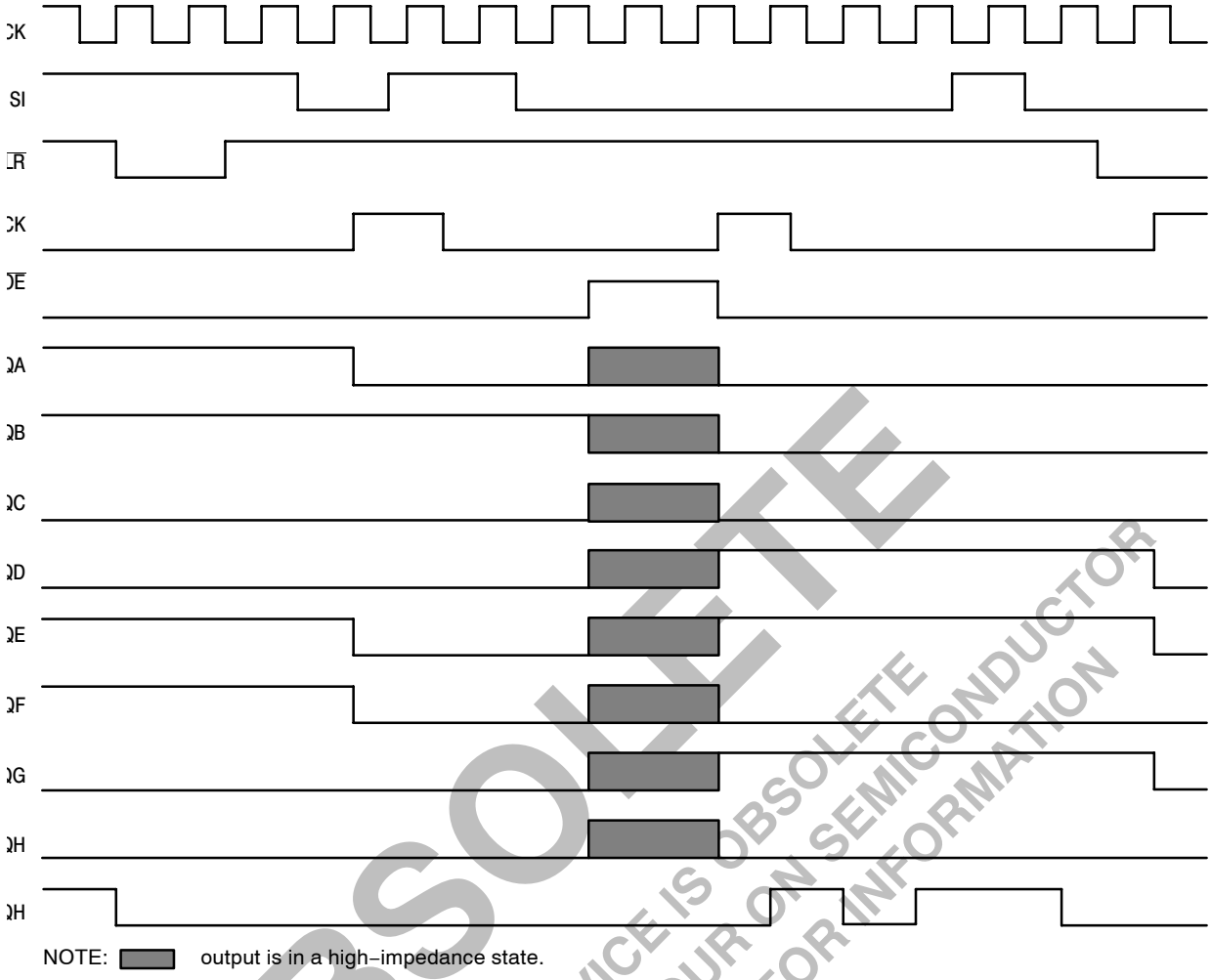


Figure 13. Timing Diagram

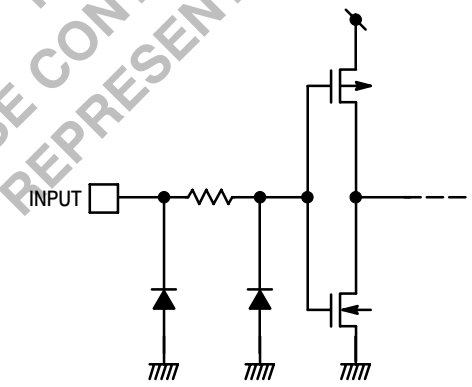
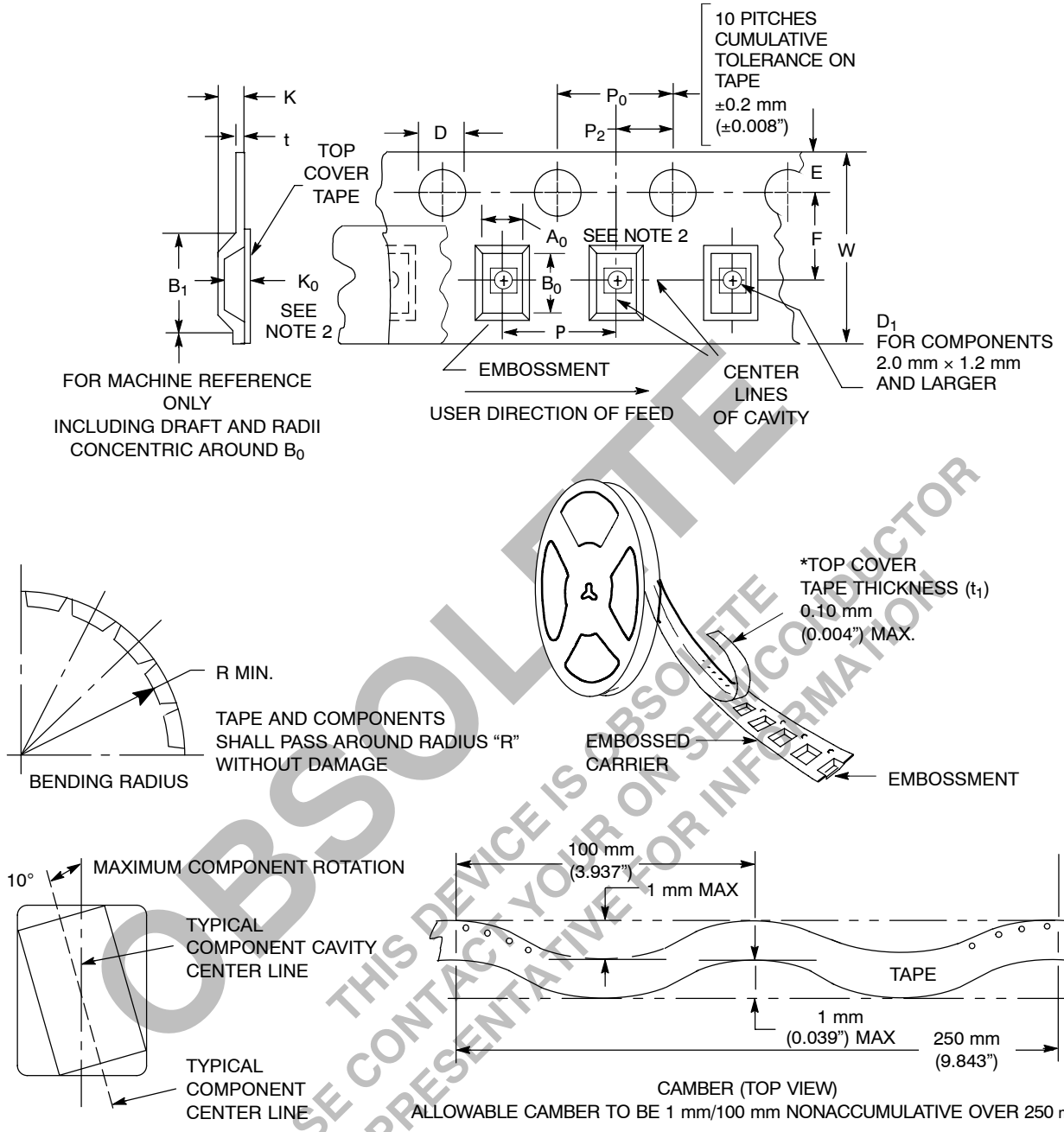


Figure 14. Input Equivalent Circuit



2. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

Figure 15. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 3 and 4)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 −0.0 (0.059" +0.004 −0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

3. Metric Dimensions Govern−English are in parentheses for reference only.
4. A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

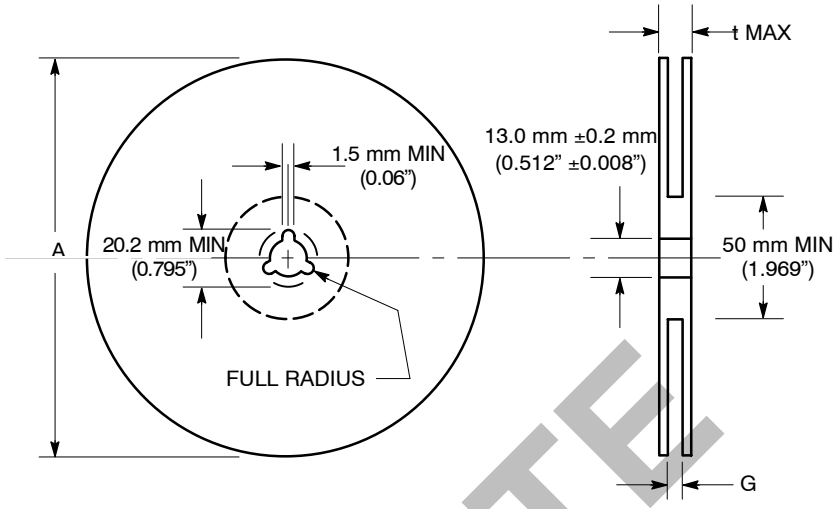


Figure 16. Reel Dimensions

REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, −0.0 (0.33" + 0.059", −0.00)	14.4 mm (0.56")
12 mm	R2	330 mm (13")	12.4 mm, +2.0 mm, −0.0 (0.49" + 0.079", −0.00)	18.4 mm (0.72")
16 mm	R2	360 mm (14.173")	16.4 mm, +2.0 mm, −0.0 (0.646" + 0.078", −0.00)	22.4 mm (0.882")
24 mm	R2	360 mm (14.173")	24.4 mm, +2.0 mm, −0.0 (0.961" + 0.078", −0.00)	30.4 mm (1.197")

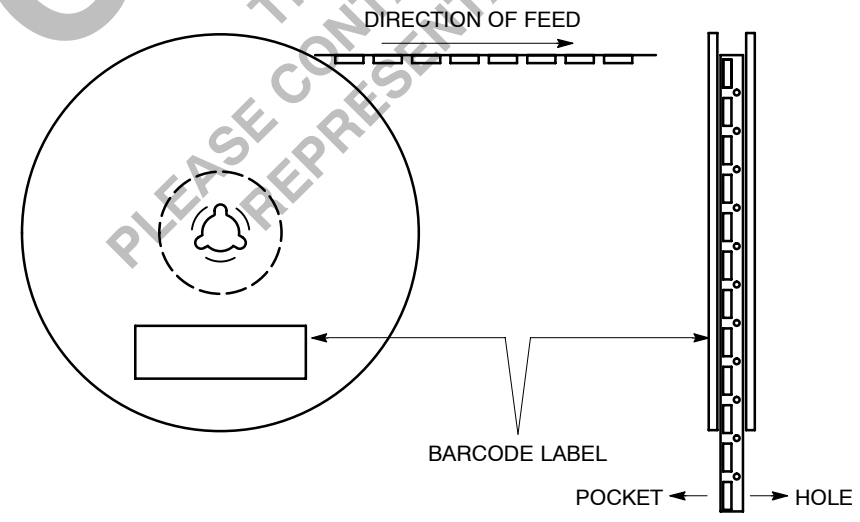


Figure 17. Reel Winding Direction

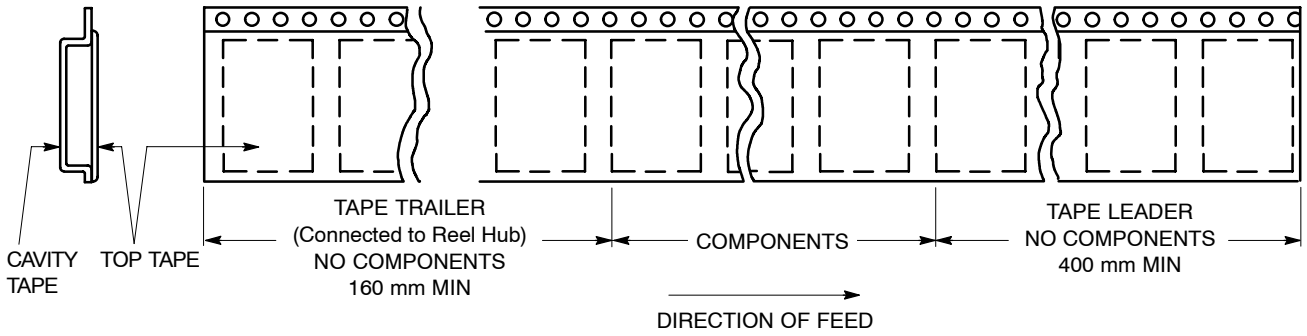


Figure 18. Tape Ends for Finished Goods

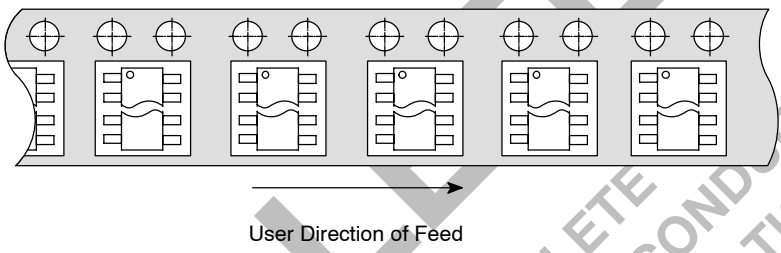


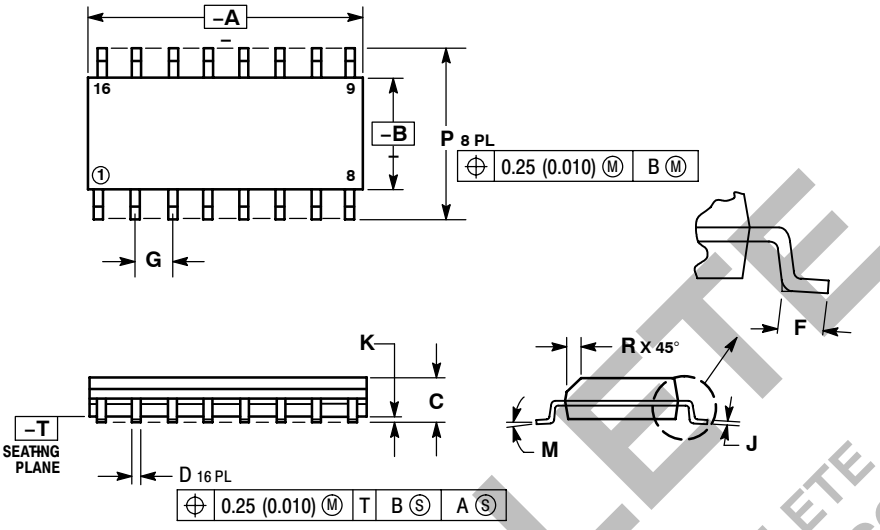
Figure 19. TSSOP and SOIC R2 Reel Configuration/Orientation

TAPE UTILIZATION BY PACKAGE

Tape Size	SOIC	TSSOP	QFN	SC88A / SOT−353 SC88/SOT−363
8 mm				5−, 6−Lead
12 mm	8−Lead	8−, 14−, 16−Lead	8−, 14−, 16−Lead	
16 mm	14−, 16−Lead	20−, 24−Lead	20−, 24−Lead	
24 mm	18−, 20−, 24−, 28−Lead	48−, 56−Lead	48−, 56−Lead	

PACKAGE DIMENSIONS

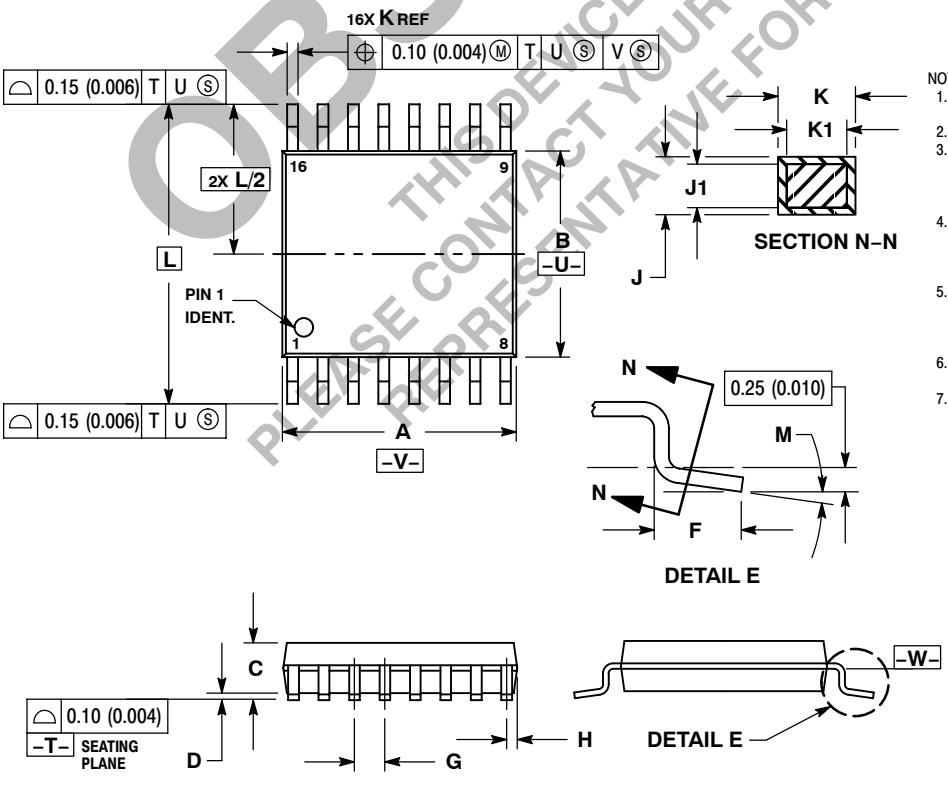
SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP−16
DT SUFFIX
CASE 948F−01
ISSUE O

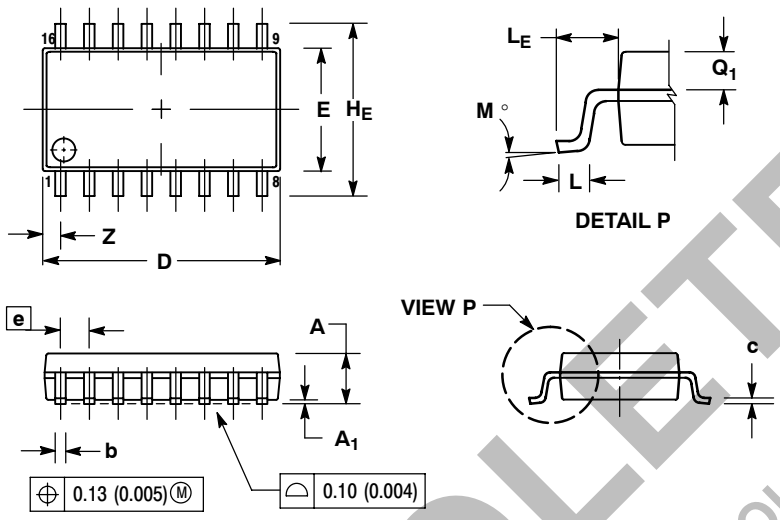


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOIC EIAJ−16
M SUFFIX
CASE 966−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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