MDNCV2003

Operational Amplifiers, High Slew Rate, Low Voltage, Rail-to-Rail Output

The MDNCV2003 op amp features high slew rate, low voltage operation with rail−to−rail output drive capability. The 1.8 V operation allows high performance operation in low voltage, low power applications. The fast slew rate and wide unity−gain bandwidth (5 MHz at 1.8 V) make this op amp suited for high speed applications. The low input offset voltage (4 mV max) allows the op amp to be used for current shunt monitoring. Additional features include no output phase reversal with overdriven inputs and ultra low input bias current of 1 pA.

The MDNCV2003 is the ideal solution for a wide range of applications and products.

Features

- Unity Gain Bandwidth: 7 MHz at V_S = 5 V
- Fast Slew Rate: 8 V/µs rising, 12.5 V/µs falling at V_S = 5 V
- Rail−to−Rail Output
- No Output Phase Reversal for Over−Driven Input Signals
- Low Offset Voltage: 0.5 mV typical
- Low Input Bias Current: 1 pA typical
- AEC−Q100 Qualified
- This Device is Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Medical Devices

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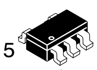
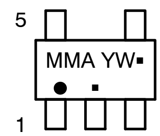


SOT23−5
CASE 483

MARKING DIAGRAM

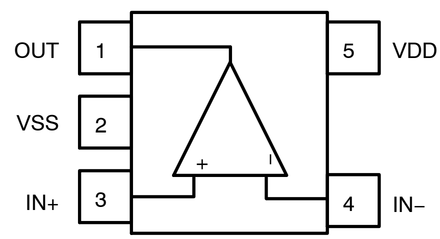


MMA	= Specific Device Code
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

Single Channel Configuration



SOT23−5
(TSOP−5)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Configuration	Automotive	Marking	Package	Shipping†
MDNCV2003SN2T1G	Single	Yes	MMA	SOT23−5 (Pb−Free)	3000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature, unless otherwise stated

Parameter	Symbol	Limit	Unit
Supply Voltage (V_{DD} − V_{SS})	V_S	7.0	V
INPUT AND OUTPUT PINS			
Input Voltage (Note 1)	V_{IN}	V_{SS} − 0.3 to 7.0	V
Input Current	I_{IN}	10	mA
Output Short Current (Note 2)	I_O	100	mA
TEMPERATURE			
Storage Temperature	T_{STG}	−65 to 150	°C
Junction Temperature	T_J	150	°C
ESD RATINGS (Note 3)			
Human Body Model	HBM	3000	V
Machine Model	MM	200	V
Charged Device Model	CDM	1000	V
OTHER PARAMETERS			
Moisture Sensitivity Level (Note 5)	MSL	Level 1	
Latch−up Current (Note 4)	I_{LU}	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Neither input should exceed the range of V_{SS} − 300 mV to 7.0 V. This device contains internal protection diodes between the input pins and V_{DD}. When V_{IN} exceeds V_{DD}, the input current should be limited to the specified value.
2. Indefinite duration; however, maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 and JESD22−A114
   ESD Machine Model tested per AEC−Q100−003 and JESD22−A115
   ESD Charged Device Model tested per AEC−Q100−011 and ANSI/ESD S5.3.1−2009
4. Latch−up current tested per JEDEC Standard JESD78.
5. Moisture Sensitivity Level tested per IPC/JEDEC standard J−STD−020A.

THERMAL INFORMATION

Thermal Metric	Symbol	Package	**Single Layer Board** (Note 6)	**Multi Layer Board** (Note 7)	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	SOT23−5	408	355	°C/W

6. Values based on a 1S standard PCB according to JEDEC51−3 with 1.0 oz copper and a 300 mm^2 copper area
7. Values based on a 1S2P standard PCB according to JEDEC51−7 with 1.0 oz copper and a 100 mm^2 copper area

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage (V_{DD} − V_{SS})	V_S	1.7	5.5	V
Specified Operating Range	T_A	−40	+125	°C
Input Common Mode Range	V_{CM}	V_{SS}	V_{DD}−0.6	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.5	4.0	mV
					5.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			**2.0**		µV/°C
		(Note 8)			6.0	µV/°C
Input Bias Current	I_{IB}			1		pA
Input Offset Current	I_{OS}			1		pA
Input Resistance	R_{IN}			1		TΩ
Input Capacitance	C_{IN}			1.2		pF
Common Mode Rejection Ratio	CMRR	V_{IN} = V_{SS} to V_{DD} – 0.6 V	70	80		dB
		V_{IN} = V_{SS} + 0.2 V to V_{DD} – 0.6 V	**65**			
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ	80	92		dB
			75			
		R_L = 2 kΩ		92		
			70			
Output Current Capability (Note 8)	I_{SC}	Sourcing	5	8		mA
		Sinking	10	14		
Output Voltage High	V_{OH}	R_L = 10 kΩ	**1.75**	1.798		V
		R_L = 2 kΩ	**1.7**	1.78		
Output Voltage Low	VOL	R_L = 10 kΩ		7	**50**	mV
		R_L = 2 kΩ		20	**100**	
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz		20		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.1		pA√Hz
DYNAMIC PERORMANCE						
Gain Bandwidth Product	GBWP			5		MHz
Slew Rate at Unity Gain	SR	Rising Edge, R_L = 2 kΩ, A_V = +1		6		V/µs
		Falling Edge, R_L = 2 kΩ, A_V = +1		9		
Phase Margin	ψ_m	R_L = 10 kΩ, C_L = 5 pF		53		°
Gain Margin	A_m	R_L = 10 kΩ, C_L = 5 pF; NCx2003, A		12		dB
		NCx2003x		8		
Settling Time	t_S	V_O = 1 Vpp, Gain = 1, C_L = 20 pF; Settling time to 0.1%		1.8		µs
Total Harmonics Distortion + Noise	THD+N	V_O = 1 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 1 kHz		0.005		%
		V_O = 1 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 10 kHz		0.025		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR		72	80		dB
			65			
Quiescent Current	I_{DD}	No load, per channel		230	560	µA
					1000	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design and/or characterization.

ELECTRICAL CHARACTERISTICS: V_S = +5.0 V At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted. **Boldface** limits apply over the specified temperature range. Guaranteed by design and/or characterization.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.5	4.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			**2.0**		µV/°C
Input Bias Current	I_{IB}			1		pA
Input Offset Current	I_{OS}			1		pA
Input Resistance	R_{IN}			1		TΩ
Input Capacitance	C_{IN}			1.2		pF
Common Mode Rejection Ratio	CMRR	V_{IN} = V_{SS} to V_{DD} – 0.6 V	65	90		dB
		V_{IN} = V_{SS} + 0.2 V to V_{DD} – 0.6 V	**63**			
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ	86	92		dB
			78			
		R_L = 2 kΩ	83	92		
			78			
Output Current Capability (Note 9)	I_{SC}	Sourcing	40	76		mA
		Sinking	50	96		
Output Voltage High	V_{OH}	R_L = 10 kΩ	**4.95**	4.99		V
		R_L = 2 kΩ	**4.9**	4.97		
Output Voltage Low	V_{OL}	R_L = 10 kΩ		8	**50**	mV
		R_L = 2 kΩ		24	**100**	
NOISE PERFORMANCE						
Voltage Noise Density	e_N	f = 1 kHz		20		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		0.1		pA√Hz
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP			7		MHz
Slew Rate at Unity Gain	SR	Rising Edge, R_L = 2 kΩ, Av = +1		8		V/µs
		Falling Edge, R_L = 2 kΩ, Av = +1		12.5		
Phase Margin	ψ_m	R_L = 10 kΩ, C_L = 5 pF		64		°
Gain Margin	A_m	R_L = 10 kΩ, C_L = 5 pF		9		dB
Settling Time	t_S	V_O = 1 V_{pp}, Gain = 1, C_L = 20 pF; Settling time to 0.1%		0.6		µs
Total Harmonics Distortion + Noise	THD+N	V_O = 4 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 1 kHz		0.002		%
		V_O = 4 V_{pp}, R_L = 2 kΩ, A_V = +1, f = 10 kHz		0.01		
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR		72	80		dB
			65			
Quiescent Current	I_{DD}	No load, per channel		300	660	µA
					1000	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. Guaranteed by design and/or characterization.

TYPICAL CHARACTERISTICS

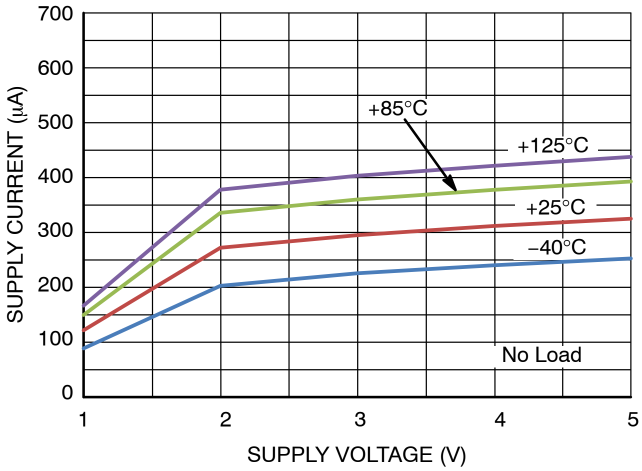


Figure 1. Quiescent Supply Current vs. Supply Voltage

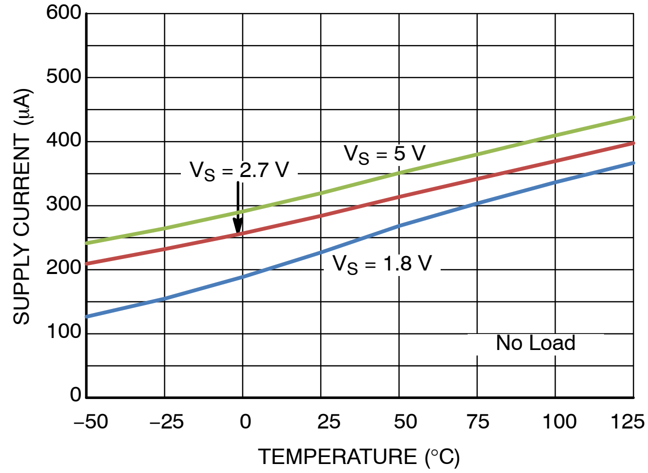


Figure 2. Quiescent Supply Current vs. Temperature

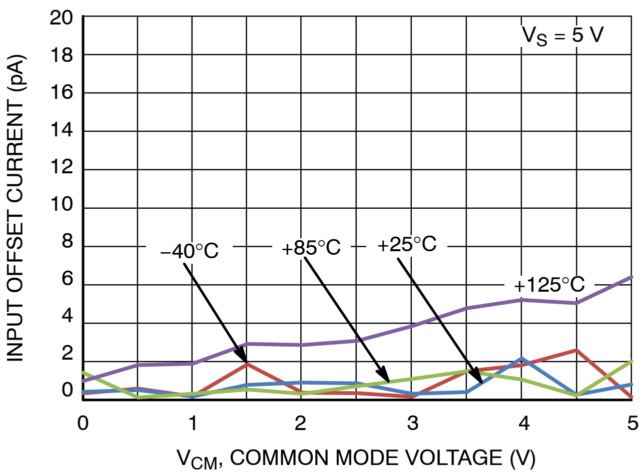


Figure 3. Input Offset Current vs. V_{CM}

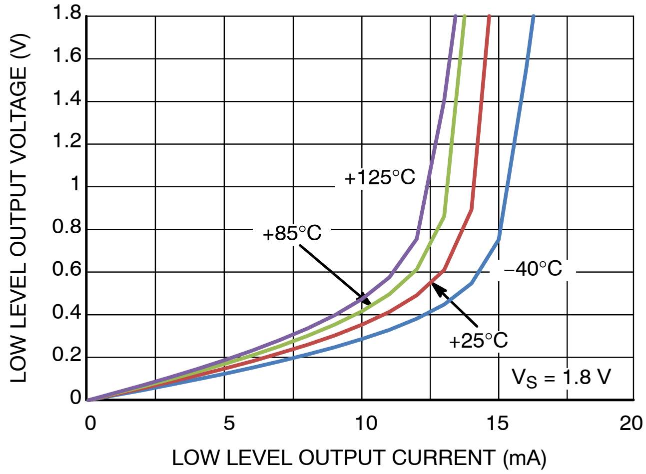


Figure 4. Low Level Output Voltage vs. Output Current @ V_S = 1.8 V

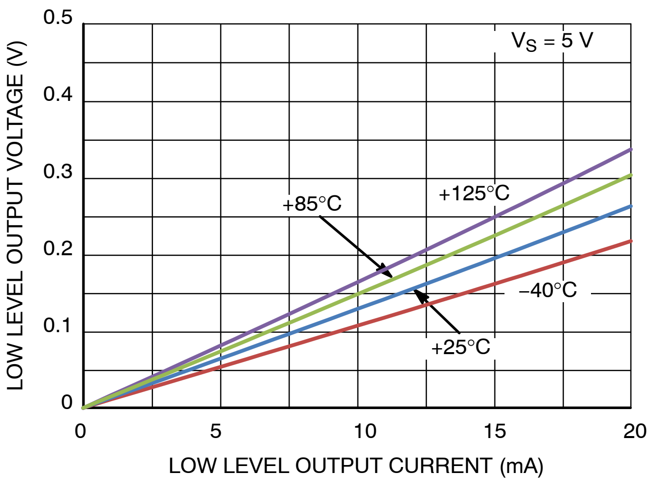


Figure 5. Low Level Output Voltage vs. Output Current @ V_S = 5 V

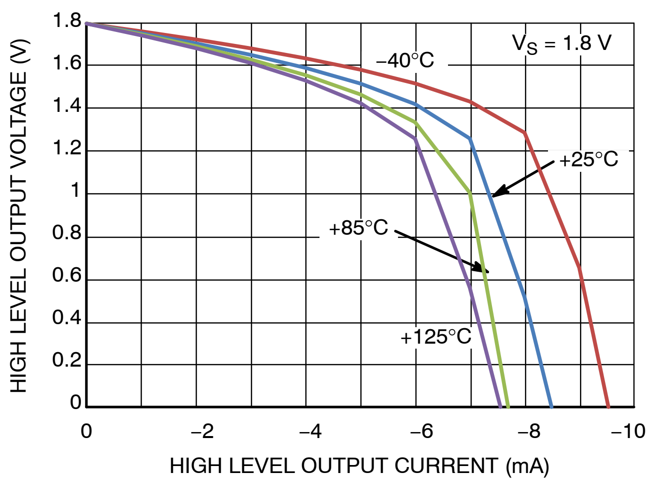


Figure 6. High Level Output Voltage vs. Output Current @ V_S = 1.8 V

TYPICAL CHARACTERISTICS

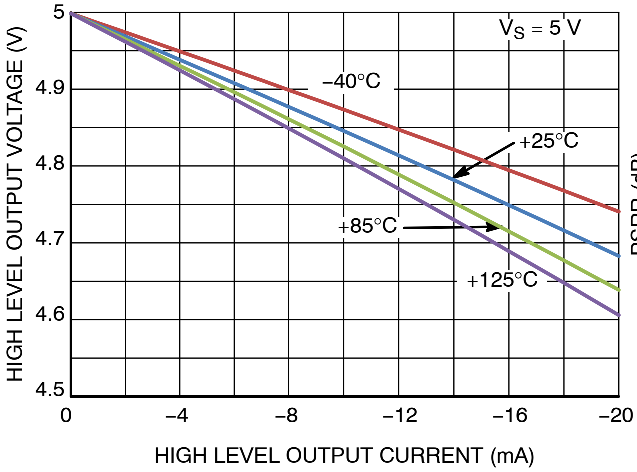


Figure 7. High Level Output Voltage vs. Output Current @ V_S = 5 V

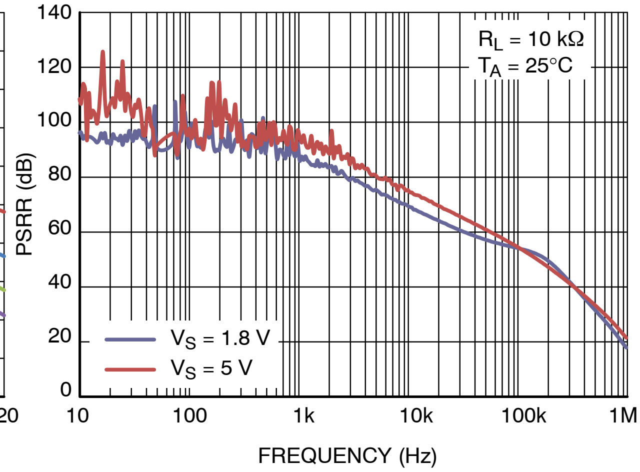


Figure 8. PSRR vs. Frequency

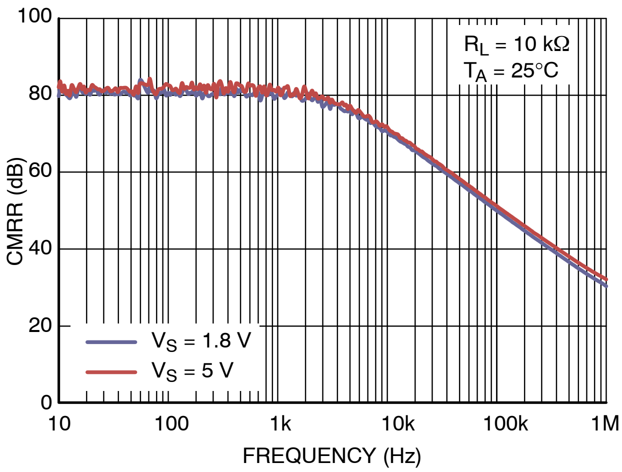


Figure 9. CMRR vs. Frequency

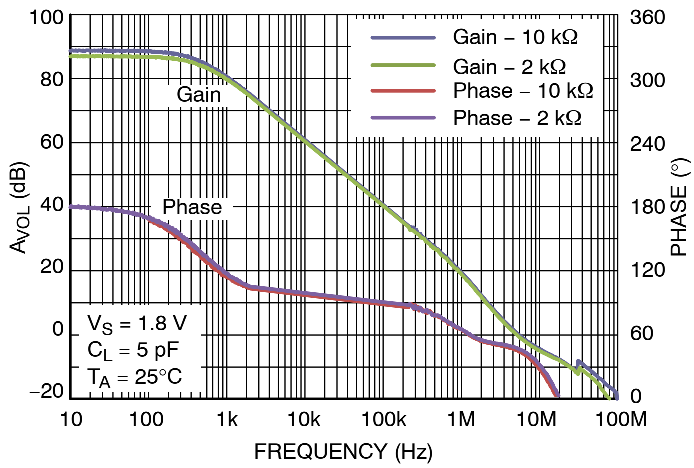


Figure 10. Open Loop Gain and Phase vs. Frequency @ V_S = 1.8 V

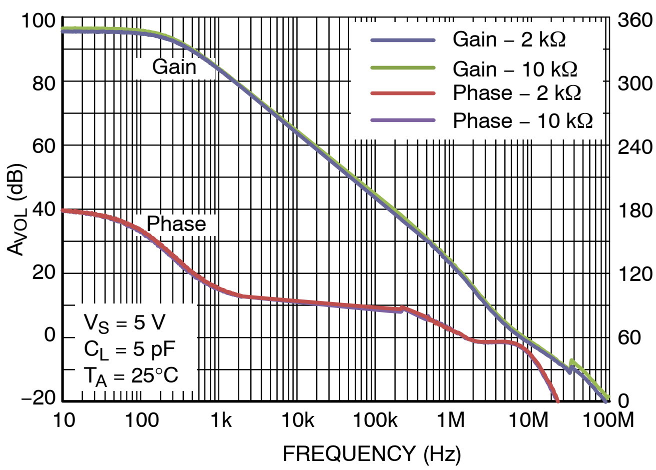


Figure 11. Open Loop Gain and Phase vs. Frequency @ V_S = 5 V

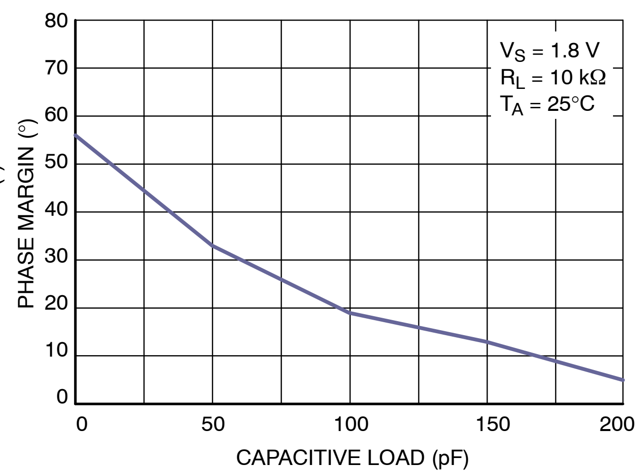


Figure 12. Phase Margin vs. Capacitive Load

TYPICAL CHARACTERISTICS

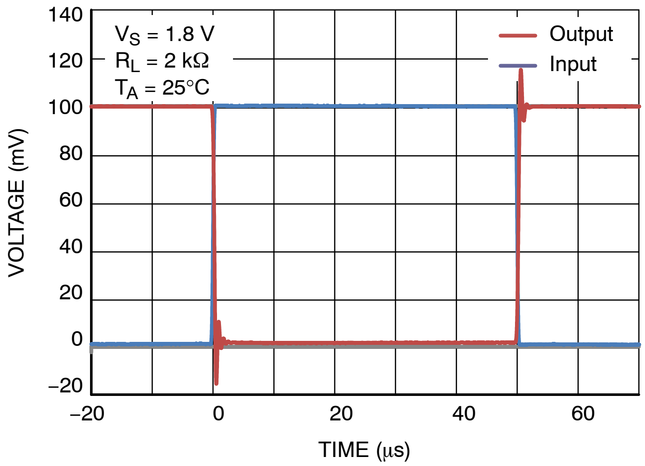


Figure 13. Inverting Small Signal Transient Response

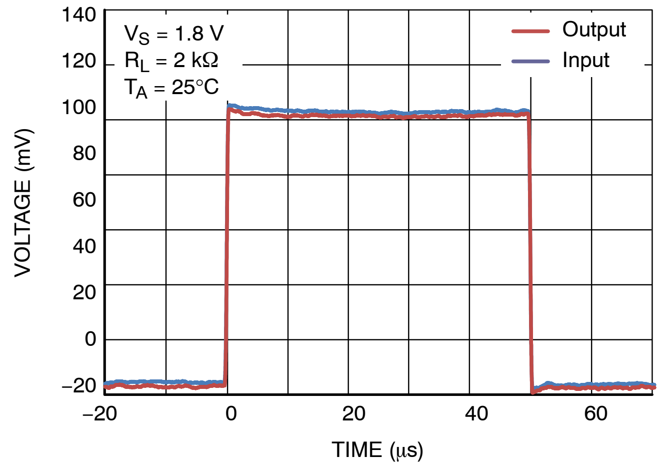


Figure 14. Non−Inverting Small Signal Transient Response

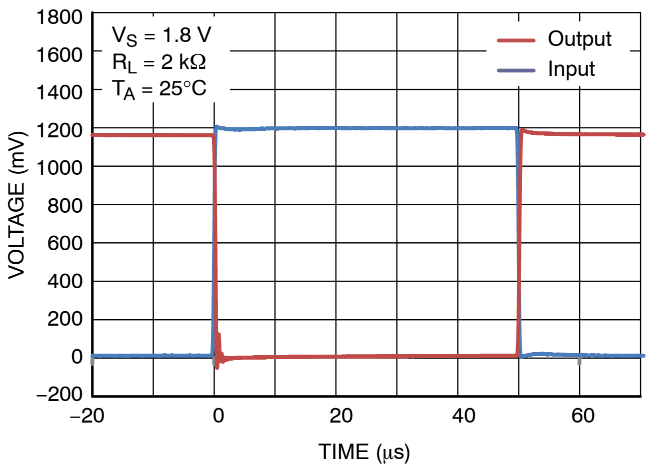


Figure 15. Inverting Large Signal Transient Response

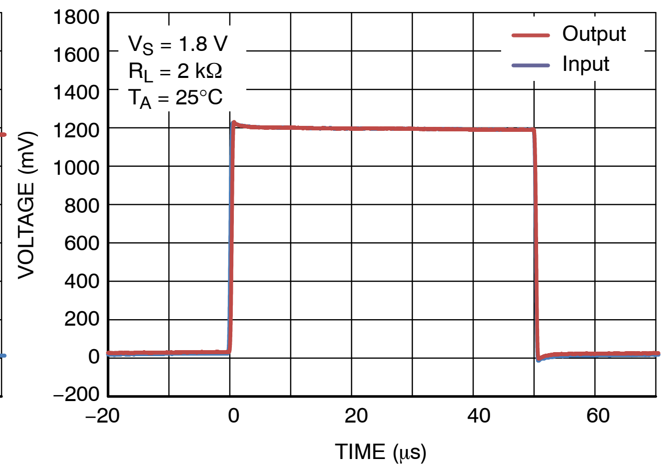


Figure 16. Non−Inverting Large Signal Transient Response

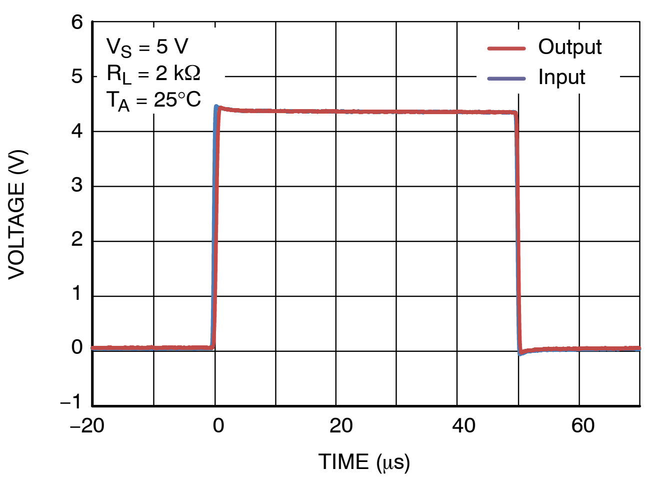


Figure 17. Non−Inverting Large Signal Transient Response

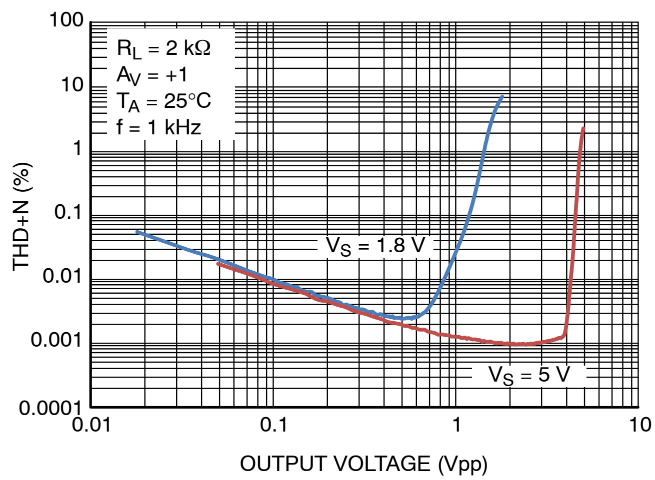


Figure 18. THD+N vs. Output Voltage

TYPICAL CHARACTERISTICS

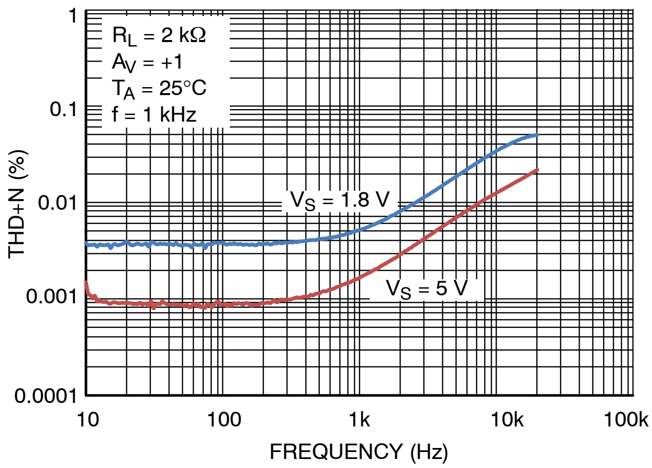


Figure 19. THD+N vs. Frequency

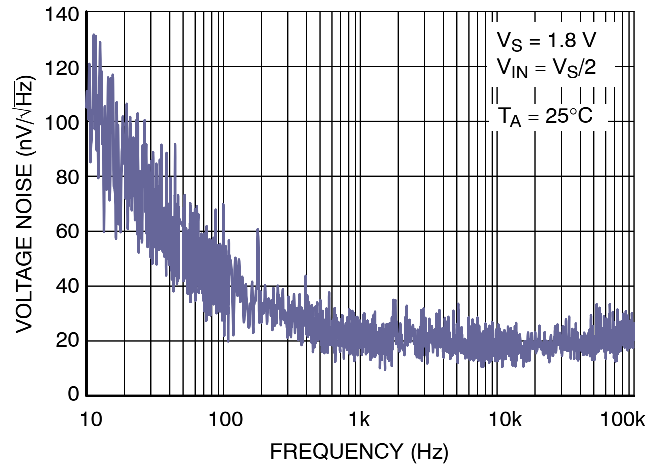


Figure 20. Input Voltage Noise vs. Frequency

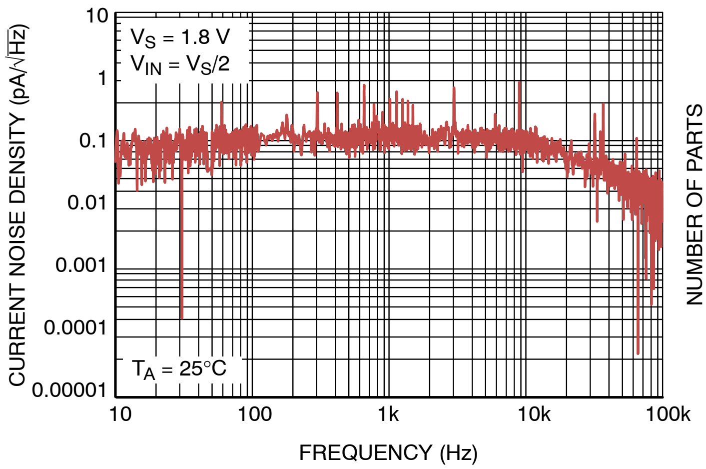


Figure 21. Noise Density vs. Frequency

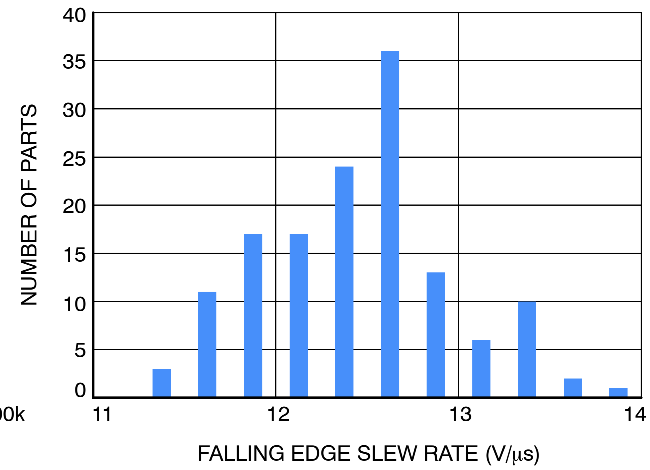


Figure 22. Falling Edge Slew Rate @ Vs = 5 V

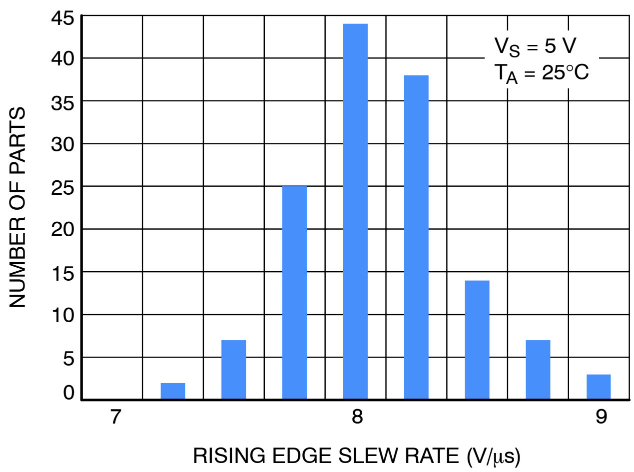


Figure 23. Rising Edge Slew Rate @ Vs = 5 V

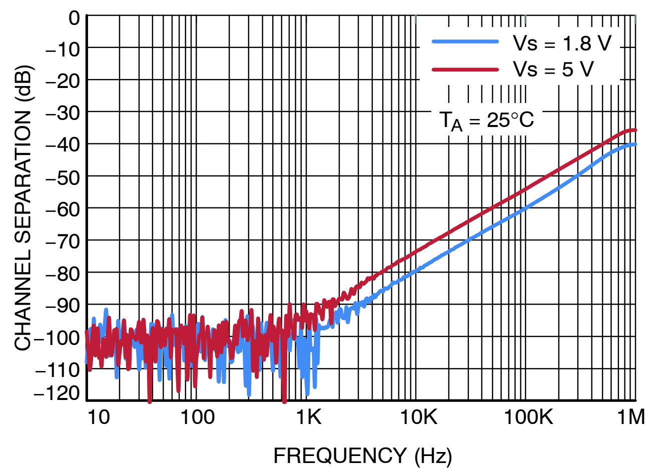
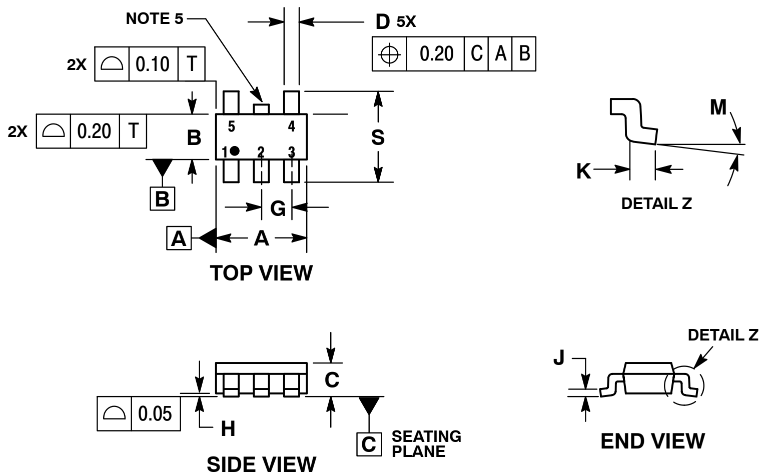


Figure 24. Channel Separation

PACKAGE DIMENSIONS

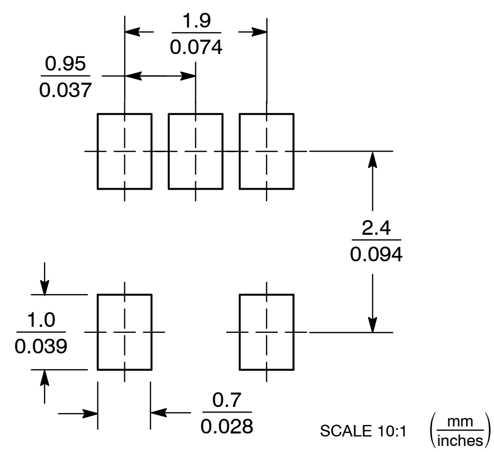
TSOP−5
CASE 483−02
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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