MJD13003

High Voltage SWITCHMODE™ Series

DPAK For Surface Mount Applications

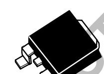
This device is designed for high−voltage, high−speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V SWITCHMODE applications such as switching regulators, inverters, motor controls, solenoid/relay drivers and deflection circuits.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C . . .
  t_c @ 1.0 A,
  100°C is 290 ns (Typ)
- 700 V Blocking Capability
- Switching and SOA Applications Information
- Electrically Similar to the Popular MJE13003

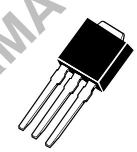
ON Semiconductor®

http://onsemi.com

NPN SILICON POWER TRANSISTOR 1.5 AMPERES 400 VOLTS, 15 WATTS

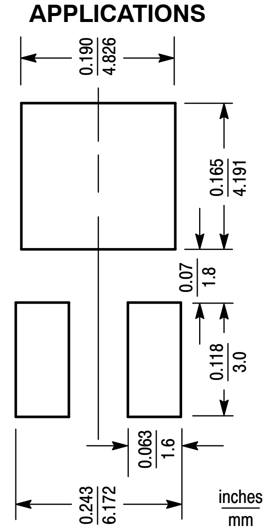


CASE 369A−13



CASE 369−07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector−Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5	Adc
Total Power Dissipation @ T_A = 25°C (2) Derate above 25°C	P_D	1.56 0.0125	Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient (2)	$R_{\theta JA}$	80	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) When surface mounted on minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector−Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	0.1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	2	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 12			
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				—
(I_C = 0.5 Adc, V_{CE} = 2 Vdc)		8	—	40	
(I_C = 1 Adc, V_{CE} = 2 Vdc)		5	—	25	
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)		—	—	0.5	
(I_C = 1 Adc, I_B = 0.25 Adc)		—	—	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)		—	—	3	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		—	—	1	
Base−Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)		—	—	1	
(I_C = 1 Adc, I_B = 0.25 Adc)		—	—	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		—	—	1.1	
DYNAMIC CHARACTERISTICS					
Current−Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	10	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	21	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle 1%)	t_d	—	0.05	0.1	μs
Rise Time	t_r	—	0.5	1	μs
Storage Time	t_s	—	2	4	μs
Fall Time	t_f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Storage Time (I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	1.7	4	μs
Crossover Time	t_c	—	0.29	0.75	μs
Fall Time	t_{fi}	—	0.15	—	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

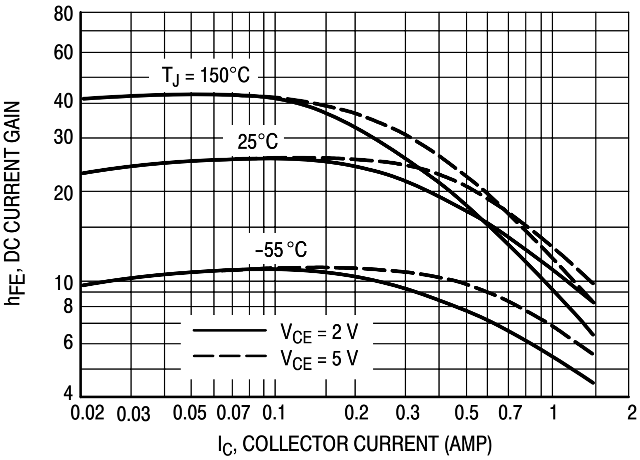


Figure 1. DC Current Gain

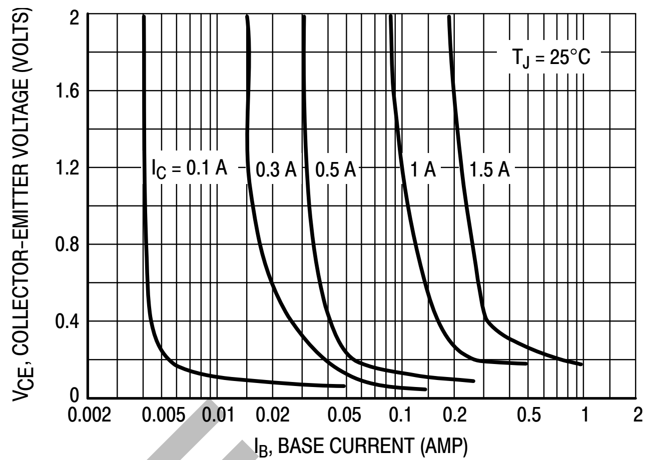


Figure 2. Collector Saturation Region

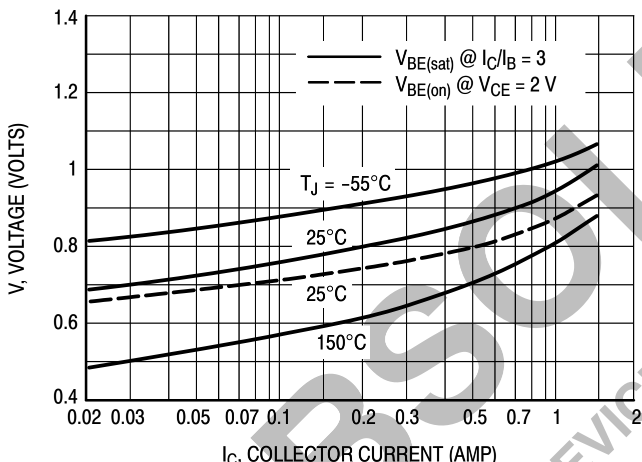


Figure 3. Base−Emitter Voltage

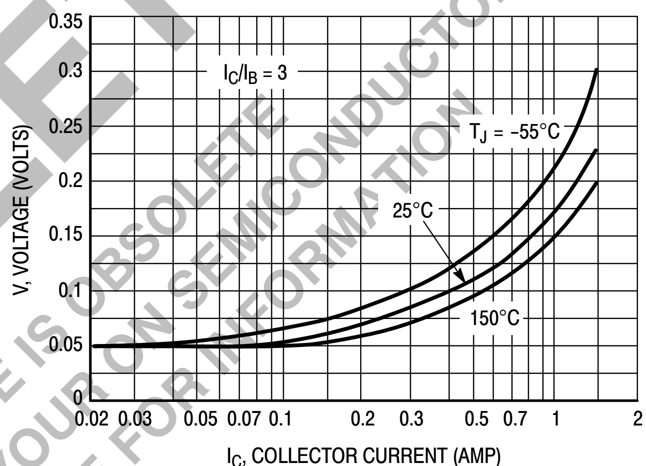


Figure 4. Collector−Emitter Saturation Region

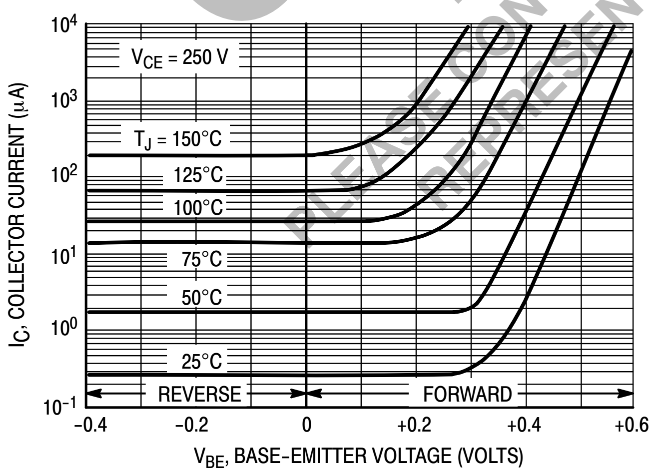


Figure 5. Collector Cutoff Region

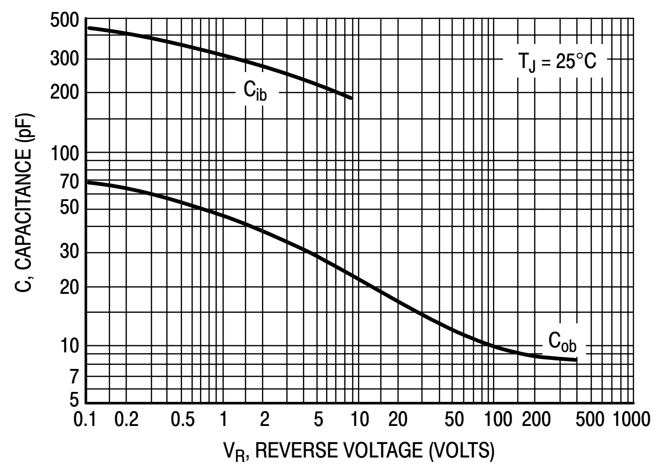
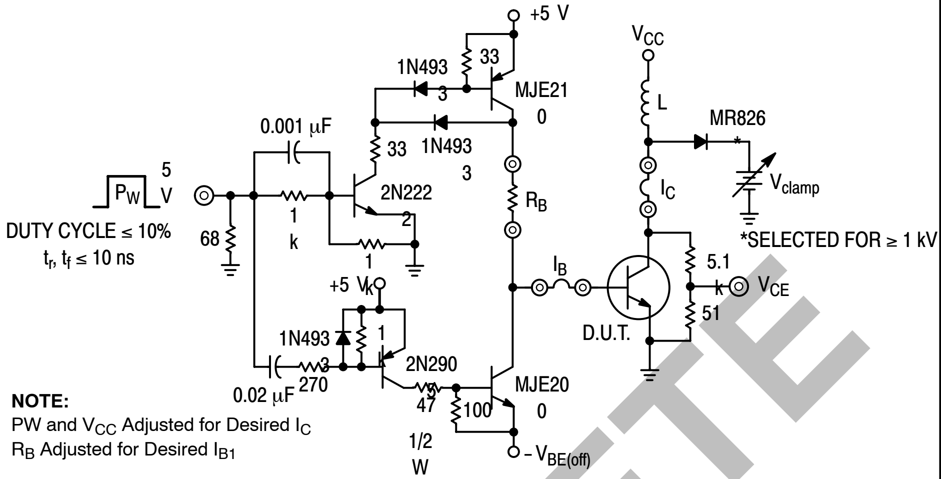
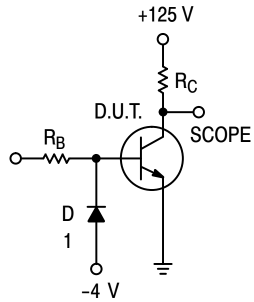
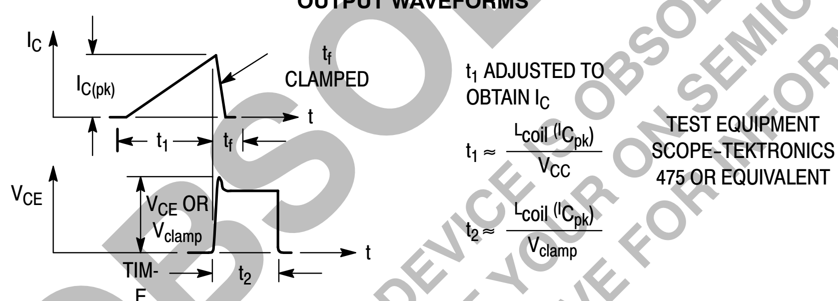
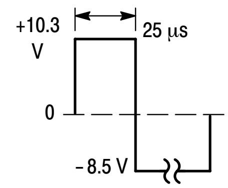


Figure 6. Capacitance

Table 1. Test Conditions For Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE:** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~200 TURNS) #20 GAP FOR 30 mH/2 A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 OR EQUIV. R_B = 47 Ω
TEST WAVEFORMS	**OUTPUT WAVEFORMS** 	 t_r, t_f < 10 ns DUTY CYCLE = 1.0% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

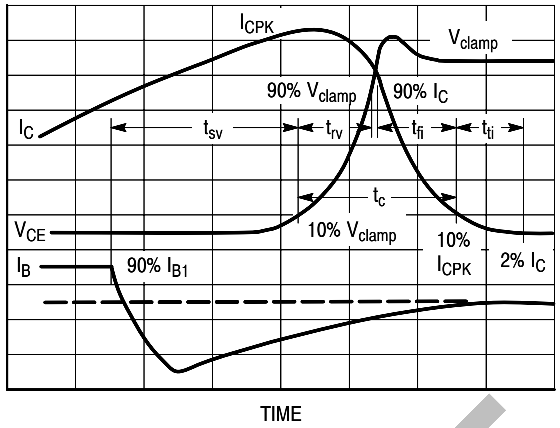


Figure 7. Inductive Switching Measurements

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25 100	1.3 1.6	0.23 0.26	0.30 0.30	0.35 0.40	0.30 0.36
1	25 100	1.5 1.7	0.10 0.13	0.14 0.26	0.05 0.06	0.16 0.29
1.5	25 100	1.8 3	0.07 0.08	0.10 0.22	0.05 0.08	0.16 0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10 – 90% V_{clamp}
t_{fi} = Current Fall Time, 90 – 10% I_C
t_{ti} = Current Tail, 10 – 2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the equation:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

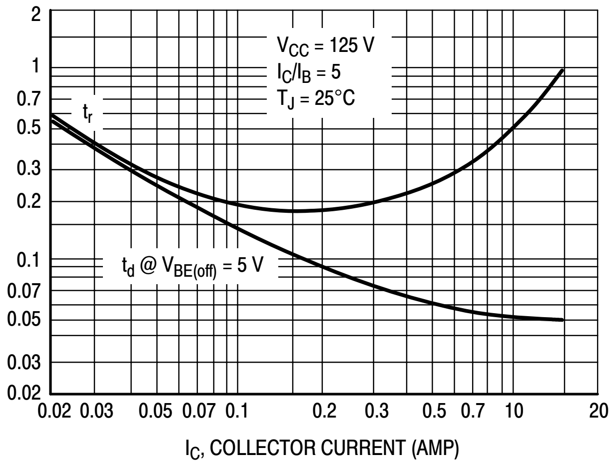


Figure 8. Turn−On Time

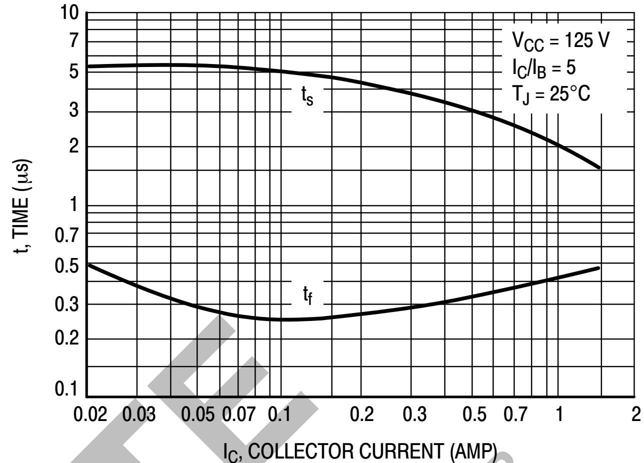


Figure 9. Turn−Off Time

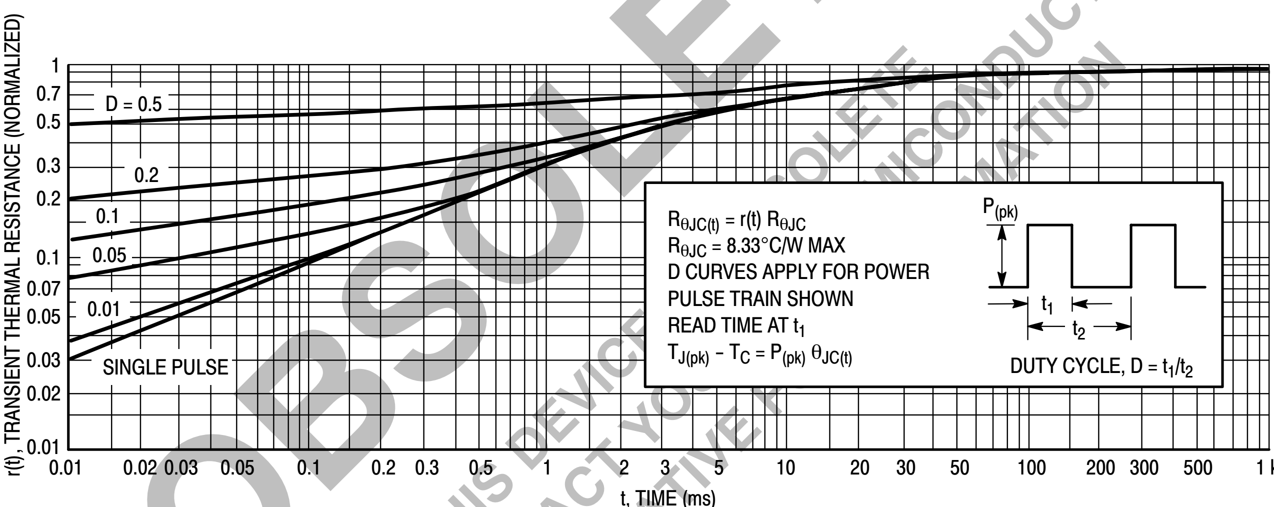


Figure 10. Thermal Response

The Sale Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

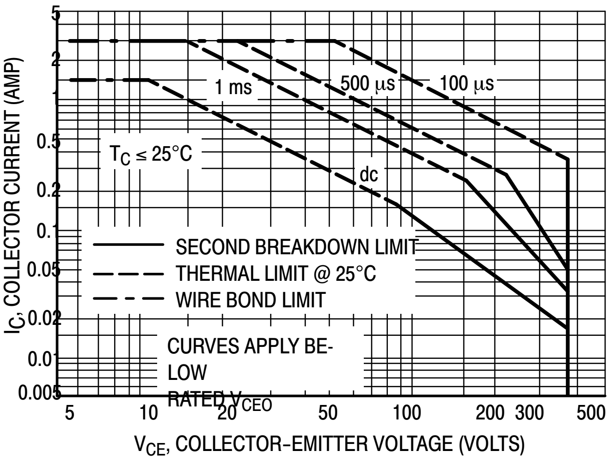


Figure 11. Active Region Safe Operating Area

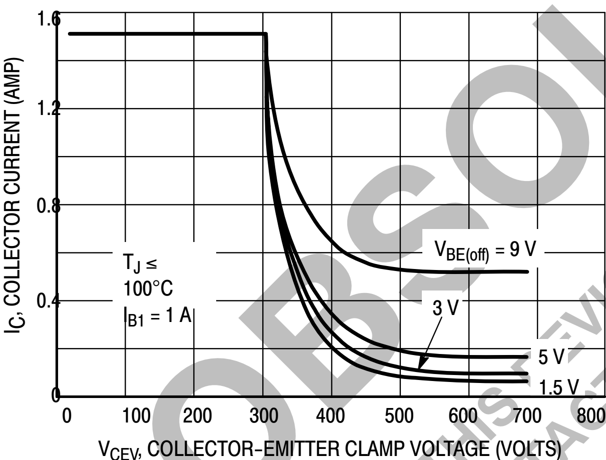


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by applying curves on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

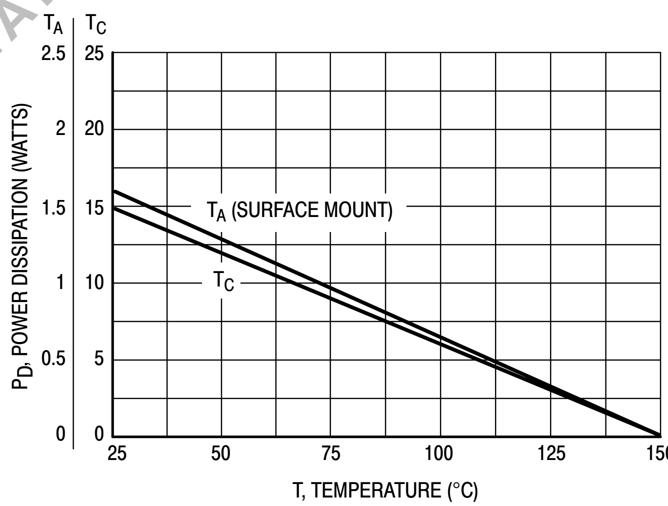
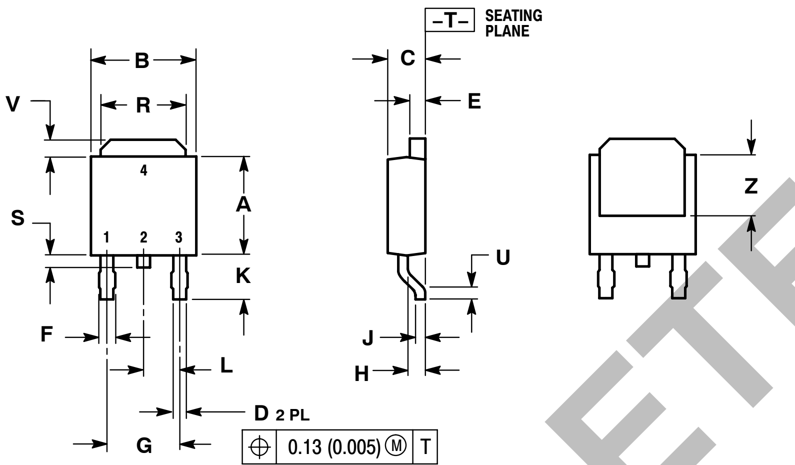


Figure 13. Power Derating

PACKAGE DIMENSIONS

CASE 369A–13
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

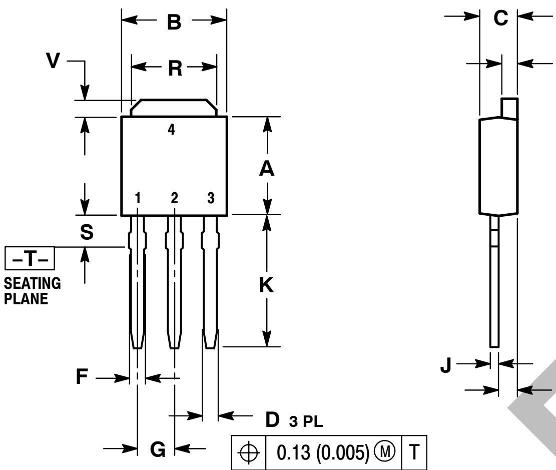
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

PACKAGE DIMENSIONS

CASE 369–07
ISSUE K



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C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

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