

NPN Silicon Power Transistor SWITCHMODE™ Series

This transistor is designed for high-voltage, power switching in inductive circuits where RBSOA and breakdown voltage are critical. They are particularly suited for line-operated SWITCHMODE applications.

Typical Applications:

- Fluorescent Lamp Ballasts
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

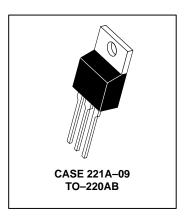
Features:

- High V_{CEV} Capability (1800 Volts)
- Low Saturation Voltage
- 100°C Performance Specified for:

Reverse–Biased SOA with Inductive Loads Switching Times with Inductive Loads Saturation Voltages Leakage Currents

MJE1320

POWER TRANSISTOR 2 AMPERES 900 VOLTS 80 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V _{CEO(sus)}	900	Vdc
Collector–Emitter Voltage	V _{CEV}	1800	Vdc
Emitter Base Voltage	V _{EB}	9	Vdc
Collector Current — Continuous Peak(1)	I _C	2 5	Adc
Base Current — Continuous Peak(1)	I _B	1.5 2.5	Adc
Total Power Dissipation @ T _C = 25°C @ T _C = 100°C Derate above 25°C	P _D	80 32 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{ heta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T _L	275	°C

⁽¹⁾ Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

	Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTER	ISTICS						
Collector–Emitter (I _C = 50 mA, I _B	Sustaining Voltage = 0)		V _{CEO(sus)}	900	_	_	Vdc
	value, $V_{BE(off)} = 1.5 \text{ Vdc}$) Value, $V_{BE(off)} = 1.5 \text{ Vdc}$, $V_{C} = 100^{\circ}\text{C}$)		I _{CEV}	_ _	_ _	0.25 2.5	mAdc
Emitter Cutoff Cut (V _{EB} = 9 Vdc, I ₀			I _{EBO}	_	_	0.25	mAdc
SECOND BREAKE	OWN						
Second Breakdov	vn Collector Current with base forward bias	sed	I _{S/b}	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 14				
ON CHARACTERIS	STICS ⁽¹⁾						
DC Current Gain	(V _{CE} = 5 Vdc)	$I_C = 2 \text{ Adc}$ $I_C = 1 \text{ Adc}$	h _{FE}	2.5 3	4.5 7	_	_
$(I_C = 1 \text{ Adc}, I_B = (I_C = 2 \text{ Adc}, I_B = 1)$	•		V _{CE(sat)}	_ _ _	0.18 0.3 0.3	1 2.5 1.5	Vdc
Base–Emitter Saturation Voltage $(I_C = 1 \text{ Adc}, I_B = 0.5 \text{ Adc})$ $(I_C = 2 \text{ Adc}, I_B = 1 \text{ Adc})$ $(I_C = 1 \text{ Adc}, I_B = 0.5 \text{ Adc}, T_C = 100^{\circ}\text{C})$		V _{BE(sat)}	_ _ _	0.2 0.9 0.15	1.5 2.8 1.5	Vdc	
DYNAMIC CHARA	CTERISTICS						
Output Capacitan (V _{CB} = 10 Vdc,	ce I _E = 0, f _{test} = 1 MHz)		C _{ob}	_	80	_	pF
SWITCHING CHAR	ACTERISTICS						
Resistive Load (Table 1)						
Delay Time			t _d	_	0.1	_	μs
Rise Time	V_{CC} = 250 Vdc, I_{C} = 1 A I_{B1} = I_{B2} = 0.5 Adc I_{p} = 25 μs, Duty Cycle ≤ 2%		t _r	_	0.8	_	μs
Storage Time			t _s	_	4	_	μs
Fall Time			t _f	_	0.8	_	μs
Inductive Load,	Clamped (Table 2)	•			•	•	
Storage Time		T 0500	t _{sv}	_	2.8	_	μs
Crossover Time	1	T _C = 25°C	t _c	_	2.2	_	μs
Storage Time	$I_C = 1 \text{ A, V}_{clamp} = 400 \text{ Vdc,}$ $V_{BE(off)} = 2 \text{ Vdc, I}_{B1} = 0.5 \text{ Adc}$		t _{sv}	_	3.7	10.5	μs
Crossover Time	$T_{C} = 100^{\circ}C$		t _c	_	3.5	10	μs
Fall Time							

Fall Time (1) Pulse Test: Pulse Width = 300 μ s. Duty Cycle \leq 2%.

TYPICAL STATIC CHARACTERISTICS

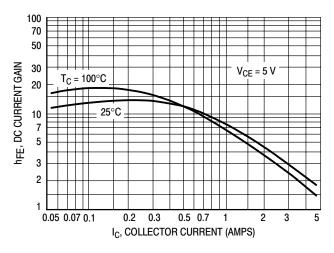


Figure 1. DC Current Gain

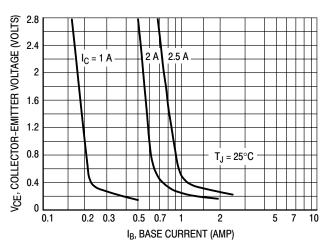


Figure 2. Collector Saturation Region

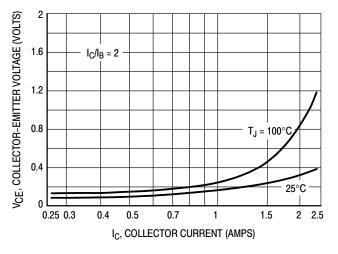


Figure 3. Collector–Emitter Saturation Voltage

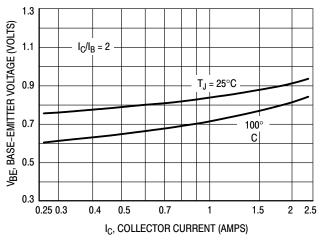


Figure 4. Base-Emitter Saturation Voltage

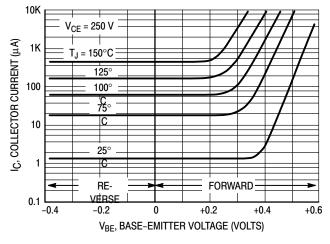


Figure 5. Collector Cutoff Region

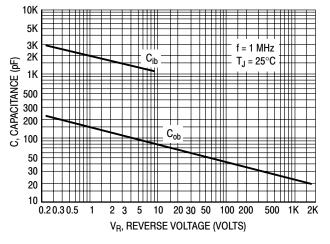
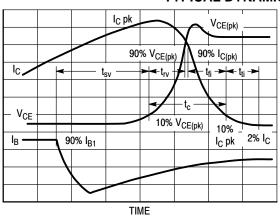


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS



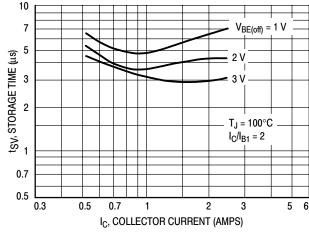


Figure 7. Inductive Switching Measurements

Figure 8. Inductive Storage Time

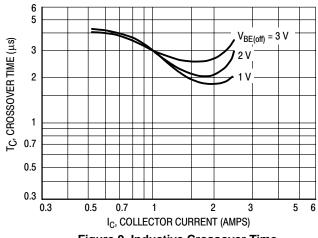


Figure 9. Inductive Crossover Time

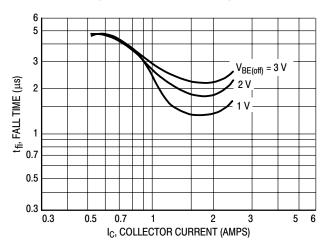
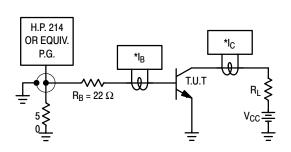


Figure 10. Inductive Fall Time

Table 1. Resistive Load Switching

t_d and t_r





*Tektronix AM503 P6302 or Equivalent

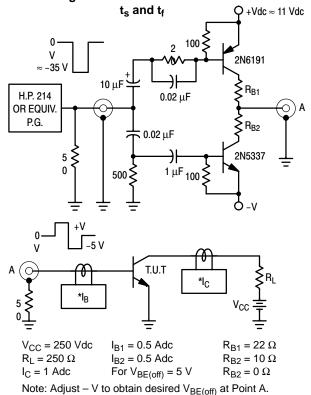
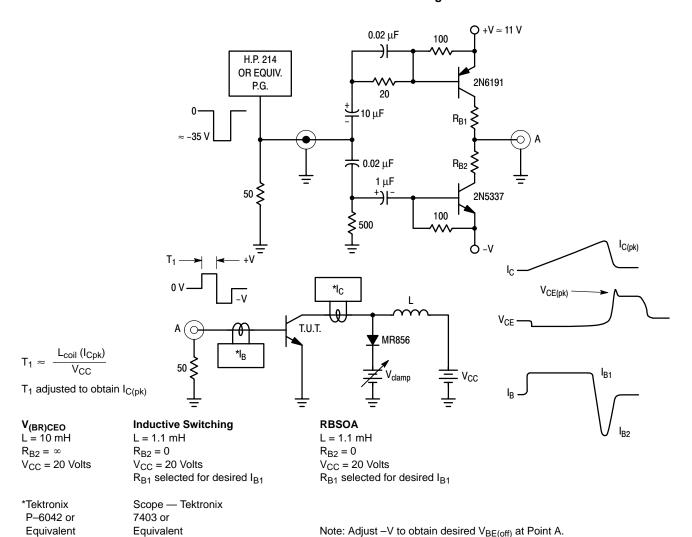


Table 2. Inductive Load Switching



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

 $T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA

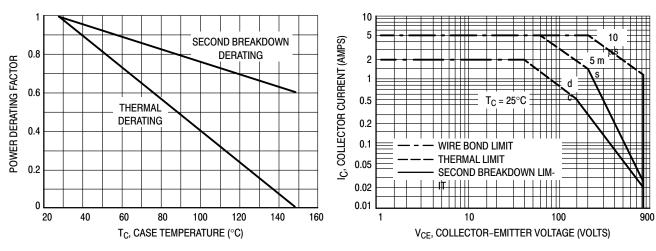


Figure 11. Power Derating

Figure 12. Maximum Rated Forward Bias Safe Operating Area

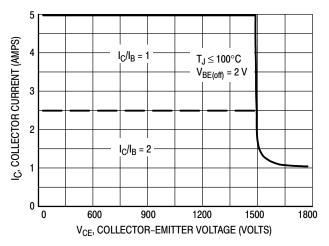


Figure 13. Maximum Rated Reverse Bias Safe Operating Area

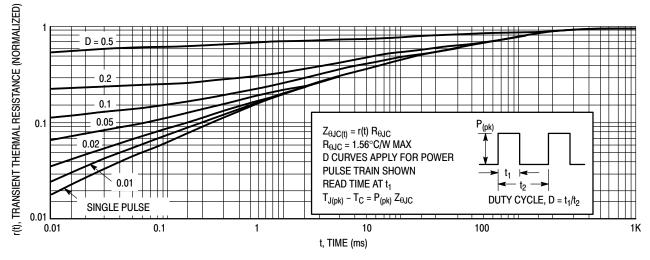
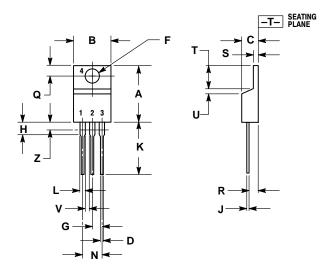


Figure 14. Thermal Response

PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

Notes

Notes

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