MT9P031-DIE

1/2.5-Inch 5 Mp CMOS Digital Image Sensor Die

The MT9P031 from ON Semiconductor is a 1/2.5-inch CMOS active-pixel digital image sensor die with an active imaging pixel array of 2592 (H) × 1944 (V). It incorporates sophisticated camera functions on-die, such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The 5-Mp CMOS image sensor die features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a full resolution image at 14 frames per second (fps).

An on-die analog-to-digital converter (ADC) provides 12 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

The MT9P031 produces extraordinarily clear, sharp, digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including digital still cameras, digital video cameras, and PC cameras.

Features

- High Frame Rate
- Superior Low-light Performance
- Low Dark Current
- Global Reset Release, which Starts Exposure of All Rows Simultaneously
- Bulb Exposure Mode for Arbitrary Exposure Times
- Snapshot Mode to Take Frames on Demand
- Horizontal and Vertical Mirror Image
- Column and Row Skip Modes to Reduce Image Size without Reducing the Field-of-View
- Column and Row Binning Modes to Improve Image Quality when Resizing
- Simple Two-wire Serial Interface
- Programmable Controls: Gain, Frame Rate, Frame Size, and Exposure
- On-die PLL

Die Database

- Die Outline (see Figure 2)
- Singulated Die Size: 8,499 μm ±25 μm × 7,950 μm ±25 μm
- Bond Pad Location and Identification Tables (see Tables 1 and 2)

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Options	Designator
Form − Die	D
Testing − Standard (Level 1) Probe	C1

ORDERING INFORMATION

Die
MT9P031D00STCC18BC1

Consult die distributor or factory before ordering to verify long-term availability of these die products.

General Physical Specifications

- Die Thickness: 200 μm ±12 μm *(Consult Factory for Other Thickness)*
- Back Side Wafer Surface of Bare Silicon
- Typical Metal 1 Thickness: 3.1 kÅ
- Typical Metal 2 Thickness: 3.1 kÅ
- Typical Metal 3 Thickness: 6.1 kÅ
- Metallization Composition: 99.5% Al and 0.5% Cu over Ti
- Typical Topside Passivation: 2.2 kÅ Nitride over 6.0 kÅ of Undoped Oxide
- Passivation Openings (MIN): 75 x 90 mm

Key Performance Parameters

- Optical Format: 1/2.5-inch (4:3)
- Active Imager Size: 7.13 mm Diagonal, 5.70 mm (H) × 4.28 mm (V)
- Active Pixels: 2592 (H) × 1944 (V)
- Pixel Size: 2.2 μm × 2.2 μm
- Color Filter Array: RGB Bayer Pattern
- Shutter Type
  - Global Reset Release (GRR), Snapshot Only
  - Electronic Rolling Shutter (ERS)
- Maximum Data Rate/Master Clock
  - 96 Mp/s at 96 MHz (2.8 V I/O)
  - 48 Mp/s at 48 MHz (1.8 V I/O)
- Frame Rate
  - Full Resolution, Programmable Up to 14 fps
  - VGA (640 (H) × 480 (V), with Binning), Programmable Up to 53 fps

Key Performance Parameters (Continued)

- ADC Resolution: 12-bit, On-die
- Responsivity: 1.4 V/lux−sec (550 nm)
- Pixel Dynamic Range: 70.1 dB
- SNR MAX: 38.1 dB
- Supply Voltage
  - I/O Digital: 1.7–3.1 V
  - Digital: 1.7–1.9 V (1.8 V Nominal)
  - Analog: 2.6–3.1 V (2.8 V Nominal)
- Power Consumption: 381 mW (Full Resolution)
- Operating Temperature: –30°C to +70°C

Die Testing Procedures

ON Semiconductor imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to ensure product functionality in ON Semiconductor's standard package. Because the package environment is not within ON Semiconductor's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

ON Semiconductor retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. ON Semiconductor reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to ON Semiconductor's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on our web site (www.onsemi.com).

Bonding Instructions

The MT9P031 imager die has 67 bond pads. Refer to Table 1 and Table 2 for a complete list of bond pads and coordinates.

The MT9P031 imager die does not require the user to determine bond option features.

The die also has several pads defined as "do not use." These pads are used for engineering purposes and should not be used. Bonding these pads could result in a nonfunctional die.

Figure 1 shows the typical die connections. For low-noise operation, the MT9P031 die requires separate supplies for analog and digital power. Power supply rails should be decoupled to ground using capacitors. The use of inductance filters is not recommended.

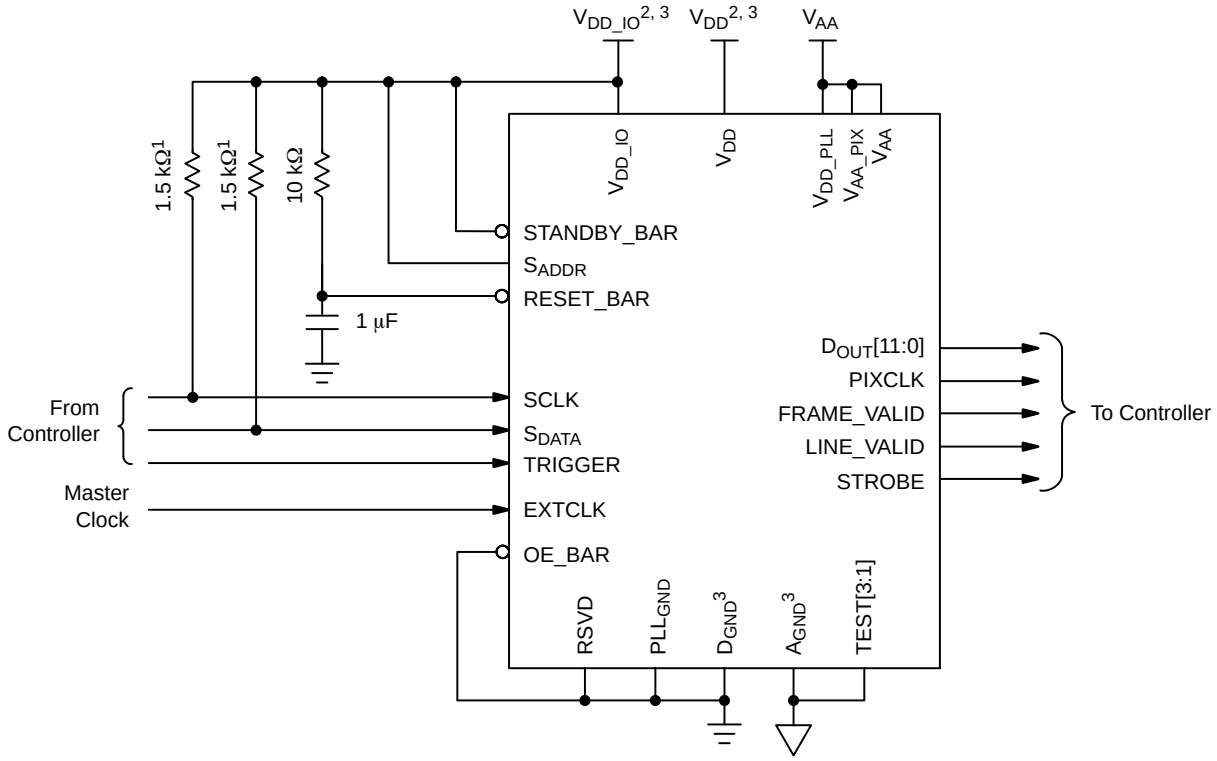
All D_{GND} pads must be tied together, as must all A_{GND} pads, all V_{DD_IO} pads, and all V_{DD} pads. Doing so will minimize risk of damage to the sensor in an ESD event.

Storage Requirements

ON Semiconductor die products are packaged for shipping in a clean room environment. Upon receipt, the customer should transfer the die or wafers to a similar environment for storage. ON Semiconductor recommends the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% relative humidity ±10%. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Configuration

Figure 1 shows typical configuration schematics for the MT9P031.



Notes:
1. ON Semiconductor recommends a resistor value of 1.5 kΩ, but greater values may be used for slower two-wire speed.
2. All power supplies should be adequately decoupled.
3. All D_{GND} pads must be tied together, as must all A_{GND} pads, all V_{DD_IO} pads, and all V_{DD} pads.

Figure 1. Typical Configuration (Connection) Parallel Mode

Bond Pad Location and Identification Tables

Table 1. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF PAD 1

Pad Number	Pad Name	“X” Microns (Note 1)	“Y” Microns (Note 1)	“X” Inches (Note 1)	“Y” Inches (Note 1)
1	DNU (Note 2)	0.00	0.00	0.0000000	0.0000000
2	DNU	131.04	0.00	0.0051591	0.0000000
3	DNU	7592.00	0.00	0.2988976	0.0000000
4	DNU	7723.04	0.00	0.3040567	0.0000000
5	V_{DD}[1]	7970.63	–258.39	0.3138041	–0.0101726
6	V_{DD}[2]	7970.63	–400.23	0.3138041	–0.0157569
7	D_{GND}[3]	7970.63	–749.43	0.3138041	–0.0295049
8	D_{GND}[4]	7970.63	–880.47	0.3138041	–0.0346640
9	D_{OUT}[11]	7970.63	–1115.47	0.3138041	–0.0439159
10	D_{OUT}[10]	7970.63	–1350.47	0.3138041	–0.0531679
11	D_{OUT}[9]	7970.63	–1605.03	0.3138041	–0.0631900
12	D_{OUT}[8]	7970.63	–1840.03	0.3138041	–0.0724419
13	D_{OUT}[7]	7970.63	–2094.59	0.3138041	–0.0824640
14	D_{OUT}[6]	7970.63	–2329.59	0.3138041	–0.0917159
15	D_{GND}[5]	7970.63	–2564.59	0.3138041	–0.1009679
16	D_{GND}[6]	7970.63	–2695.63	0.3138041	–0.1061270
17	V_{DD_IO}[3]	7970.63	–2930.63	0.3138041	–0.1153789
18	V_{DD_IO}[4]	7970.63	–3072.47	0.3138041	–0.1209632
19	D_{OUT}[5]	7970.63	–3307.47	0.3138041	–0.1302152
20	D_{OUT}[4]	7970.63	–3562.03	0.3138041	–0.1402372
21	D_{OUT}[3]	7970.63	–3797.03	0.3138041	–0.1494892
22	D_{OUT}[2]	7970.63	–4051.59	0.3138041	–0.1595112
23	D_{OUT}[1]	7970.63	–4286.59	0.3138041	–0.1687632
24	D_{OUT}[0]	7970.63	–4541.15	0.3138041	–0.1787852
25	PIXCLK	7970.63	–4776.15	0.3138041	–0.1880372
26	EXTCLK	7970.63	–5030.71	0.3138041	–0.1980593
27	DNU	7970.63	–5421.19	0.3138041	–0.2134325
28	DNU	7970.63	–5711.19	0.3138041	–0.2248498
29	DNU	7970.63	–6077.83	0.3138041	–0.2392844
30	DNU	7970.63	–6367.83	0.3138041	–0.2507018
31	GND_PLL	7970.63	–6899.27	0.3138041	–0.2716246
32	V_{DD_PLL}	7970.63	–7134.27	0.3138041	–0.2808766
33	DNU	131.04	–7669.53	0.0051591	–0.3019500
34	DNU	0.00	–7669.53	0.0000000	–0.3019500
35	V_{AA}[4]	–247.59	–7411.15	–0.0097474	–0.2917774
36	V_{AA}[3]	–247.59	–7269.31	–0.0097474	–0.2861931
37	V_{AA}[2]	–247.59	–7127.47	–0.0097474	–0.2806089
38	V_{AA}[1]	–247.59	–6985.63	–0.0097474	–0.2750246
39	A_{GND}[6]	–247.59	–6750.63	–0.0097474	–0.2657726
40	A_{GND}[5]	–247.59	–6619.59	–0.0097474	–0.2606136
41	A_{GND}[4]	–247.59	–6488.55	–0.0097474	–0.2554545
42	A_{GND}[3]	–247.59	–6357.51	–0.0097474	–0.2502955
43	TEST1 (Note 3)	–247.59	–6122.51	–0.0097474	–0.2410435

Table 1. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF PAD 1 (continued)

Pad Number	Pad Name	"X" Microns (Note 1)	"Y" Microns (Note 1)	"X" Inches (Note 1)	"Y" Inches (Note 1)
44	TEST2 (Note 3)	–247.59	–5887.51	–0.0097474	–0.2317915
45	DNU	–247.59	–5652.51	–0.0097474	–0.2225396
46	DNU	–247.59	–5417.51	–0.0097474	–0.2132876
47	OE_BAR	–247.59	–4911.51	–0.0097474	–0.1933663
48	RESET_BAR	–247.59	–4676.51	–0.0097474	–0.1841144
49	TRIGGER	–247.59	–4441.51	–0.0097474	–0.1748624
50	STANDBY_BAR	–247.59	–4206.51	–0.0097474	–0.1656104
51	S_{ADDR}	–247.59	–3971.51	–0.0097474	–0.1563585
52	V_{DD}[3]	–247.59	–3799.59	–0.0097474	–0.1495900
53	V_{DD_IO}[2]	–247.59	–3344.55	–0.0097474	–0.1316750
54	V_{DD_IO}[1]	–247.59	–3202.71	–0.0097474	–0.1260907
55	D_{GND}[2]	–247.59	–3071.67	–0.0097474	–0.1209317
56	D_{GND}[1]	–247.59	–2940.63	–0.0097474	–0.1157726
57	STROBE	–247.59	–2747.83	–0.0097474	–0.1081821
58	LINE_VALID	–247.59	–2512.83	–0.0097474	–0.0989301
59	FRAME_VALID	–247.59	–2258.27	–0.0097474	–0.0889081
60	RSVD (Note 4)	–247.59	–2023.27	–0.0097474	–0.0796561
61	S_{DATA}	–247.59	–1788.27	–0.0097474	–0.0704041
62	SCLK	–247.59	–1553.27	–0.0097474	–0.0611522
63	TEST3 (Note 3)	–247.59	–1068.55	–0.0097474	–0.0420687
64	A_{GND}[2]	–247.59	–833.55	–0.0097474	–0.0328167
65	A_{GND}[1]	–247.59	–702.51	–0.0097474	–0.0276577
66	V_{AA_PIX}[2]	–247.59	–467.51	–0.0097474	–0.0184057
67	V_{AA_PIX}[1]	–247.59	–325.67	–0.0097474	–0.0128215

1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use. See "Bonding Instructions".
3. TEST1–TEST3 pads must be tied to A_{GND} for normal device operation.
4. RSVD pad must be tied to D_{GND} for normal device operation.

Table 2. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF DIE (0,0)

Pad Number	Pad Name	"X" Microns (Note 1)	"Y" Microns (Note 1)	"X" Inches (Note 1)	"Y" Inches (Note 1)
1	DNU (Note 2)	–3861.52	3834.77	–0.1520283	0.1509750
2	DNU	–3730.48	3834.77	–0.1468693	0.1509750
3	DNU	3730.48	3834.77	0.1468693	0.1509750
4	DNU	3861.52	3834.77	0.1520283	0.1509750
5	V_{DD}[1]	4109.11	3576.38	0.1617758	0.1408024
6	V_{DD}[2]	4109.11	3434.54	0.1617758	0.1352181
7	D_{GND}[3]	4109.11	3085.34	0.1617758	0.1214701
8	D_{GND}[4]	4109.11	2954.30	0.1617758	0.1163110
9	D_{OUT}[11]	4109.11	2719.30	0.1617758	0.1070591
10	D_{OUT}[10]	4109.11	2484.30	0.1617758	0.0978071
11	D_{OUT}[9]	4109.11	2229.74	0.1617758	0.0877850
12	D_{OUT}[8]	4109.11	1994.74	0.1617758	0.0785331
13	D_{OUT}[7]	4109.11	1740.18	0.1617758	0.0685110
14	D_{OUT}[6]	4109.11	1505.18	0.1617758	0.0592591
15	D_{GND}[5]	4109.11	1270.18	0.1617758	0.0500071
16	D_{GND}[6]	4109.11	1139.14	0.1617758	0.0448480
17	V_{DD_IO}[3]	4109.11	904.14	0.1617758	0.0355961
18	V_{DD_IO}[4]	4109.11	762.30	0.1617758	0.0300118
19	D_{OUT}[5]	4109.11	527.30	0.1617758	0.0207598
20	D_{OUT}[4]	4109.11	272.74	0.1617758	0.0107378
21	D_{OUT}[3]	4109.11	37.74	0.1617758	0.0014858
22	D_{OUT}[2]	4109.11	–216.82	0.1617758	–0.0085362
23	D_{OUT}[1]	4109.11	–451.82	0.1617758	–0.0177882
24	D_{OUT}[0]	4109.11	–706.38	0.1617758	–0.0278102
25	PIXCLK	4109.11	–941.38	0.1617758	–0.0370622
26	EXTCLK	4109.11	–1195.94	0.1617758	–0.0470843
27	DNU	4109.11	–1586.42	0.1617758	–0.0624575
28	DNU	4109.11	–1876.42	0.1617758	–0.0738748
29	DNU	4109.11	–2243.06	0.1617758	–0.0883094
30	DNU	4109.11	–2533.06	0.1617758	–0.0997268
31	GND_PLL	4109.11	–3064.50	0.1617758	–0.1206496
32	V_{DD_PLL}	4109.11	–3299.50	0.1617758	–0.1299016
33	DNU	–3730.48	–3834.77	–0.1468693	–0.1509750
34	DNU	–3861.52	–3834.77	–0.1520283	–0.1509750
35	V_{AA}[4]	–4109.11	–3576.38	–0.1617758	–0.1408024
36	V_{AA}[3]	–4109.11	–3434.54	–0.1617758	–0.1352181
37	V_{AA}[2]	–4109.11	–3292.70	–0.1617758	–0.1296339
38	V_{AA}[1]	–4109.11	–3150.86	–0.1617758	–0.1240496
39	A_{GND}[6]	–4109.11	–2915.86	–0.1617758	–0.1147976
40	A_{GND}[5]	–4109.11	–2784.82	–0.1617758	–0.1096386
41	A_{GND}[4]	–4109.11	–2653.78	–0.1617758	–0.1044795
42	A_{GND}[3]	–4109.11	–2522.74	–0.1617758	–0.0993205
43	TEST1 (Note 3)	–4109.11	–2287.74	–0.1617758	–0.0900685
44	TEST2 (Note 3)	–4109.11	–2052.74	–0.1617758	–0.0808165

Table 2. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF DIE (0,0) (continued)

Pad Number	Pad Name	"X" Microns (Note 1)	"Y" Microns (Note 1)	"X" Inches (Note 1)	"Y" Inches (Note 1)
45	DNU	–4109.11	–1817.74	–0.1617758	–0.0715646
46	DNU	–4109.11	–1582.74	–0.1617758	–0.0623126
47	OE_BAR	–4109.11	–1076.74	–0.1617758	–0.0423913
48	RESET_BAR	–4109.11	–841.74	–0.1617758	–0.0331394
49	TRIGGER	–4109.11	–606.74	–0.1617758	–0.0238874
50	STANDBY_BAR	–4109.11	–371.74	–0.1617758	–0.0146354
51	SADDR	–4109.11	–136.74	–0.1617758	–0.0053835
52	V_{DD}[3]	–4109.11	35.18	–0.1617758	0.0013850
53	V_{DD_IO}[2]	–4109.11	490.22	–0.1617758	0.0193000
54	V_{DD_IO}[1]	–4109.11	632.06	–0.1617758	0.0248843
55	D_{GND}[2]	–4109.11	763.10	–0.1617758	0.0300433
56	D_{GND}[1]	–4109.11	894.14	–0.1617758	0.0352024
57	STROBE	–4109.11	1086.94	–0.1617758	0.0427929
58	LINE_VALID	–4109.11	1321.94	–0.1617758	0.0520449
59	FRAME_VALID	–4109.11	1576.50	–0.1617758	0.0620669
60	RSVD (Note 4)	–4109.11	1811.50	–0.1617758	0.0713189
61	S_{DATA}	–4109.11	2046.50	–0.1617758	0.0805709
62	SCLK	–4109.11	2281.50	–0.1617758	0.0898228
63	TEST3 (Note 3)	–4109.11	2766.22	–0.1617758	0.1089063
64	A_{GND}[2]	–4109.11	3001.22	–0.1617758	0.1181583
65	A_{GND}[1]	–4109.11	3132.26	–0.1617758	0.1233173
66	V_{AA_PIX}[2]	–4109.11	3367.26	–0.1617758	0.1325693
67	V_{AA_PIX}[1]	–4109.11	3509.10	–0.1617758	0.1381535

1. Reference to center of each bond pad from center of die.
2. DNU = do not use. See "Bonding Instructions".
3. TEST1–TEST3 pads must be tied to A_{GND} for normal device operation.
4. RSVD pad must be tied to D_{GND} for normal device operation.

Die Features

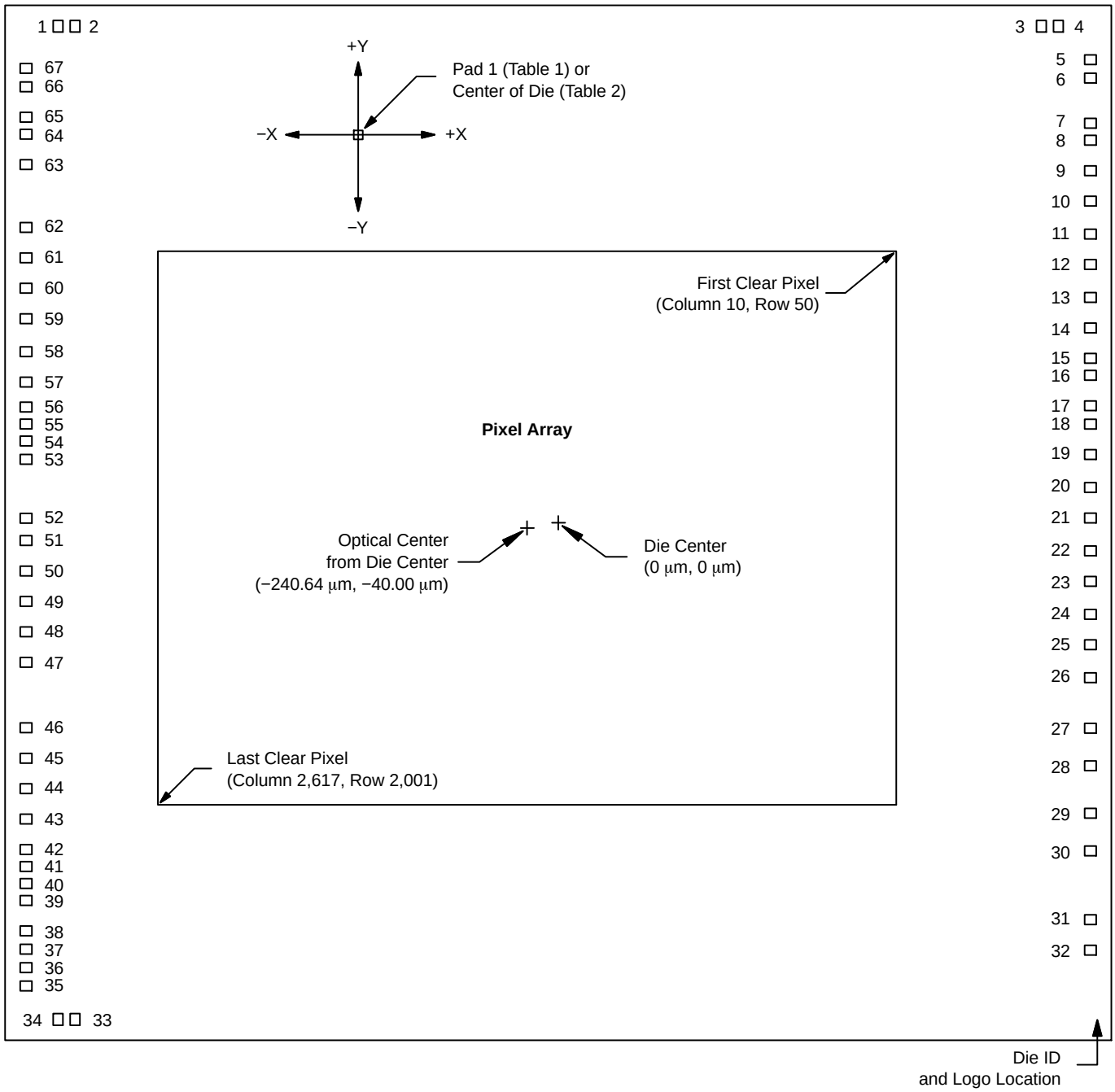


Figure 2. Die Outline (Top View)

Physical Specifications

Table 3. PHYSICAL DIMENSIONS

Feature	Dimensions
Wafer Diameter	200 mm (8″)
Die Thickness	200 μm ±12 μm
Singulated Die Size (after Wafer Saw) Width (X Dimension) Length (Y Dimension)	 8,499 μm ±25 μm 7,950 μm ±25 μm
Bond Pad Size (MIN)	85 μm × 100 μm (3.35 mil × 3.94 mil)
Passivation Openings (MIN)	75 μm × 90 μm (2.95 mil × 3.54 mil)
Minimum Bond Pad Pitch	131 μm (5.16 mil)
Center of Bond Pad 1 to Center of Die	X = 3,861.520 μm, Y = –3,834.765 μm
Optical Array Optical Center from Die Center Optical Center from Center of Pad 1	 X = –240.64 μm, Y = –40.00 μm X = 3,620.88 μm, Y = –3,874.77 μm
First Clear Pixel (Column 10, Row 50) From Die Center From Center of Pad 1	 X = 2,622.88 μm, Y = 2,106.08 μm X = 6,484.40 μm, Y = –1,728.69 μm
Last Clear Pixel (Column 2,617, Row 2,001) From Die Center From Center of Pad 1	 X = –3,112.96 μm, Y = –2,186.08 μm X = 748.56 μm, Y = –6,020.85 μm

Die Orientation in Reconstructed Wafer

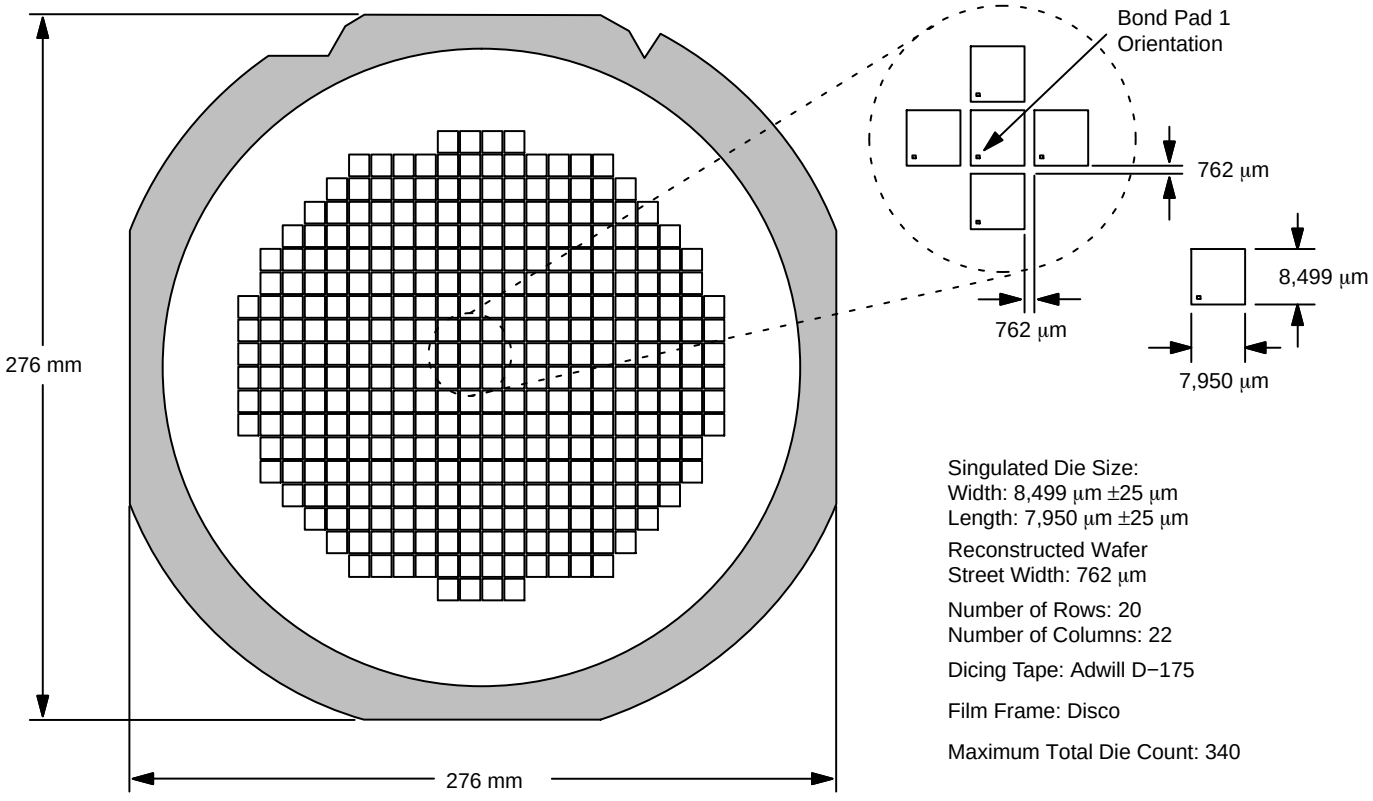


Figure 3. Die Orientation in Reconstructed Wafer

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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