MT9V124-DIE

1/13-Inch System-on-a-Chip (SOC) CMOS Digital Image Sensor Die

ON Semiconductor®

www.onsemi.com

The MT9V124 is a 1/13-inch CMOS digital image sensor with an active-pixel array of 648 (H) × 488 (V). It includes sophisticated camera functions such as auto exposure control, auto white balance, black level control, flicker detection and avoidance, and defect correction. It is designed for low light performance. It is programmable through a simple two-wire serial interface. The MT9V124 produces extraordinarily clear, sharp digital pictures that make it the perfect choice for a wide range of applications, including medical, biometric, and other industrial applications.

Options	Designator
Form − Die	D
Testing − Standard (Level 1) Probe	C1

ORDERING INFORMATION

Die
MT9V124D00STCK22DC1

Consult die distributor or factory before ordering to verify long-term availability of these die products.

Features

- DigitalClarity CMOS Imaging Technology
- Superior Low-light Performance
- Ultra-low-power
- VGA Video at 30 fps
- Internal Master Clock Generated by On-chip Phase Locked Loop (PLL) Oscillator
- Electronic Rolling Shutter (ERS), Progressive Scan
- Integrated Image Flow Processor (IFP) for Single-die Camera Module
- Automatic Image Correction and Enhancement, Including Four-channel Lens Shading Correction
- Supports ITU−R.656 Format with Odd Timing Code
- Two-wire Serial Interface Providing Access to Registers and Microcontroller Memory
- Selectable Output Data Format: YCbCr, 565RGB, RAW8+2-bit, and BT656
- LVDS Serial Data Output
- Independently Configurable Gamma Correction
- Direct XDMA Access (Reducing Serial Commands)
- Integrated Hue Rotation ±22 Degrees

Die Database

- Die Outline (see Figure 2)
- Singulated Die Size (Nominal Dimension): 2,711.55 μm × 2,711.55 μm
- Bond Pad Location and Identification Tables (see Tables 1 and 2)

General Physical Specifications

- Die Thickness: 200 μm ±12 μm *(Consult Factory for Other Thickness)*
- Backside Die Surface of Bare Silicon
- Typical Metal 1 Thickness: 3.1 kÅ
- Typical Metal 2 Thickness: 3.2 kÅ
- Typical Metal 3 Thickness: 3.2 kÅ
- Typical Metal 4 Thickness: 4.0 kÅ
- Metallization Composition: 99.5% Al and 0.5% Cu over Ti
- Typical Topside Passivation: 2.2 kÅ Nitride over 5.0 kÅ of Undoped Oxide
- Passivation Openings (MIN): 75 × 90 μm

Key Performance Parameters

- Optical Format: 1/13-inch
- Full Resolution: 640 × 480 Pixels (VGA)
- Pixel Size: 1.75 × 1.75 μm
- Dynamic Range: 58 dB
- SNR_{MAX} (Temporal): 33.4 dB
- Responsivity: 1.65 V/lux−sec
- Chief Ray Angle: 24°
- Color Filter Array: RGB Bayer Pattern
- Active Pixel Array Area: 648 × 488
- Shutter Type: Electronic Rolling Shutter (ERS)

Key Performance Parameters (Continued)

- Input Clock Frequency: 4–44 MHz
- Maximum Frame Rate: 30 fps at Full Resolution
- Maximum Serial Output Frequency: 264 MHz
- Supply Voltage:
  - Analog: 2.8 V
  - Digital: 1.8 V
- Typical Power Consumption: 55 mW
- Operating Temperature: –30°C to +70°C

Die Testing Procedures

ON Semiconductor imager die products are tested with a standard probe (C1) test level. Wafer probe is performed at an elevated temperature to test product functionality in ON Semiconductor's standard package. Because the package environment is not within ON Semiconductor's control, the user must determine the necessary heat sink requirements to ensure that the die junction temperature remains within specified limits.

Image quality is verified through various imaging tests. The probe functional test flow provides test coverage for the on-die ADC, logic, two-wire serial interface bus, and pixel array. Test conditions, margins, limits, and test sequence are determined by individual product yields and reliability data.

ON Semiconductor retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. ON Semiconductor reserves the right to change the probe program at any time to improve the reliability, packaged device yield, or performance of the product.

Die users may experience differences in performance relative to ON Semiconductor's data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Functional Specifications

The specifications provided in this document are for reference only. For target functional and parametric specifications, refer to the product data sheet found on our web site (www.onsemi.com).

Bonding Instructions

The MT9V124 die has 30 bond pads. Refer to Table 1 and Table 2 for a complete list of bond pads and coordinates.

The MT9V124 die does not require the user to determine bond option features.

To ensure proper device operation, all power supply bond pads must be bonded.

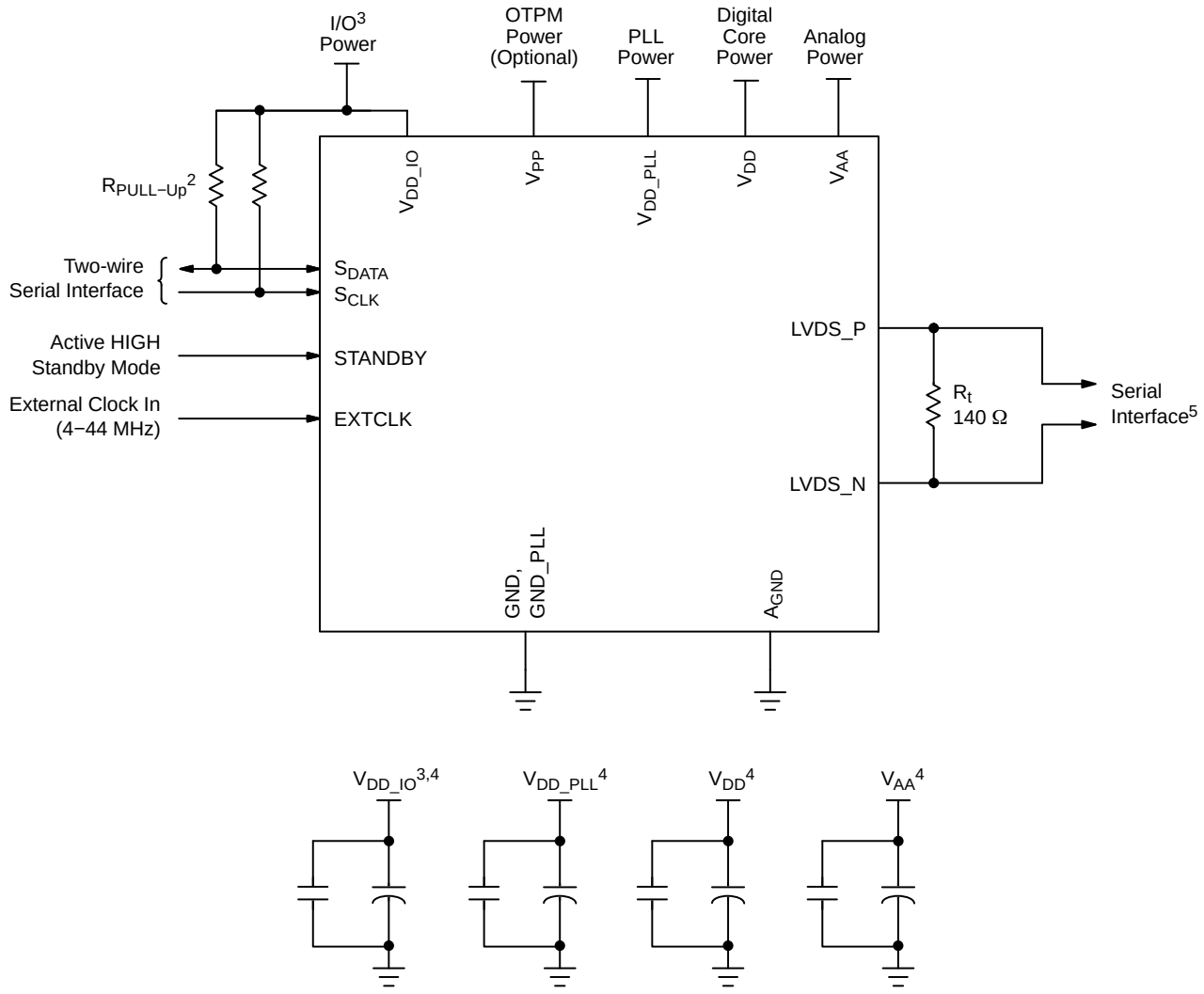
Figure 1 shows typical MT9V124 device connections. For low-noise operation, the MT9V124 requires separate supplies for analog and digital sections of the die. Both power supply rails should be decoupled to ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

The MT9V124 provides dedicated signals for digital core, and I/O power domains that can be at different voltages. The PLL and analog circuitry require clean power sources.

Storage Requirements

ON Semiconductor die products are packaged for shipping in a clean room environment. Upon receipt, the customer should transfer the die to a similar environment for storage. ON Semiconductor recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% relative humidity ±10%. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

Typical Connection



Notes:
1. This typical connection shows only one scenario out of multiple possible variations for this sensor.
2. ON Semiconductor recommends a 1.5 kΩ resistor value for the two-wire serial interface $R_{PULL-UP}$; however, a greater value may be used for slower transmission speed.
3. All inputs must be configured with V_{DD_IO}.
4. ON Semiconductor recommends that 0.1 μF and 1 μF decoupling capacitors for each power supply are mounted as close as possible to the module (Low-Z path). Actual values and numbers may vary depending on layout and design considerations, such as capacitor effective series resistance (ESR), dielectric, or power supply source impedance.
5. LVDS output requires termination resistor (140 Ω) to be placed closely at the sensor side.

Figure 1. Typical Configuration (Connection)

Bond Pad Location and Identification Tables

Table 1. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF PAD 1

Pad Number	Pad Name	"X" Microns (Note 1)	"Y" Microns (Note 1)	"X" Inches (Note 1)	"Y" Inches (Note 1)
1	V_{PP}	0	0	0	0
2	V_{DD}[2]	695.94	161.575	0.027399158	0.006361208
3	STANDBY	847.71	161.575	0.033374343	0.006361208
4	DNU (Note 2)	1009.12	161.575	0.039729054	0.006361208
5	GND[2]	1159.12	161.575	0.045634554	0.006361208
6	DNU	1308.75	161.575	0.051525488	0.006361208
7	V_{DD_IO}[2]	1459.12	161.575	0.057445554	0.006361208
8	DNU	1609.12	161.575	0.063351054	0.006361208
9	DNU	1772.91	161.575	0.069799467	0.006361208
10	DNU	2547	42.215	0.10027539	0.001662005
11	DNU	2547	–122.315	0.10027539	–0.004815542
12	V_{DD_IO}[1]	2547	–272.315	0.10027539	–0.010721042
13	DNU	2547	–422.685	0.10027539	–0.016641108
14	GND[1]	2547	–572.685	0.10027539	–0.022546608
15	V_{DD}[1]	2547	–722.685	0.10027539	–0.028452108
16	S_{DATA}	1464.44	–2385.425	0.057655003	–0.093914182
17	S_{CLK}	1309.78	–2385.425	0.051566039	–0.093914182
18	DNU	1157.885	–2385.425	0.045585932	–0.093914182
19	V_{DD_OP}[0]	1007.42	–2385.425	0.039662125	–0.093914182
20	DNU	857.325	–2385.425	0.033752885	–0.093914182
21	CLKIN	706.835	–2385.425	0.027828094	–0.093914182
22	V_{DD}[0]	556.66	–2385.425	0.021915704	–0.093914182
23	LVDS_N	406.66	–2385.425	0.016010204	–0.093914182
24	LVDS_P	242.5	–2385.425	0.009547225	–0.093914182
25	GND[0]	92.5	–2385.425	0.003641725	–0.093914182
26	GND_PLL[0]	0	–1589.125	0	–0.062563851
27	V_{DD_PLL}[0]	0	–1438.725	0	–0.056642603
28	V_{AA}[0]	0	–443.145	0	–0.017446619
29	A_{GND}[0]	0	–292.745	0	–0.011525371
30	DNU	0	–182.345	0	–0.007178923

1. Reference to center of each bond pad from center of bond pad 1.
2. DNU = do not use.

Table 2. BOND PAD LOCATION AND IDENTIFICATION FROM CENTER OF DIE (0,0)

Pad Number	Pad Name	"X" Microns (Note 1)	"Y" Microns (Note 1)	"X" Inches (Note 1)	"Y" Inches (Note 1)
1	V_{PP}	–1273.5	1111.925	–0.050137695	0.043776487
2	V_{DD}[2]	–577.56	1273.5	–0.022738537	0.050137695
3	STANDBY	–425.79	1273.5	–0.016763352	0.050137695
4	DNU (Note 2)	–264.38	1273.5	–0.010408641	0.050137695
5	GND[2]	–114.38	1273.5	–0.004503141	0.050137695
6	DNU	35.25	1273.5	0.001387793	0.050137695
7	V_{DD_IO}[2]	185.62	1273.5	0.007307859	0.050137695
8	DNU	335.62	1273.5	0.013213359	0.050137695
9	DNU	499.41	1273.5	0.019661772	0.050137695
10	DNU	1273.5	1154.14	0.050137695	0.045438492
11	DNU	1273.5	989.61	0.050137695	0.038960946
12	V_{DD_IO}[1]	1273.5	839.61	0.050137695	0.033055446
13	DNU	1273.5	689.24	0.050137695	0.027135379
14	GND[1]	1273.5	539.24	0.050137695	0.021229879
15	V_{DD}[1]	1273.5	389.24	0.050137695	0.015324379
16	S_{DATA}	190.94	–1273.5	0.007517308	–0.050137695
17	S_{CLK}	36.28	–1273.5	0.001428344	–0.050137695
18	DNU	–115.615	–1273.5	–0.004551763	–0.050137695
19	V_{DD_IO}[0]	–266.08	–1273.5	–0.01047557	–0.050137695
20	DNU	–416.175	–1273.5	–0.01638481	–0.050137695
21	CLKIN	–566.665	–1273.5	–0.022309601	–0.050137695
22	V_{DD}[0]	–716.84	–1273.5	–0.028221991	–0.050137695
23	LVDS_N	–866.84	–1273.5	–0.034127491	–0.050137695
24	LVDS_P	–1031	–1273.5	–0.04059047	–0.050137695
25	GND[0]	–1181	–1273.5	–0.04649597	–0.050137695
26	GND_PLL[0]	–1273.5	–477.2	–0.050137695	–0.018787364
27	V_{DD_PLL}[0]	–1273.5	–326.8	–0.050137695	–0.012866116
28	V_{AA}[0]	–1273.5	668.78	–0.050137695	0.026329869
29	A_{GND}[0]	–1273.5	819.18	–0.050137695	0.032251117
30	DNU	–1273.5	929.58	–0.050137695	0.036597565

1. Reference to center of each bond pad from center of die (0, 0).
2. DNU = do not use.

Die Features

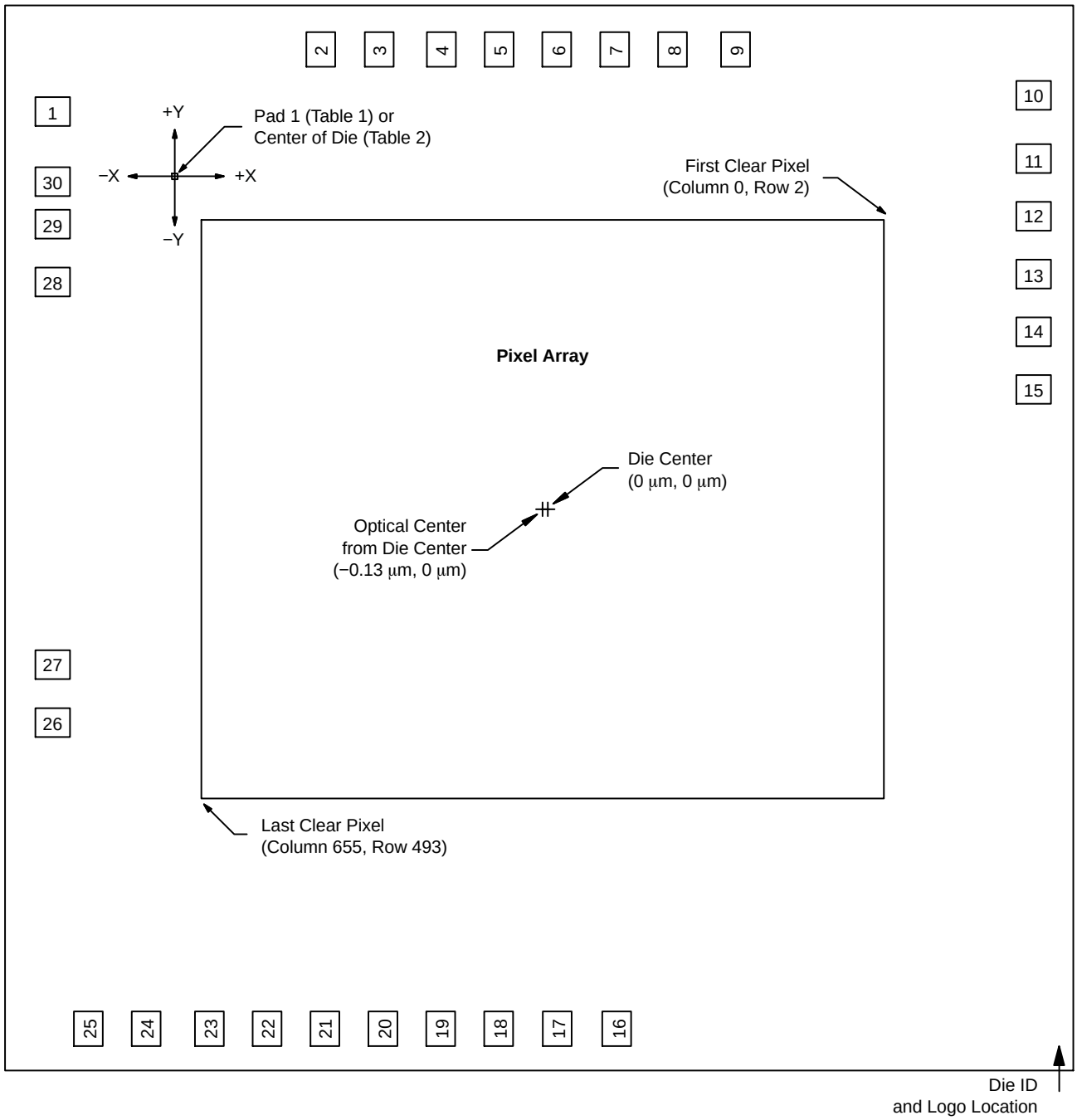


Figure 2. Die Outline (Top View)

Physical Specifications

Table 3. PHYSICAL DIMENSIONS

Feature	Dimensions
Wafer Diameter	200 mm (8″)
Die Thickness	200 μm ±12 μm
Singulated Die Size Width Length	 2711.55 μm ±25 μm 2711.55 μm ±25 μm
Bond Pad Size (MIN)	85 μm × 100 μm
Passivation Openings (MIN)	75 μm × 90 μm
Minimum Bond Pad Pitch	149.63 μm
Optical Array Optical Center from Die Center Optical Center from Center of Pad 1	 X = −0.13 μm, Y = 0 μm X = 1273.38 μm, Y = 1111.93 μm
First Clear Pixel (Column 0, Row 2) From Die Center From Center of Pad 1	 X = 573.00 μm, Y = 429.60 μm X = 1846.50 μm, Y = 682.33 μm
Last Clear Pixel (Column 655, Row 493) From Die Center From Center of Pad 1	 X = −573.10 μm, Y = 429.60 μm X = 700.40 μm, Y = 1541.53 μm

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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