MT9V127

MT9V127 1/4-Inch Color CMOS NTSC/PAL Digital Image SOC with Overlay Processor

ON Semiconductor®

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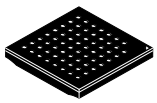

IBGA63 9x9
CASE 503AL

Table 1. KEY PARAMETERS

Parameter	Typical Value
Pixel Size and Type	5.6 μm × 5.6 μm Active Pinnedphotodiode with High−sensitivity Mode for Low−light Conditions
Sensor Format	680 (H) × 512 (V) (includes ±2.5% of Rows and Columns for Lens Alignment)
NTSC Output	720 H × 480 V
PAL Output	720 H × 576 V
Imaging Area	Total Array Size: 3.584 mm x 2.688 mm
Optical Format	$^1/_4$−inch
Frame Rate	50/60 Fields/sec
Sensor Scan Mode	Progressive Scan
Color Filter Array	RGB Standard Bayer
Shutter Type	Electronic Rolling Shutter (ERS)
Automatic Functions	Exposure, White Balance, Black Level Offset Correction, Flicker Avoidance, Color Saturation Control, On−the−fly Defect Correction, Aperture Correction
Programmable Controls	Exposure, White Balance, Horizontal and Vertical Blanking, Color, Sharpness, Gamma Correction, Lens Shading Correction, Horizontal and Vertical Image Flip, Zoom, Windowing, Sampling Rates, GPIO Control

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

Features

- Low−power CMOS Image Sensor with Integrated Image Flow Processor (IFP) and Video Encoder
- 1/4−inch Optical Format, VGA Resolution (640 (H) × 480 (V))
- ±2.5% Additional Columns and Rows to Compensate for Lens Alignment Tolerances
- Integrated Video Encoder for NTSC/PAL with Overlay Capability and 10−bit I−DAC
- Overlay Generator for Dynamic Bitmap Overlay
- Integrated Video Encoder for NTSC/PAL with Overlay Capability and 10−bit I−DAC

Features (continued)

- Integrated Microcontroller for Flexibility
- On−chip Image Flow Processor Performs Sophisticated Processing, Such as Color Recovery and Correction, Sharpening, Gamma, Lens Shading Correction, On−the−fly Defect Correction, Auto White Balancing, and Auto Exposure
- Auto Black Level Calibration
- 10−bit, On−chip Analog−to−digital Converter (ADC)
- Internal Master Clock Generated by On−chip Phaselocked Loop (PLL)
- Two−wire Serial Programming Interface
- Interface to Low−cost Flash through SPI Bus
- High−level Host Command Interface
- Stand Alone Operation Support
- Comprehensive Tool Support for Overlay Generation and Lens Correction Setup
- Development System with DevWare
- Overlay Generation and Compilation Tools

Applications

- Automotive Rearview Camera and Side Mirror
- Blind Spot and Surround View

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Table 2. KEY PARAMETERS (continued)

Parameter		Typical Value
Overlay Support (Note 1)		Utilizes SPI interface to load overlay data from external flash/EEPROM memory with the following features: – Overlay Size 360 x 480 pixel rendered into 720 x 480 pixel display format – Up to four (4) overlays may be blended simultaneously – Selectable readout: Rotating order user selected – Dynamic scenes by loading pre–rendered frames from external memory – Palette of 32 colors out of 64,000 – 8 colors per bitmap – Blend factor dynamically programmable for smooth transitions – Fast Update rate of up to 30 fps – Every bitmap object has independent x/y position – Statistic Engine to calibrate optical alignment – Number Generator
External Overlay Processing Support		Digital input to on–chip NTSC encoder allows for external overlay, processing by a DSP, or FPGA
Windowing		Programmable to any size
Max Analog Gain		0.5–16x
ADC		10–bit, on–chip
Output Interface		Analog composite video out, single–ended or differential; 8–, 10–bit parallel digital output
Output Data Formats (Note 1)		Digital: Raw Bayer 8–,10–bit, CCIR656, 565RGB, 555RGB, 444RGB
Data Rate		Parallel: 27 MB/s
		NTSC: 60 fields/sec
		PAL: 50 fields/sec
Control Interface		Two–wire I/F for register interface plus high–level command exchange. SPI port to interface to external memory to load overlay data, register settings, or firmware extensions.
Input Clock for PLL		27 MHz
SPI Clock Frequencies		4.5 – 9.0 – 18 MHz, programmable
Supply Voltage		Analog: 2.8 V ±5%
		Core: 1.8 V ±5%
		IO: 2.8 V ±5%
Power Consumption		Full resolution at 60 fps: <350 mW[2]
Package		63–BGA, 9 mm x 9 mm, 1 mm pin pitch
Ambient Temperature		Operating: –40°C to 105°C
		Functional: –40°C to +85°C
		Storage: –50°C to +150°C
Dark Current		< 200 e/s at 60°C with a gain of 1
Fixed Pattern Noise	Column	< 2%
	Row	< 2%
Responsivity		17.2 V/lux–s at 550 nm
Signal to Noise Ratio (S/N)		46 dB
Pixel Dynamic Range		74.8 dB

1. Graphical overlay is available only in CCIR656 output format.
2. Analog output enabled; parallel output disabled.

ORDERING INFORMATION

Table 3. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
MT9V127IA3XTC−DP1	VGA 1/4” SOC	Dry Pack with Protective Film
MT9V127IA3XTC−DR1	VGA 1/4” SOC	Dry Pack with Protective Film
MT9V136W00STCK22BC1−750	VGA 1/4” CIS SOC	Tape & Reel with Protective Film
MT9V127IA3XTC−TR	VGA 1/4” CIS SOC	Tape & Reel with Protective Film

NEW FEATURES

Integrated Video Encoder for PAL/NTSC with Overlay Capability

- Composite analog output (NTSC/PAL)
- 8−bit parallel digital output ITU−R BT.656 format
- Raw Bayer format
- Digital input to on−chip NTSC encoder to allow additional processing functions by external DSP or FPGA

On−Chip Overlay Generator

- Static and dynamic overlay graphics with four overlay planes plus number plane
- Support for serial SPI memory up to 16 megabytes
- Number generator
- Overlay blending and x/y positioning
- Overlay position adjustment and statistics engine to calibrate overlay
- Overlay support utilizes SPI interface to load overlay data from external Serial Flash/EEPROM to support the following features:
  - Overlay size 360 x 480 pixel rendered into 720 x 480 pixel display format
  - Up to four overlays may be blended simultaneously
  - Selectable readout: rotating order user selected
  - Dynamic scenes by loading pre−rendered frames from external memory
  - Palette of 32 colors out of 64,000
  - Eight colors per bitmap
  - Blend factor dynamically programmable for smooth transitions
  - Fast update rate of up to 30 fps
  - Every bitmap object has independent x/y position
  - Statistics engine to calibrate optical alignment
  - External overlay processing supports digital input to on−chip NTSC encoder; this enables external overlay processing by a DSP or FPGA

GENERAL DESCRIPTION

The ON Semiconductor MT9V127 is a VGA−format, single−chip CMOS active−pixel digital image sensor for automotive applications. It captures high−quality color images at VGA resolution and outputs NTSC or PAL interlaced composite video.

The VGA CMOS image sensor features ON Semiconductor's breakthrough low−noise CMOS imaging technology that achieves near−CCD image quality (based on signal−to− noise ratio and low−light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of ON Semiconductor's advanced active pixel CMOS process technology.

The MT9V127 is a complete camera−on−a−chip. It incorporates sophisticated camera functions on−chip and is programmable through a simple two−wire serial interface or by an attached SPI Flash memory that contains setup information that may be loaded automatically at startup.

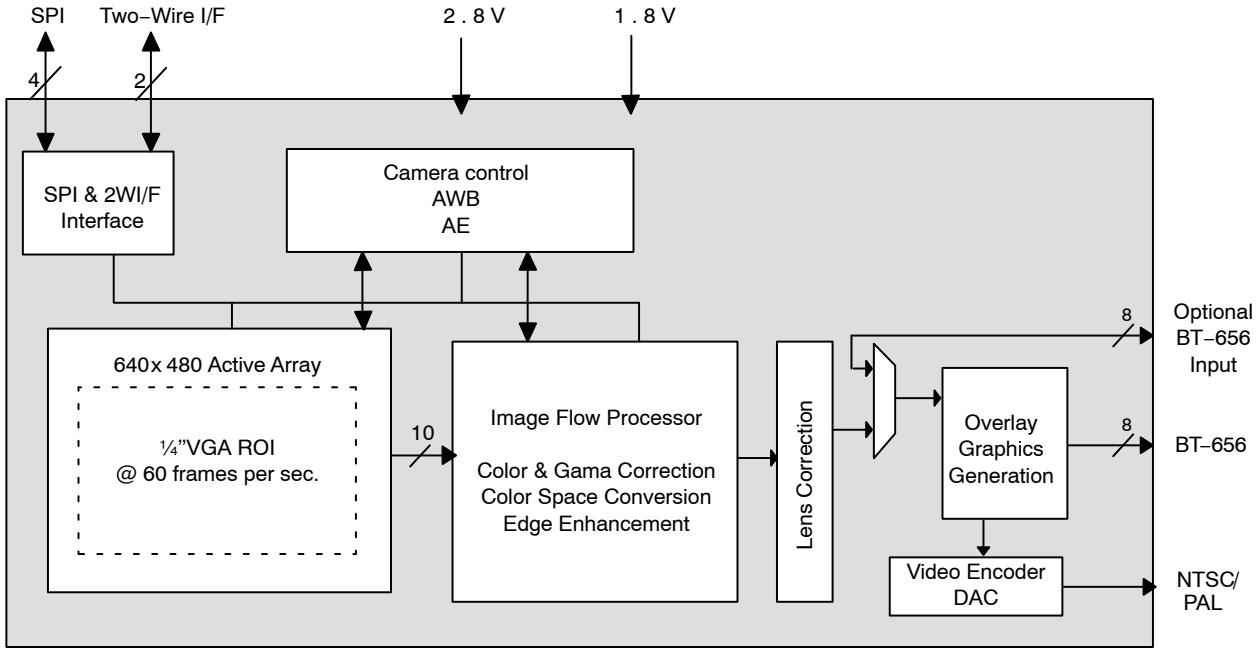
The MT9V127 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, 50 Hz/60 Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on−the−fly defect identification and correction.

The MT9V127 outputs interlaced−scan images at 30 or 25 fps, supporting both NTSC and PAL video formats. The image data can be output on one or two output ports:

- Composite analog video (single−ended and differential output support)
- Parallel 8−, 10−bit digital

ARCHITECTURE

Internal Block Diagram



NOTE: The active array is smaller than the sensor array.

Figure 1. Internal Block Diagram

SYSTEM BLOCK DIAGRAM

The system block diagram will depend on the application. The system block diagram in Figure 2 shows all components; optional peripheral components are highlighted.

Control information will be received by a microcontroller through the automotive bus, such as LIN or CAN bus, to communicate with the MT9V127 through its two−wire serial bus. Optional components will vary by application. For further details, see the MT9V127 Register and Variable Reference.

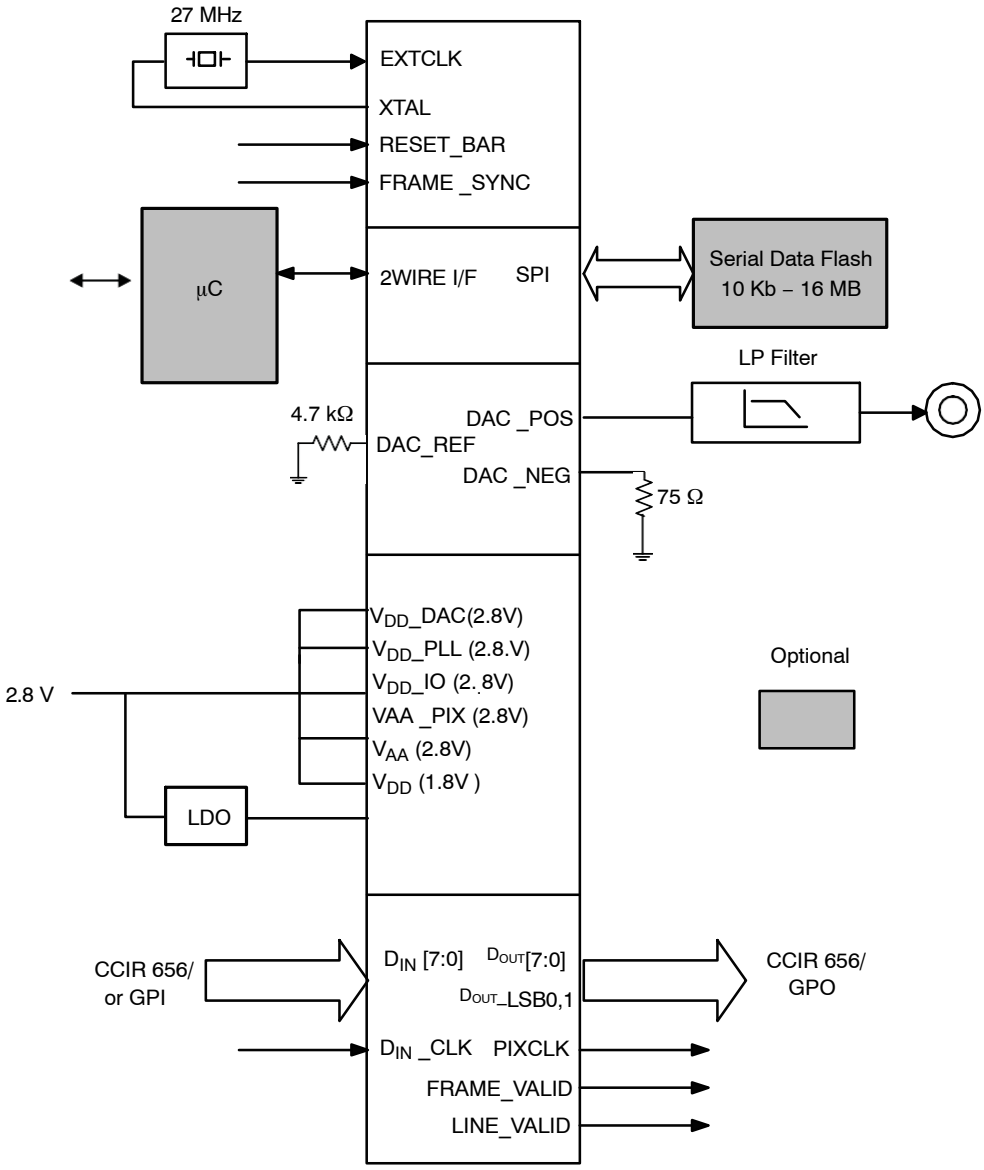


Figure 2. System Block Diagram

Crystal Usage

As an alternative to using an external oscillator, a fundamental 27 MHz crystal may be connected between EXTCLK and XTAL. Two small loading capacitors of 15–22 pF of NPO dielectric should be added as shown in Figure 3.

ON Semiconductor does not recommend using the crystal option for automotive applications above 85°C. A crystal oscillator with temperature compensation is recommended.

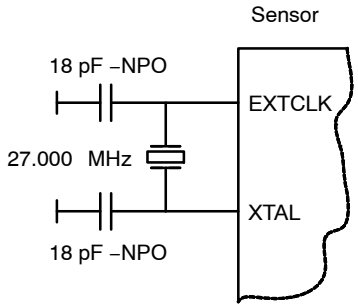


Figure 3. Using a Crystal Instead of an External Oscillator

When using Xtal as the clock source, the internal inverter circuit has a 100 K bias resistor in parallel to Xtal, which can be connected or disconnected by register 0x0014 bit[14].

The clockin_bias_en bit is set to 1 by default.

PIN DESCRIPTIONS AND ASSIGNMENTS

Table 4. PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
CLOCK AND RESET			
B1	EXTCLK	Input	Master input clock (27 MHz): This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected) or connected directly to a crystal
B2	XTAL	Output	If EXTCLK is connected to one pin of a crystal, this signal is connected to the other pin; otherwise this signal must be left unconnected
C1	RESET_BAR	Input	Asynchronous active−low reset: When asserted, the device will return all interfaces to their reset state. When released, the device will initiate the boot sequence
C2	FRAME_SYNC	Input	This input can be used to set the output timing of the MT9V127 to a fixed point in the frame. The input buffer associated with this input is permanently enabled. This signal should be connected to GND if not used
REGISTER INTERFACE			
G3	SCLK	Input	These two signals implement serial communications protocol for access to the internal registers and variables
H3	SDATA	Input/OD	
H2	SADDR	Input	This signal controls the device ID that will respond to serial communication commands Two−wire serial interface device ID selection: 0: 0x90 1: 0xBA
SPI INTERFACE			
H5	SPI_SCLK	Output	Clock output for interfacing to an external SPI memory such as Flash/ EEPROM. Tristate when RESET_BAR is asserted
G5	SPI_SDI	Input	Data in from SPI device. This signal has an internal pull−up resistor
H4	SPI_SDO	Output	Data out to SPI device. Tristate when RESET_BAR is asserted
G4	SPI_CS_N	Output	Chip selects to SPI device. Tristated when RESET_BAR is asserted

Table 4. PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Type	Description
(PARALLEL) PIXEL DATA INPUT			
D1	DIN_CLK	Input	Pixel clock input: Data on DIN[7:0] are sampled at the rising or falling edge of this clock. (Alternatively, an internal sampling clock may be used)
H1, G1, F1, G2, F2, E1, E2, D2	DIN[7:0]	Input	Data coming in on this interface is passed through the overlay blender and to the video encoder output. The input buffers associated with inputs 7 to 0 are powered down by default. This allows these signals to be left unconnected if not required. These inputs can also be used as general purpose inputs
(PARALLEL) PIXEL DATA OUTPUT			
E7	FRAME_VALID	Input/Output	Pixel data from the MT9V127 can be routed out on this interface and processed externally. To save power, these signals are driven to a constant logic level unless the parallel pixel data output or alternate (GPIO) function is enabled for these pins. For more information see Table 16. This interface is disabled by default. The slew rate of these outputs is programmable. These signals can also be used as general purpose input/outputs
E6	LINE_VALID	Input/Output	
E8	PIXCLK	Output	
C7, B6, C8, B7, B8, A6, A7, A8	D_{OUT}[7:0]	Output	
D7	D_{OUT}_LSB1	Input/Output	When the sensor core is running in bypass mode, it will generate 10 bits of output data per pixel. These two pins make the two LSB of pixel data available externally. Leave DOUT_LSB1 unconnected if not used. To save power, these signals are driven to a constant logic level unless the sensor core is running in bypass mode or the alternate function is enabled for these pins. The slew rate of these outputs is programmable. For analog output, the DOUT_LSB0 cannot be left unconnected, and must be strapped to select either NTSC or PAL mode. For more information, see Table 16.
D8	D_{OUT}_LSB0	Input/Output	
COMPOSITE VIDEO OUTPUT			
B3	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single−ended mode. This interface is enabled by default using NTSC/PAL signalling. For applications where composite video output is not required, the video DAC can be placed in a power−down state under software control
A4	DAC_NEG	Output	Negative video DAC output in differential mode. Connect to AGND in single− ended mode
A2	DAC_REF	Output	External reference resistor for the video DAC
MANUFACTURING TEST INTERFACE			
D6	TDI	Input	JTAG Test pin (Reserved for Test Mode)
C6	TDO	Output	JTAG Test pin (Reserved for Test Mode)
F3	TMS	Input	JTAG Test pin (Reserved for Test Mode)
F4	TCK	Input	JTAG Test pin (Reserved for Test Mode)
F5	TRST_N	Input	Connect to GND
F6	ATEST1	Input	Analog test input. Connect to GND in normal operation
G6	ATEST2	Input	Analog test input. Connect to GND in normal operation
POWER			
C3, D3, E3	VDD	Supply	Supply for VDD core: 1.8 V nominal
C5, D5, E5	VDD_IO	Supply	Supply for digital IOs: 2.8 V nominal
A5	VDD_DAC	Supply	Supply for video DAC: 2.8 V nominal
B5	VDD_PLL	Supply	Supply for PLL: 2.8 V nominal
G7, G8	VAA	Supply	Analog power: 2.8 V nominal
F7, F8	VAA_PIX	Supply	Analog pixel array power: 2.8 V nominal. Must be at same voltage potential as V_{AA}
A3	GND_DAC	Supply	Video DAC ground
B4, C4, D4, E4	DGND	Supply	Digital ground
H6, H7, H8	AGND	Supply	Analog ground

Pin Assignments

Pin 1 is not populated with a ball. That allows the device to be identified by an additional marking.

Table 5. PIN ASSIGNMENT

	1	2	3	4	5	6	7	8
A		DAC_REF	GND_DAC	DAC_NEG	V_{DD}_DAC	D_{OUT2}	D_{OUT1}	D_{OUT0}
B	EXTCLK	XTAL	DAC_POS	GND	V_{DD}_PLL	D_{OUT6}	D_{OUT4}	D_{OUT3}
C	RESET_BAR	FRAME_SYNC	V_{DD}	GND	V_{DD}_IO	TDO	D_{OUT7}	D_{OUT5}
D	DIN_CLK	D_{IN0}	V_{DD}	GND	V_{DD}_IO	TDI	DOUT_LSB1	D_{OUT}_LSB0
E	D_{IN2}	D_{IN1}	V_{DD}	GND	V_{DD}_IO	LINE_VALID	FRAME_VALID	PIXCLK
F	D_{IN5}	D_{IN3}	TMS	TCK	TRST_N	ATEST1	VAA_PIX	V_{AA}_PIX
G	D_{IN6}	D_{IN4}	SCLK	SPI_CS_N	SPI_SDI	ATEST2	V_{AA}	V_{AA}
H	D_{IN7}	S_{ADDR}	S_{DATA}	SPI_SDO	SPI_SCLK	A_{GND}	A_{GND}	A_{GND}

Table 6. RESET/DEFAULT STATE OF INTERFACES

Name	Reset State	Default State	Notes
EXTCLK	Clock running or stopped	Clock running	Input
XTAL	N/A	N/A	Input
RESET_BAR	Asserted	De−asserted	Input
SCLK	N/A	N/A	Input. Must always be driven to a valid logic level
SDATA	High impedance	High impedance	Input/Output. A valid logic level should be established by pull−up resistor
SADDR	N/A	N/A	Input. Must always be driven to a valid logic level. Must be permanently tied to VDD_IO or GND
SPI_SCLK	High impedance.	Driven, logic 0	Output. Output enable is R0x0032[9]
SPI_SDI	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up is permanently enabled
SPI_SDO	High impedance	Driven, logic 0	Output enable is R0x0032[9]
SPI_CS_N	High impedance	Driven, logic 1	Output enable is R0x0032[9]
DINCLK	Input buffer powered down	Input buffer powered down	Input. This interface is disabled by default, and the input buffers are powered down. If this interface is not required, these pins can be left unconnected (floating)
DIN7			
DIN6			
DIN5			
DIN4			
DIN3			
DIN2			
DIN1			
DIN0			
FRAME_VALID	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered up, sampled, then powered down again as part of the autoconfiguration mechanism. See Note 4
LINE_VALID			

Table 6. RESET/DEFAULT STATE OF INTERFACES (continued)

Name	Reset State	Default State	Notes
PIXCLK	High impedance	Driven, logic 0	Output. This interface disabled by default. See Note 3
DOUT7			
DOUT6			
DOUT5			
DOUT4			
DOUT3			
DOUT2			
DOUT1			
DOUT0			
DOUT_LSB1	High impedance	High impedance	Input/Output. This interface disabled by default. Input buffers (used for GPIO function) powered down by default, so these pins can be left unconnected (floating). After reset, these pins are powered−up, sampled, then powered down again as part of the auto−configuration mechanism.
DOUT_LSB0	High impedance	Driven, logic 0	
DAC_POS	High impedance	Driven	Output. Interface disabled by hardware reset and enabled by default when the device starts streaming
DAC_NEG			
DAC_REF			
TDI	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TDO	High impedance	High impedance	Output. Driven only during appropriate parts of the JTAG shifter sequence
TMS	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TCK	Internal pull−up enabled	Internal pull−up enabled	Input. Internal pull−up means that this pin can be left unconnected (floating)
TRST_N	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND for normal operation
FRAME_SYNC	N/A	N/A	Input. Must always be driven to a valid logic level. Must be driven to GND for normal operation
ATEST1			Must be driven to GND for normal operation
ATEST2			Must be driven to GND for normal operation

3. The reason for defining the default state as logic 0 rather than high impedance is this: when wired in a system (for example, on our demo boards), these outputs will be connected, and the inputs to which they are connected will want to see a valid logic level. No current drain should result from driving these to a valid logic level (unless there is a pull−up at the system level).
4. These pads have their input circuitry powered down, but they are not output−enabled. Therefore, they can be left floating but they will not drive a valid logic level to an attached device.

SOC DESCRIPTION

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array, an analog readout chain, a 10−bit ADC with programmable gain and black offset, and timing and control as illustrated in Figure 4.

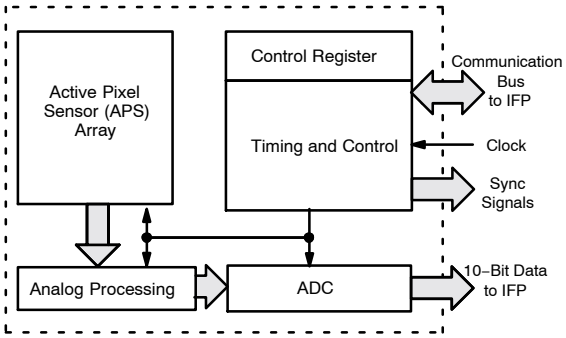


Figure 4. Sensor Core Block Diagram

Pixel Array Structure

The sensor core pixel array is configured as 744 columns by 512 rows, as shown in Figure 5. This includes black rows and columns.

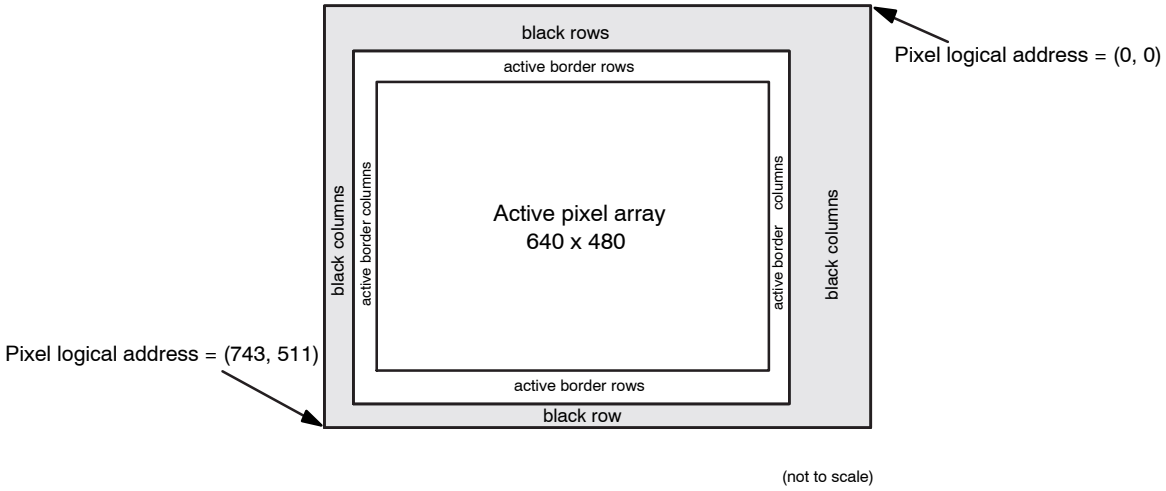


Figure 5. Pixel Array Description

The black row data are used internally for the automatic black level adjustment. However, these black rows can also be read out by setting the sensor to raw data output mode.

There are 744 columns by 512 rows of optically−active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

The one additional active column and two additional active rows are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 6 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right corner. The image is presented in true orientation by the output display.

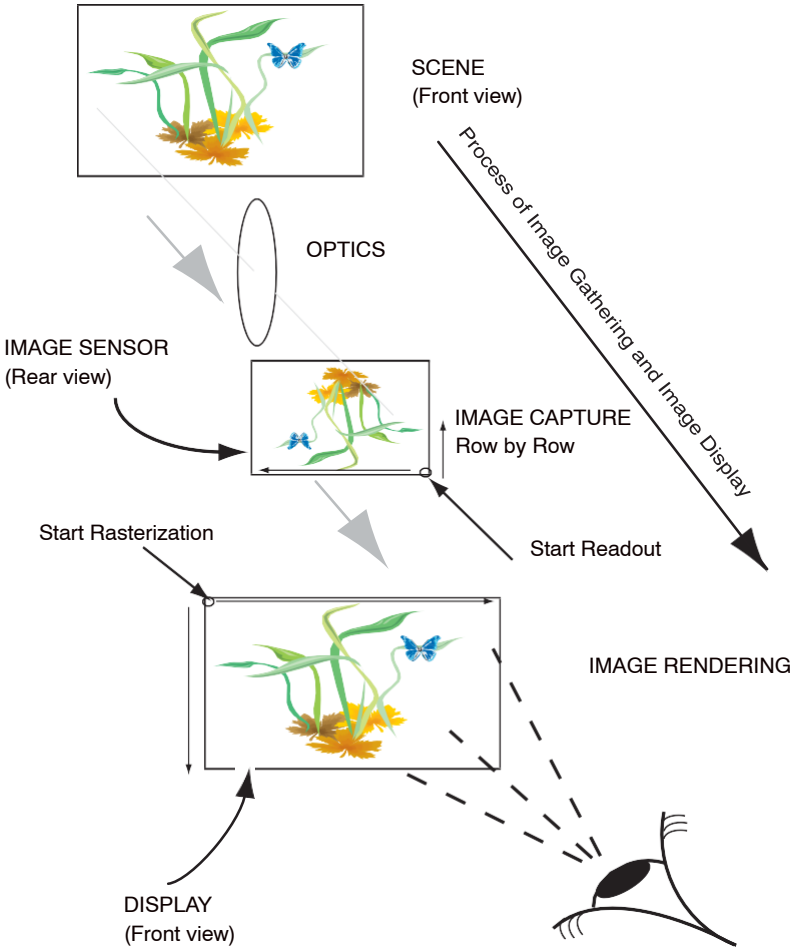


Figure 6. Image Capture Example

SENSOR PIXEL ARRAY

The active pixel array is 640 x 480 pixels. In addition, there are rows and columns for lens alignment and demosaic.

Not shown in Figure 7 are pixels for black level calibration.

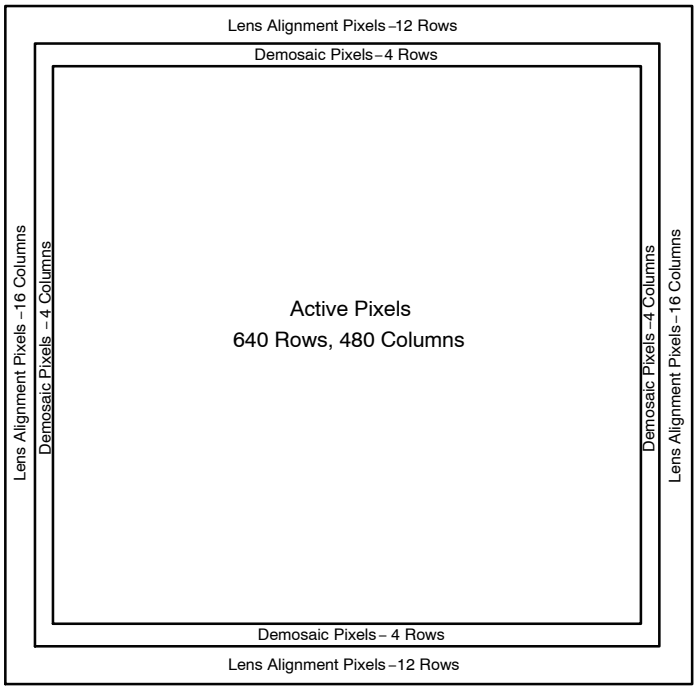


Figure 7. Sensor Pixel Array

The range of adjustment is from Row 0 to 22 and Column 0 to 30. There are 4 rows/ columns needed to calculate the RGB values. The window should be moved only at even numbers.

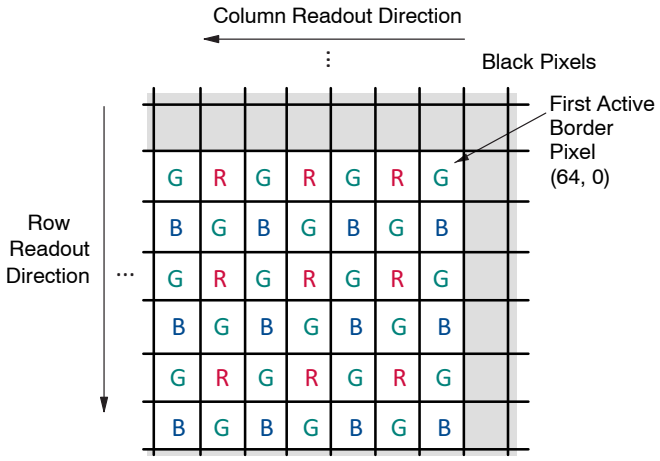


Figure 8. Pixel Color Pattern Detail (Top Right Corner)

Output Data Format

The sensor core image data are read out in progressive scan order. Valid image data are surrounded by horizontal and vertical blanking, shown in Figure 9.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; 240 image pixels and 3 dark pixels that are located at the bottom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field.

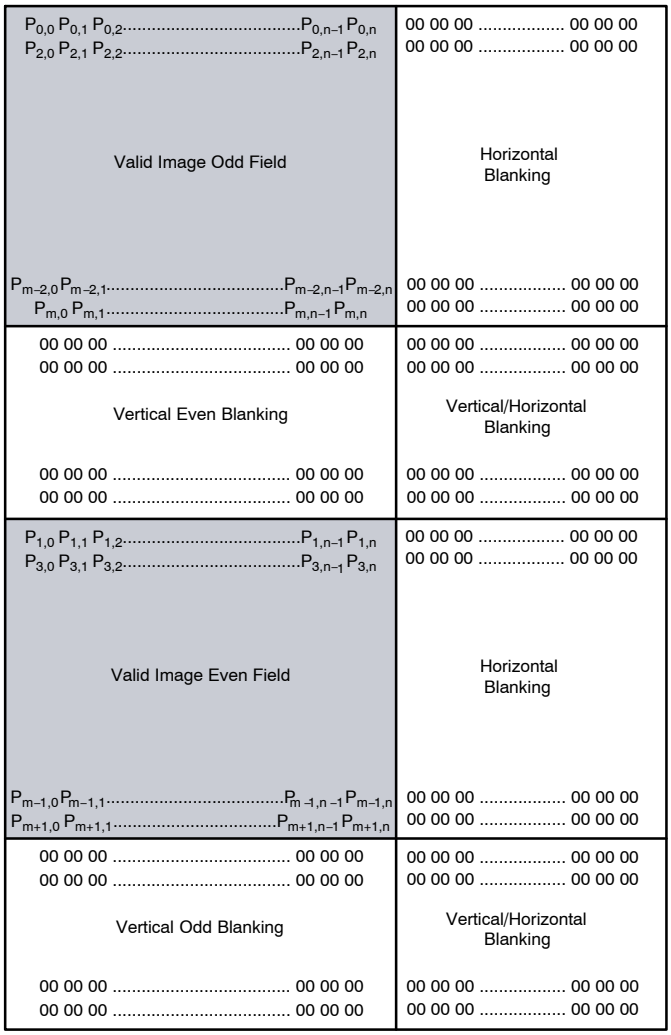


Figure 9. Spatial Illustration of Image Readout

Image Flow Processor

Image and color processing in the MT9V127 are implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operation parameters. The IFP is broken down into different sections, as outlined in Figure 10.

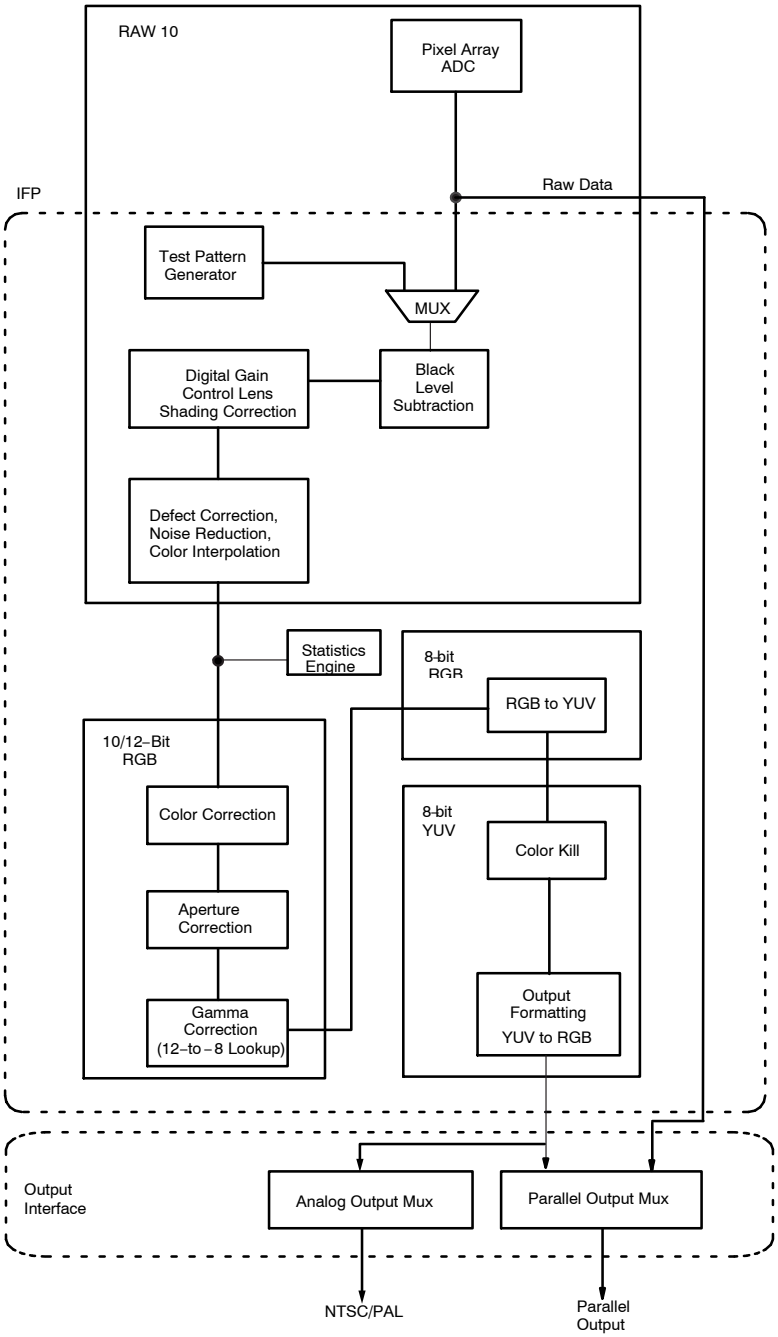


Figure 10. Color Pipeline

Test Patterns

During normal operation of the MT9V127, a stream of raw image data from the sensor core is continuously fed into the color pipeline. For test purposes, this stream can be replaced with a fixed image generated by a special test module in the pipeline. The module provides a selection of test patterns sufficient for basic testing of the pipeline.

Test patterns are accessible by programming a register and are shown in Figure 11. ON Semiconductor recommends disabling the MCU before enabling test patterns.

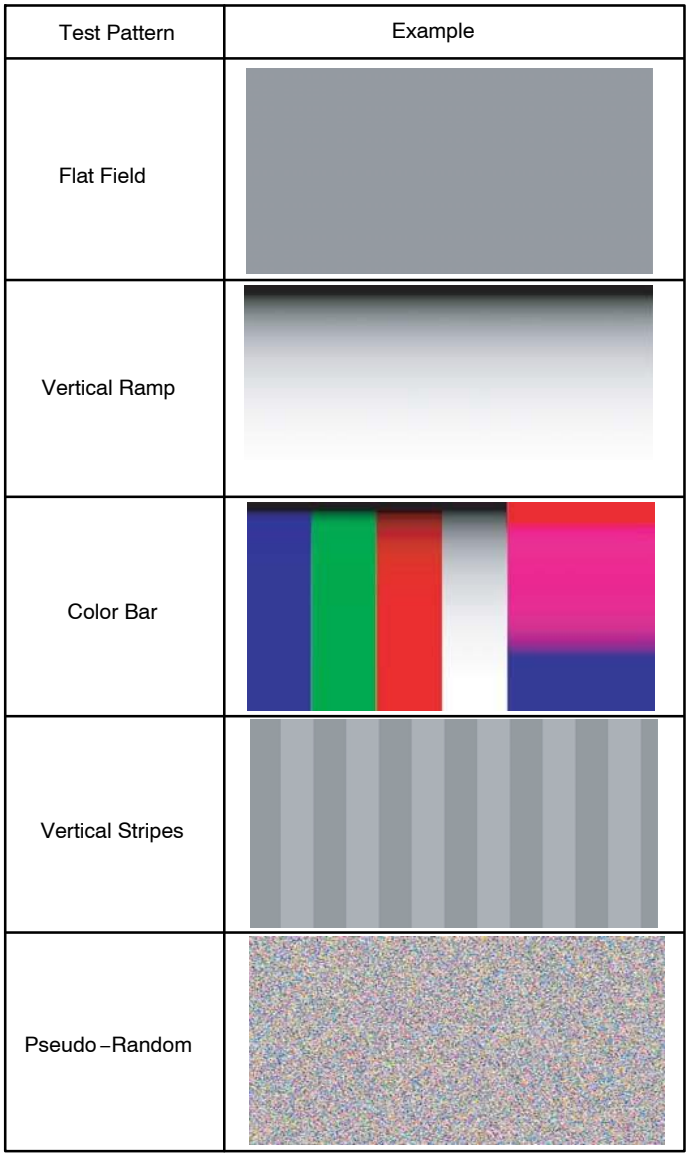


Figure 11. Color Bar Test Pattern

NTSC/PAL Test Pattern Generation

There is a built−in standard EIA (NTSC) and EBU (PAL) color bars to support hue and color saturation characterization. Each pattern consists of seven color bars (white, yellow, cyan, green, magenta, red, and blue). The Y, Cb and Cr values for each bar are detailed in Tables 7 and 8.

The test pattern is invoked through a Host Command call to the TX Manager. See the MT9V127 Host Command Specification.

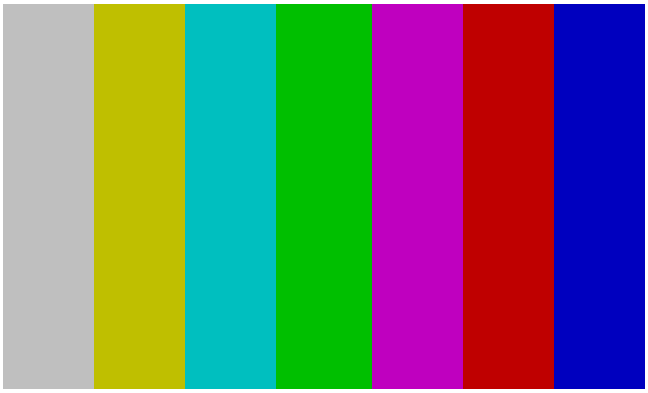


Figure 12. Color Bars

Table 7. EIA COLOR BARS (NTSC)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	180	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

Table 8. EBU COLOR BARS (PAL)

	Nominal Range	White	Yellow	Cyan	Green	Magenta	Red	Blue
Y	16 to 235	235	162	131	112	84	65	35
Cb	16 to 240	128	44	156	72	184	100	212
Cr	16 to 240	128	142	44	58	198	212	114

CCIR−656 Format

The color bar data is encoded in 656 data streams. The duration of the blanking and active video periods of the generated 656 data are summarized in the following tables.

Table 9. NTSC

Line Numbers	Field	Description
1−3	2	Blanking
4−19	1	Blanking
20−263	1	Active video
264−265	1	Blanking
266−282	2	Blanking
283−525	2	Active Video

Table 10. PAL

Line Numbers	Field	Description
1–22	1	Blanking
23–310	1	Active video
311–312	1	Blanking
313–335	2	Blanking
336–623	2	Active video
624–625	2	Blanking

Black Level Subtraction and Digital Gain

Image stream processing starts with black level subtraction and multiplication of all pixel values by a programmable digital gain. Both operations can be independently set to separate values for each color channel (R, Gr, Gb, B). Independent color channel digital gain can be adjusted with registers. Independent color channel black level adjust− ments can also be made. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The MT9V127 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The Correction Function

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{correncted}(row,\ col) = P_{sensor}(row,\ col) \times f(row,\ col) \quad \text{(eq. 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10−bit integer number, which can be considered proportional to the pixel's response to a one−color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one−color−per−pixel nature of the data stream, but after the defect correction it must be converted to a three−colors−per−pixel stream appropriate for standard color processing. The conversion is done by an edge−sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10−bit numbers. Since such sums can have up to 12 significant bits, the bit width of the image data stream is widened to 12 bits per color (36 bits per pixel). The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color−corrected image data. The gain and threshold for 2D correction can be defined through register settings.

Gamma Correction

The MT9V127 IFP includes a block for gamma correction that can adjust its shape based on brightness to enhance the performance under certain lighting conditions. Two custom gamma correction tables may be uploaded corresponding to a brighter lighting condition and a darker lighting condition. At power−up, the IFP loads the two tables with default values. The final gamma correction table used depends on the brightness of the scene and takes the form of an interpolated version of the two tables.

The gamma correction curve (as shown in Figure 13) is implemented as a piecewise linear function with 19 knee points, taking 12−bit arguments and mapping them to 8−bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096. The 8−bit ordinates are programmable through IFP registers.

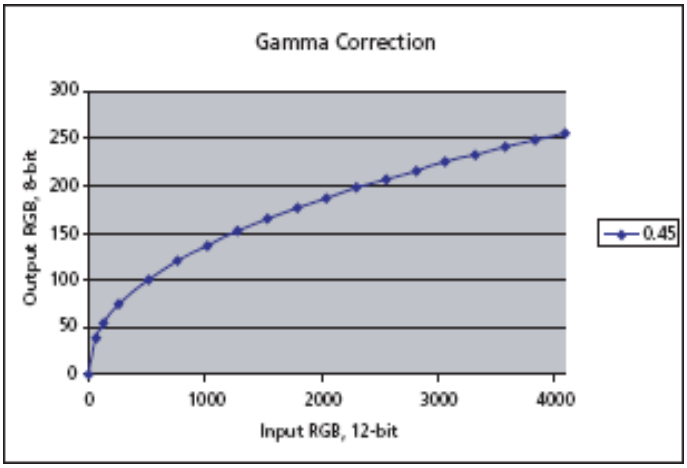


Figure 13. Gamma Correction Curve

RGB to YUV Conversion

For further processing, the data is converted from RGB color space to YUV color space.

Color Kill

To remove high−or low−light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one−dimensional low−pass filtering of Y and/or UV signals is possible. A 3− or 5−tap filter can be selected for each signal.

YUV−to−RGB/YUV Conversion and Output Formatting

The YUV data stream emerging from the scaling module can either exit the color pipe− line as−is or be converted before exit to an alternative YUV or RGB data format.

Output Format and Timing

YUV/RGB Data Ordering

The MT9V127 supports swapping YCbCr mode, as illustrated in Table 11.

Table 11. YCbCr OUTPUT DATA ORDERING

Mode	Data Sequence			
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CbCr	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CbCr, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

The RGB output data ordering in default mode is shown in Table 12. The odd and even bytes are swapped when luma/chroma swap is enabled. R and B channels are bit−wise swapped when chroma swap is enabled.

Table 12. RGB ORDERING IN DEFAULT MODE

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$
555RGB	Odd	0 $R_7R_6R_5R_4R_3G_7G_6$
	Even	$G_5G_4G_3B_7B_6B_5B_4B_3$
444xRGB	Odd	$R_7R_6R_5R_4G_7G_6G_5G_4$
	Even	$B_7B_6B_5B_4$ 0 0 0 0
x444RGB	Odd	0 0 0 0 $R_7R_6R_5R_4$
	Even	$G_7G_6G_5G_4B_7B_6B_5B_4$

Uncompressed 10−Bit Bypass Output

Raw 10−bit Bayer data from the sensor core can be output in bypass mode in two ways:

- Using 8 data output signals (D_{OUT}[7:0]) and GPIO[1:0]. The GPIO signals are the least significant 2 bits of data
- Using only 8 signals (D_{OUT}[7:0]) and a special 8 + 2 data format, shown in Table 13

Table 13. 2−BYTE BAYER FORMAT

Byte	Bits Used	Bit Sequence
Odd bytes	8 data bits	D9D8D7D6D5D4D3D2
Even bytes	2 data bits + 6 unused bits	0 0 0 0 0 0 D_1D_0

Readout Formats

Progressive format is used for raw Bayer output.

Output Formats

ITU−R BT.656 and RGB Output

The MT9V127 can output processed video as a standard ITU−R BT.656 (CCIR656) stream, an RGB stream, or as unprocessed Bayer data. The ITU−R BT.656 stream contains YCbCr 4:2:2 data with fixed embedded synchronization codes. This output is typically suitable for subsequent display by standard video equipment or JPEG/MPEG compression.

Colorpipe data (pre−lens correction and overlay) can also be output in YCbCr 4:2:2 and a variety of RGB formats in 640 by 480 progressive format in conjunction with LINE_VALID and FRAME_VALID.

The MT9V127 can be configured to output 16−bit RGB (565RGB), 15−bit RGB (555RGB), and two types of 12−bit RGB (444RGB). Refer to Table 29 and Table 30 for details.

Bayer Output

Unprocessed Bayer data are generated when bypassing the IFP completely—that is, by simply outputting the sensor Bayer stream as usual, using FRAME_VALID, LINE_VALID, and PIXCLK to time the data. This mode is called sensor stand−alone mode.

Output Ports

Composite Video Output

The composite video output DAC is external−resistor−programmable and supports both single−ended and differential output. The DAC is driven by the on−chip video encoder output.

Parallel Output

Parallel output uses either 8−bit or 10−bit output. Eight−bit output is used for ITU−R BT.656 and RGB output. Ten−bit output is used for raw Bayer output.

USAGE MODES

How a camera based on the MT9V127 will be configured depends on what features are used. In the simplest case, only an MT9V127 plus an external flash memory, or an 8−bit microcontroller (°C) might be sufficient. A back−up camera with dynamic input from the steering system will require a °C with a system bus interface such as a CAN bus or a LIN bus. Flash sizes vary depending on the data for registers, firmware, and overlay data − somewhere between 10 Kb to 16 MB. The two−wire bus is adequate since only high−level commands are used to invoke overlays, load registers from memory, or set up lens correction parameters. Overlay data can alternatively be issued by the external °C if the rate of refreshing data is deemed adequate. If there are no commands in the Flash image the device can be in auto configuration mode by which the sensor is set up according to the status of pins FRAME_VALID, LINE_VALID and D_{OUT}_LSB0. For further information, see "Auto−Configuration".

In the simplest case no Flash memory or °C is required, as shown in Figure 14. This is truly a single chip operation.

NOTE: Because mandatory patches must be loaded, the Auto−Config mode is not recommended.

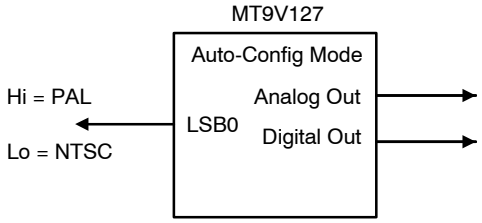


Figure 14. Auto−config Mode

The MT9V127 can be configured by a serial Flash through the SPI Interface.

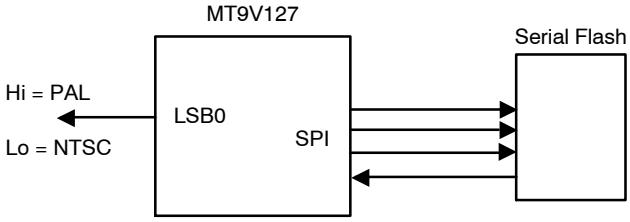


Figure 15. Flash Mode

Overlay functions can also be assigned to general purpose inputs. For instance, a proximity sensor would call up a warning message. That capability can be employed on all configurations with external Flash memory by mapping overlay images to an input.

Alternatively, the °C may poll these inputs to create an action such as a new overlay as shown in Figure 16.

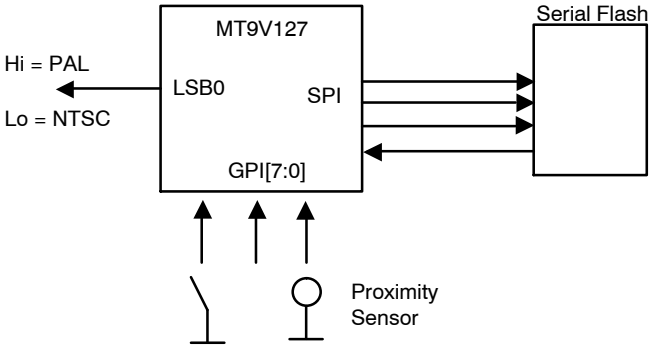


Figure 16. Usage Mode 3

Typically, an automotive bus such as CAN or LIN bus will be connected to a rear−view camera for the purpose of dynamically providing steering information that will in turn be translated into overlay images being called by the °C as shown in Figure 17.

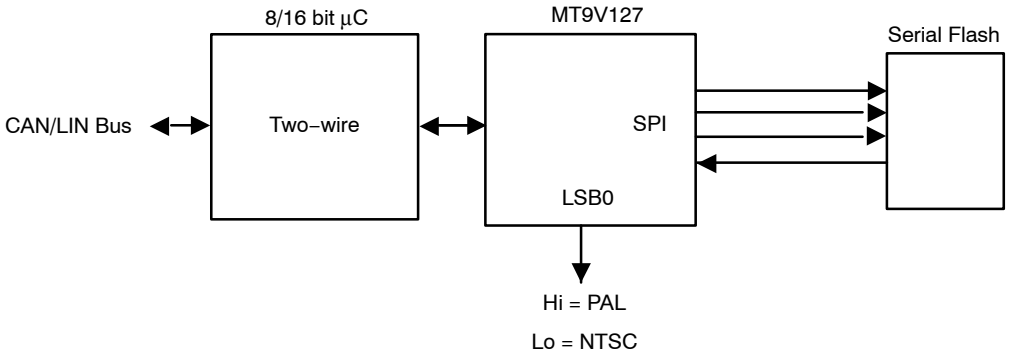


Figure 17. Host Mode with Flash

Overlay information may also be passed by the °C without a need for a Flash memory. However, because the data transfer rate is limited over the two−wire serial bus, the update rate may be slower. However, if overlay images are preloaded into the four on− chip buffers, they may be turned on and off or move location at the frame rate as shown in Figure 18.

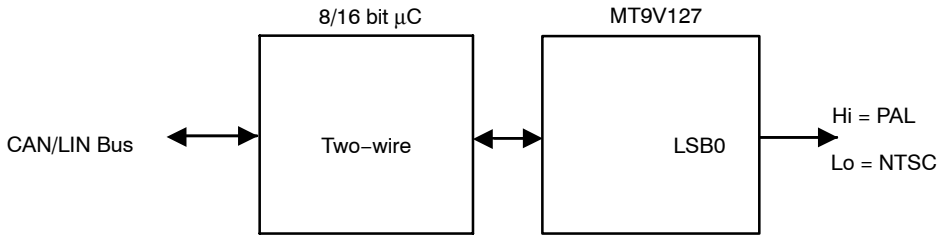


Figure 18. Host Mode

EXTERNAL OVERLAY

In addition to the on−chip overlay generator, an externally generated overlay may be superimposed onto the video output.

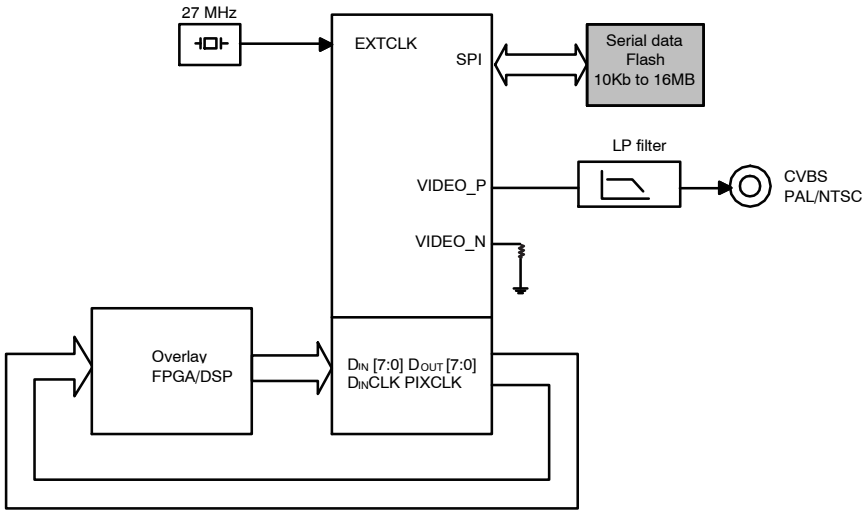


Figure 19. External Overlay System Block Diagram

MULTICAMERA SUPPORT

Two or more MT9V127 sensors may be synchronized to a frame by asserting the FRAME_SYNC signal. At that point, the sensor and video encoder will reset without affecting any register settings. The MT9V127 may be triggered to be synchronized with another MT9V127 or an external event.

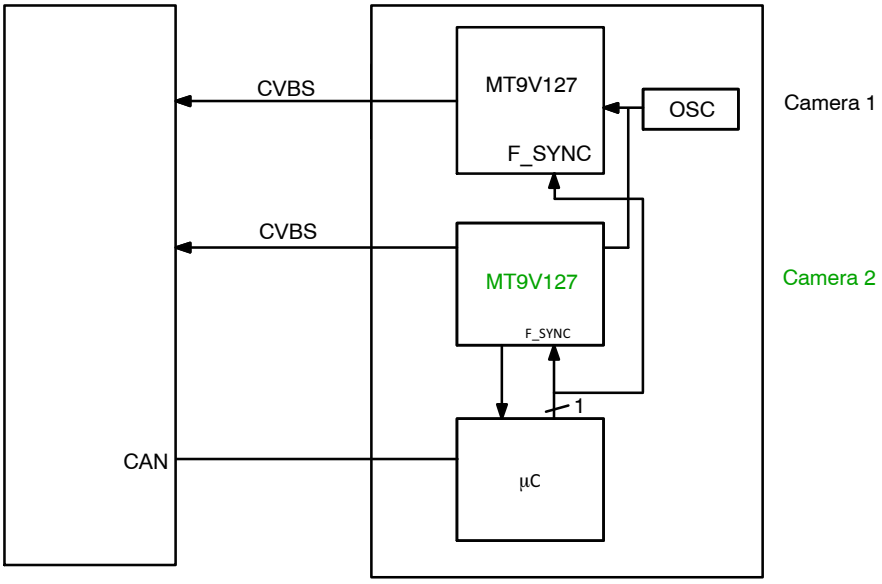


Figure 20. Multicamera System Block Diagram

EXTERNAL SIGNAL PROCESSING

An external signal processor can take data from ITU656 or raw Bayer output format and post−process or compress the data in various formats.

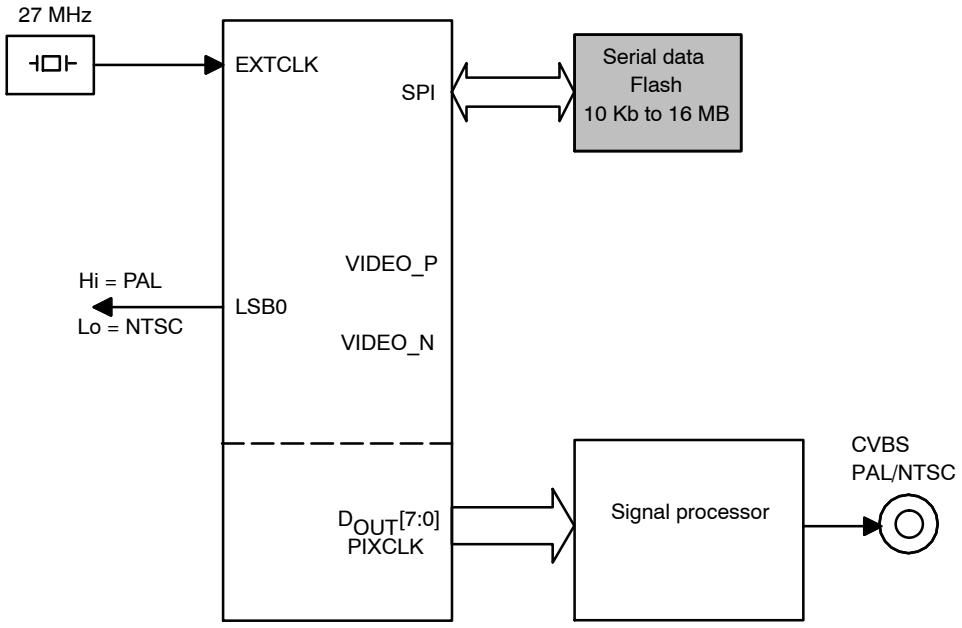


Figure 21. External Signal Processing Block Diagram

Device Configuration

After power is applied and the device is out of reset by de−asserting the RESET_BAR pin, it will enter a boot sequence to configure its operating mode. There are essentially four modes, two when Flash is present and two when Flash is not present. Figure 22: “Power−Up Sequence – Configuration Options Flow Chart,” contains more details on the configuration options.

If Flash is present and:

- A valid Flash device identifier is detected AND the Flash device contains valid configuration records, then
  - Disable Auto−Config
  - Parse Flash Content
  - Load Flash Configuration −>Flash Configuration Mode
- A valid Flash device identifier is detected BUT the Flash device DOES NOT contain valid configuration records, then
  - Enter Auto Configuration

If Flash is not present and:

- SPI_SDI == 0, then
  - Enter Host Configuration
- SPI_SDI != 0, then
  - Enter Auto Configuration

Auto−Configuration

The device supports an auto−configuration feature. During system start−up, the device first detects whether an SPI Flash device is attached to the MT9V127. If not, it will then sample the state of a number of GPI inputs including FRAME_VALID, LINE_VALID and D_{OUT}_LSB0. For more information, see Table 16, “GPIO Bit Descriptions”. The state of these inputs then determines the configuration of a number of subsystems of the device such as readout mode, pedestal and video format, respectively.

The auto−configuration feature can be disabled by grounding the SPI_DIN pin. The device samples the state of this pin during the Flash device detection process. If no SPI Flash device is detected (read device ID of 0x00 or 0xFF), OR the SPI_DIN pin is grounded, then auto−configuration is disabled.

Flash Configuration Mode

If a valid Flash is detected (by reading device ID other than 0x00 or 0xFF) and the flash device contains valid configuration records, then these configuration records are processed.

Host Configuration

This mode is entered if the SPI_DIN pin is grounded. The SOC performs no configuration, and remains idle waiting for configuration and instruction from the host.

Power Sequence

In power−up, the core voltage (1.8 V) must trail the IO (2.8 V) by a positive number. All 2.8 V rails can be turned on at the same time or follow the power−up sequence in Figure 50: “Power Up Sequence”.

In power down, the sequence is reversed. The core voltage (1.8 V) must be turned off before any 2.8 V. Refer to Figure 51: “Power Down Sequence”, for details.

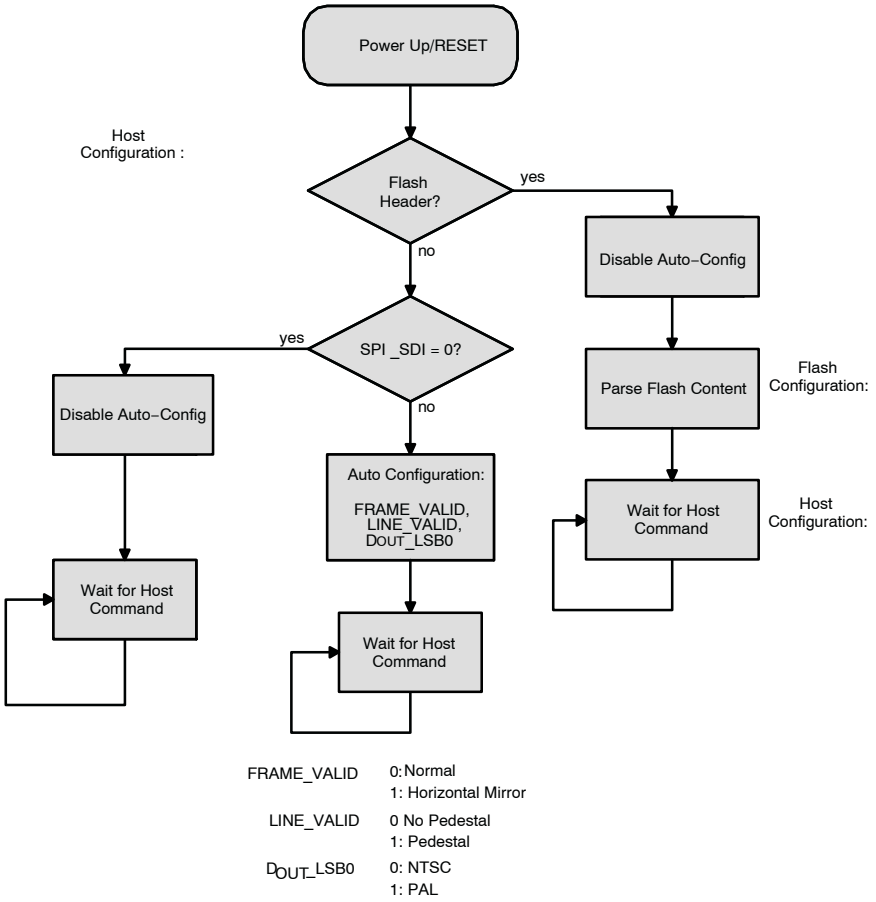


Figure 22. Power−Up Sequence – Configuration Options Flow Chart

Supported SPI Devices

Table 14 lists supported Flash devices. Devices not compatible will require a firmware patch. Contact ON Semiconductor for additional support.

Table 14. SPI FLASH DEVICES

Type	Density	Manufacturer	Device	Speed (MHz)	Standard	Temp Range (μF)	Supported
Flash	8 MB	Atmel	AT26DF081A	70	JEDEC/Device ID	−20 to +85	Yes
Flash	1 MB	ST	M25P10−AVMB3	50		−40 to +125	Yes

Supported SPI Commands

The SPI commands shown in Table 15 are supported by the MT9V127.

Table 15. SPI COMMANDS SUPPORTED

Command	Value
Read Array	0x03
Block Erase	0xD8
Chip Erase	0xC7
Read Status	0x05
Write status	0x01
Byte Page Program	0x02
Write Enable	0x06
Write Disable	0x04
Read Manufacturer and Device ID	0x9F
(Fast) Read Array	0x0B

Table 16. GPIO BIT DESCRIPTIONS

	GPI[2] (D_{OUT}_LSB0)	GPI[1] (FRAME_VALID)	GPI[0] (LINE_VALID)
Low (“0”)	NTSC	Normal	No pedestal
High (“1”)	PAL	Horizontal mirror	Pedestal

Host Command Interface

ON Semiconductor's sensors and SOCs contain numerous registers that are accessed through a two−wire interface with speeds up to 400 kHz.

The MT9V127, in addition to writing or reading straight to/from registers or firmware variables, has a mechanism to write higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on chip firmware and the results are reported back. In general, registers shall not be accessed with the exception of registers that are marked for "User Access."

Flash memory is also available to store commands for later execution. Under DMA control, a command is written into the SOC and executed.

For a complete spec on host commands, refer to the MT9V127 Host Command Interface Specification.

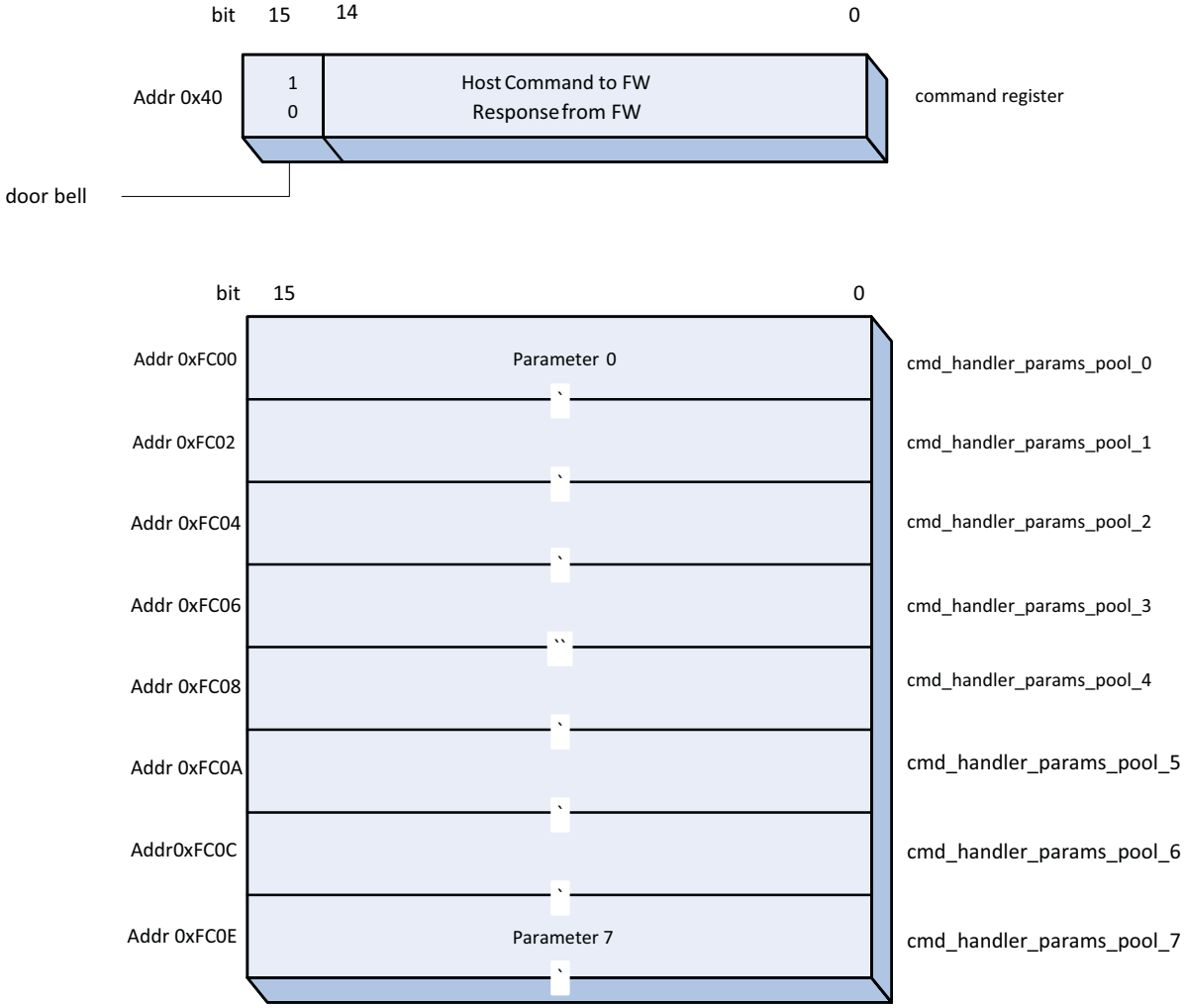


Figure 23. Interface Structure

Host Command Process Flow

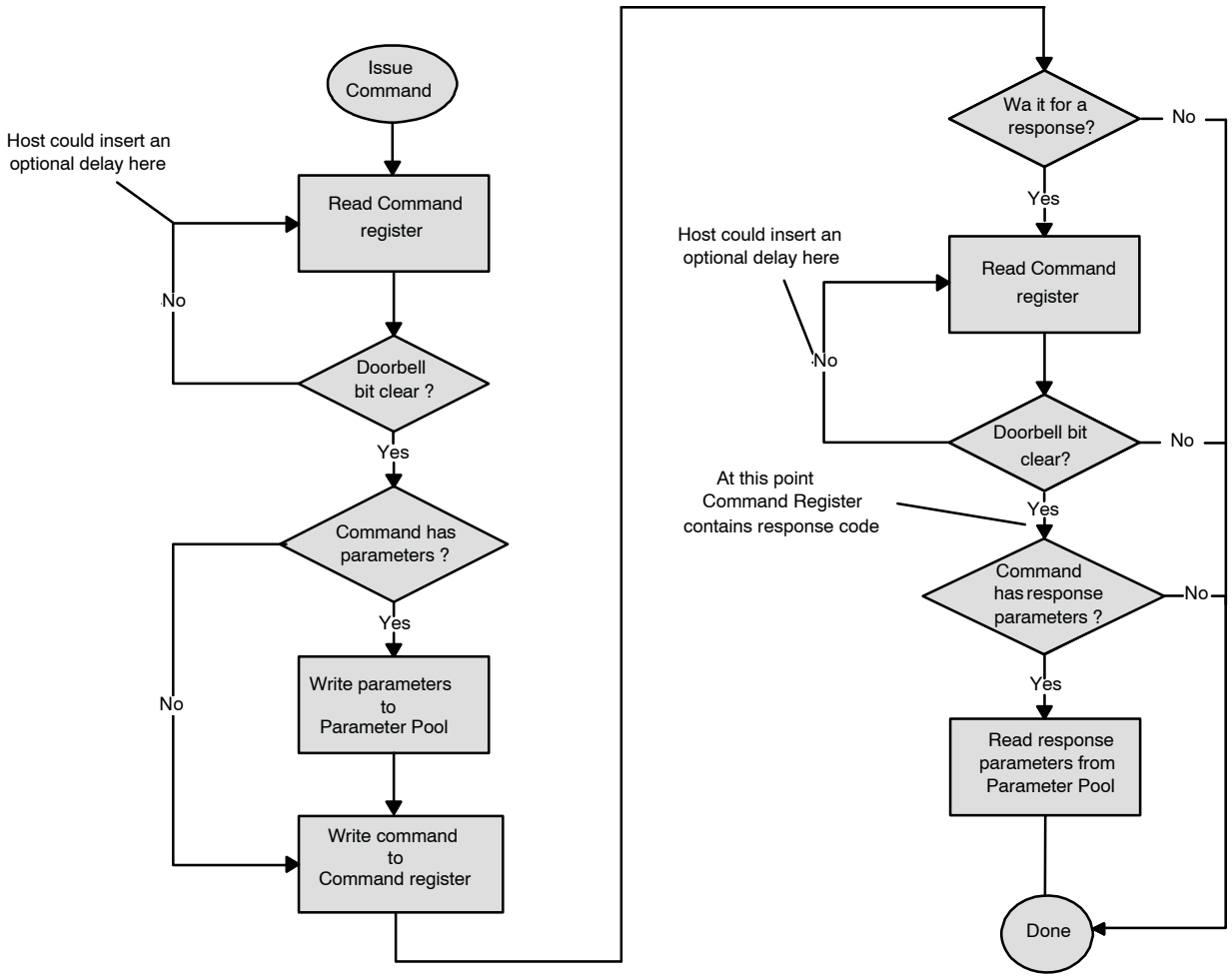


Figure 24. Host Command Process Flow

Command Flow

The host issues a command by writing (through a two−wire interface bus) to the command register. All commands are encoded with bit 15 set, which automatically generates the host command (doorbell) interrupt to the microprocessor.

Assuming initial conditions, the host first writes the command parameters (if any) to the parameters pool (in the command handler's logical page), then writes the command to command register. The interrupt handler then signals the command handler task to process the command.

If the host wishes to determine the outcome of the command, it must poll the command register waiting for the doorbell bit to be cleared. This indicates that the firmware completed processing the command. The contents of the command register indicate the command's result status. If the command generated response parameters, the host can now retrieve these from the parameters pool.

NOTE: The host must not write to the parameters pool, nor issue another command, until the previous command completes. This is true even if the host does not care about the result of the previous command. Therefore, the host must always poll the command register to determine the state of the doorbell bit, and ensure the bit is cleared before issuing a command.

For a complete command list and further information consult the Host Command Inter− face Specification.

An example of how (using DevWare) a command may be initiated in the form of a "Preset" follows.

Set Parallel Mode – Normal (Overlay i656)

All DevWare presets supplied by ON Semiconductor poll and test the doorbell bit after issuing the command. Therefore there is no need to check if the doorbell bit is clear before issuing the next command.

```
REG = 0xFC00, 0x1000 //
CMD_HANDLER_PARAMS_POOL_0
REG= 0x0040, 0x8801 // issue command
// POLL COMMAND_REGISTER::DOORBELL => 0x0
```

Summary of Host Commands

Table 17 through Table 22 show summaries of the host commands. The commands are divided into the following sections:

- System Manager
- Overlay
- Dewarp (or Lens Distortion Correction)
- GPIO Host interface
- Flash Manager Host
- Patch Loader Interface
- TX Manager

Following is a summary of the Host Interface commands. The description gives a quick orientation. The "Type" column shows if it is an asynchronous or synchronous command. For a complete list of all commands including parameters, consult the Host Command Interface Specification document.

Table 17. SYSTEM MANAGER COMMANDS

System Manager Host Command	Value	Type	Description
Set State	0x8100	Asynchronous	Request the system enter a new state
Get State	0x8101	Synchronous	Get the current state of the system

Table 18. OVERLAY HOST COMMANDS

Overlay Host Command	Value	Type	Description
Enable Overlay	0x8200	Synchronous	Enable or disable the overlay subsystem
Get Overlay State	0x8201	Synchronous	Retrieve the state of the overlay subsystem
Set Calibration	0x8202	Synchronous	Set the calibration offset
Set Bitmap Property	0x8203	Synchronous	Set a property of a bitmap
Get Bitmap Property	0x8204	Synchronous	Get a property of a bitmap
Set String Property	0x8205	Synchronous	Set a property of a character string
Load Buffer	0x8206	Asynchronous	Load an overlay buffer with a bitmap (from Flash)
Load Status	0x8207	Synchronous	Retrieve status of an active load buffer operation
Write Buffer	0x8208	Synchronous	Write directly to an overlay buffer
Read Buffer	0x8209	Synchronous	Read directly from an overlay buffer
Enable Layer	0x820A	Synchronous	Enable or disable an overlay layer
Get Layer Status	0x820B	Synchronous	Retrieve the status of an overlay layer
Set String	0x820C	Synchronous	Set the character string
Load String	0x820E	Asynchronous	Load a character string (from Flash)

Table 19. GPIO HOST COMMANDS

GPIO Host Command	Value	Type	Description
Set GPIO Property	0x8400	Synchronous	Set a property of one or more GPIO pins
Get GPIO Property	0x8401	Synchronous	Retrieve a property of a GPIO pin
Set GPO State	0x8402	Synchronous	Set the state of a GPO pin or pins
Get GPIO State	0x8403	Synchronous	Get the state of a GPI pin or pins
Set GPI Association	0x8404	Synchronous	Associate a GPI pin state with a Command Sequence stored in SPI Flash

Table 20. FLASH MANAGER HOST COMMANDS

Flash Manager Host Command	Value	Type	Description
Get Lock	0x8500	Asynchronous	Request the Flash Manager access lock
Lock Status	0x8501	Synchronous	Retrieve the status of the access lock request
Release Lock	0x8502	Synchronous	Release the Flash Manager access lock
Config	0x8503	Synchronous	Configure the Flash Manager and underlying SPI Flash subsystem
Read	0x8504	Asynchronous	Read data from the SPI Flash
Write	0x8505	Asynchronous	Write data to the SPI Flash
Erase Block	0x8506	Asynchronous	Erase a block of data from the SPI Flash
Erase Device	0x8507	Asynchronous	Erase the SPI Flash device
Query Device	0x8508	Asynchronous	Query device−specific information
Status	0x8509	Synchronous	Obtain status of current asynchronous operation

Table 21. SEQUENCER HOST COMMANDS

Sequencer Host Command	Value	Type	Description
Set Encoding Mode	0x8603	Synchronous	Set the encoding mode
Enable Horizontal Flip	0x8604	Synchronous	Enable or disable horizontal flip
Set Flicker Frequency	0x8605	Synchronous	Set the flicker frequency
Refresh Mode	0x8606	Synchronous	Refresh the Sequencer mode/context

Table 22. TX MANAGER HOST COMMANDS

TX Manager Host Command	Value	Type	Description
Config DAC	0x8800	Synchronous	Configure the Video DAC
Set Parallel Mode	0x8801	Synchronous	Configure the Parallel output port

SLAVE TWO−WIRE SERIAL INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the MT9V127. This interface is designed to be compatible with the MIPI Alliance Standard for Camera Serial Interface 2 (CSI−2) 1.0, which uses the electrical characteristics and transfer protocols of the two−wire serial interface specification.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and used to synchronize transfers.

Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a pull−up resistor in the range of 1.5 to 4.7 kΩ resistor.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low− level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16−bit register address
- an acknowledge or a no−acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 23 below.

Table 23. TWO−WIRE INTERFACE ID ADDRESS SWITCHING

SADDR	Two−Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The default slave addresses used by the MT9V127 are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two−wire serial interface specification.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Typical Operation

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which a WRITE will take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16−bit data, as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, just as in the write request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

Figure 25 shows the typical READ cycle of the host to MT9V127. The first two bytes sent by the host are an internal 16−bit register address. The following 2−byte READ cycle sends the contents of the registers to host.

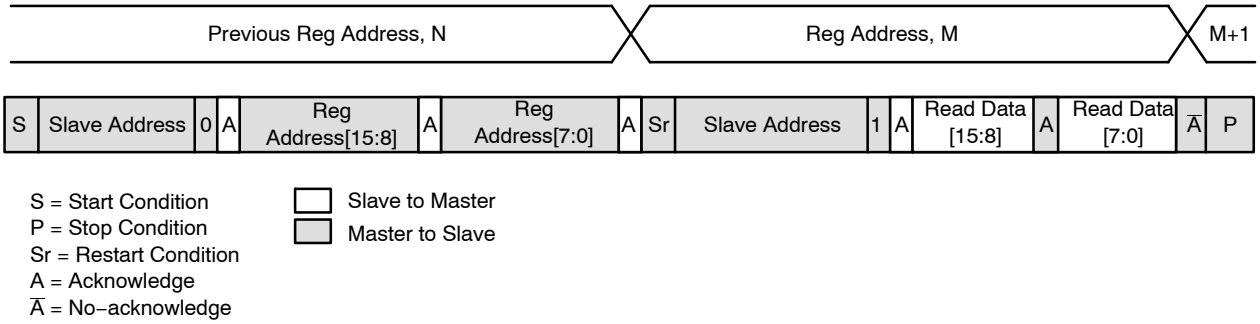


Figure 25. Single READ from Random Location

Single READ from Current Location

Figure 26 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

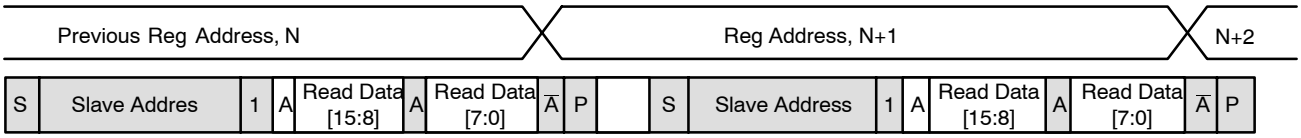


Figure 26. Single Read from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 27) starts in the same way as the single READ from current location (Figure 25). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until “L” bytes have been read.

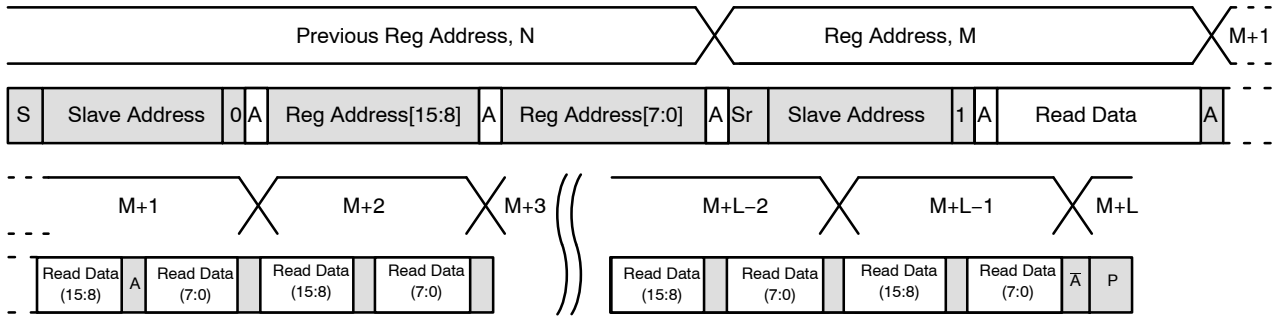


Figure 27. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 28) starts in the same way as the single READ from current location (Figure 26). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until “L” bytes have been read.

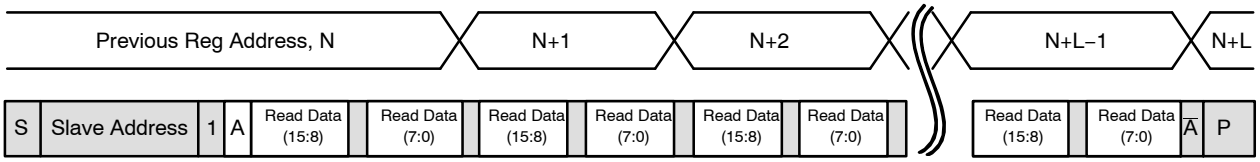


Figure 28. Sequential READ, Start from Current Loacation

Single WRITE to Random Location

Figure 29 shows the typical WRITE cycle from the host to the MT9V127. The first 2 bytes indicate a 16−bit address of the internal registers with most−significant byte first. The following 2 bytes indicate the 16−bit data.

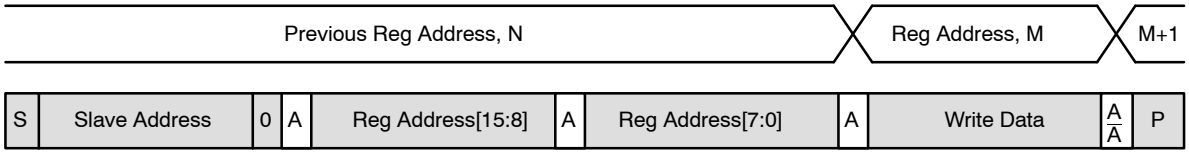


Figure 29. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 30) starts in the same way as the single WRITE to random location (Figure 29). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

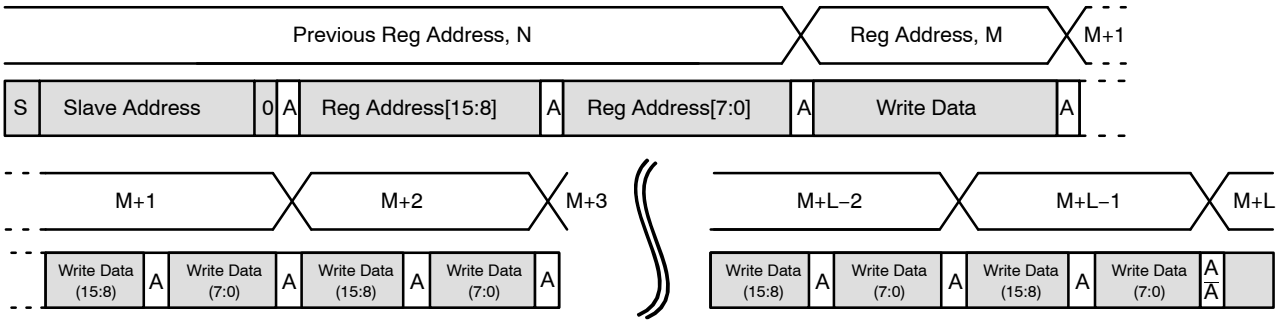


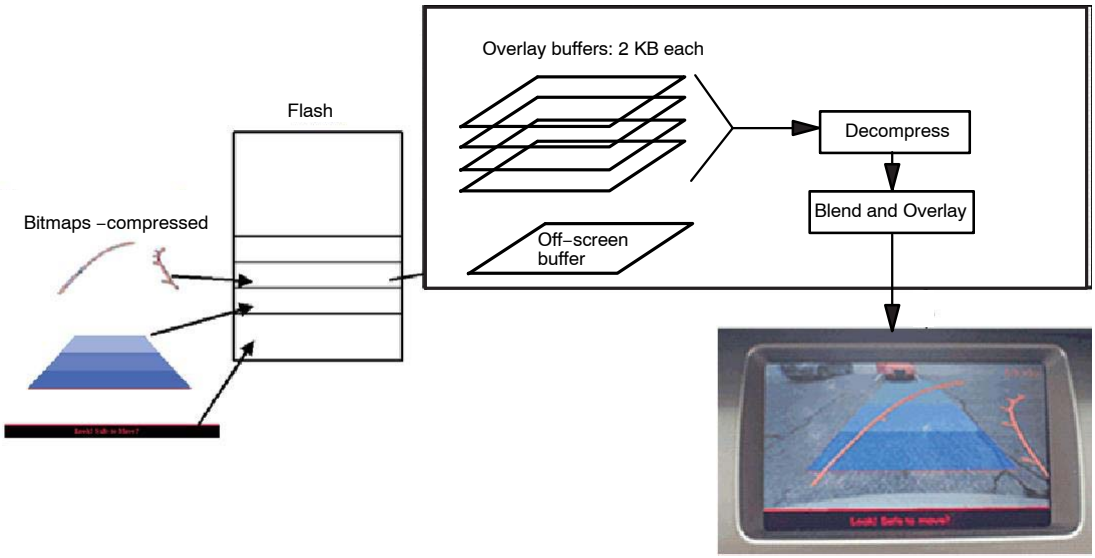
Figure 30. Sequential WRITE, Start at Random Location

OVERLAY CAPABILITY

Figure 31 highlights the graphical overlay data flow of the MT9V127. The images are separated to fit into 2 KB blocks of memory after compression.

- Up to four overlays may be blended simultaneously
- Overlay size 360 x 480 pixels rendered into a display area of 720 x 480 pixels
- Selectable readout: rotating order is user programmable
- Dynamic movement through predefined overlay images
- Palette of 32 colors out of 64,000 with eight colors per bitmap
- Blend factors may be changed dynamically to achieve smooth transitions

The host commands allow a bitmap to be written piecemeal to a memory buffer through the I²C, and through the DMA direct from SPI Flash memory. Multiple encoding passes may be required to fit an image into a 2 KB block of memory; alternatively, the image can be divided into two or more blocks to make the image fit. Every graphic image may be positioned in an x/y direction and overlap with other graphic images.



NOTE: These images are not actually rendered, but show conceptual objects and object blending.

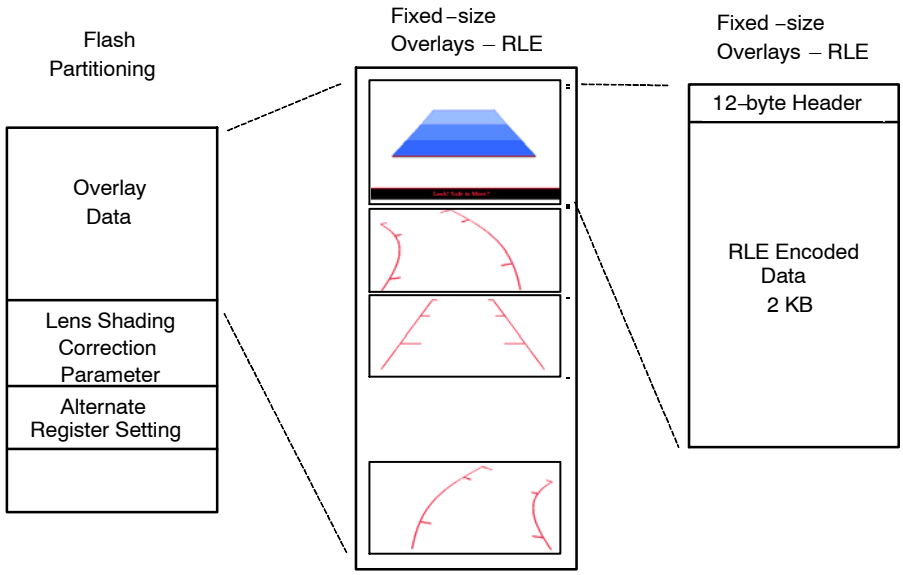
Figure 31. Overlay Data Flow

SERIAL MEMORY PARTITION

The contents of the Flash/EEPROM memory partition logically into three blocks (see Figure 32):

- Memory for overlay data and descriptors
- Memory for register settings, which may be loaded at boot−up
- Firmware extensions or software patches; in addition to the on−chip firmware, extensions reside in this block of memory

These blocks are not necessarily contiguous.



NOTE: For a complete description of memory organization, refer to the MT9V127 SPI Flash Contents Encoding Specification.

Figure 32. Memory Partitioning

External Memory Speed Requirement

For a 2 KB block of overlay to be transferred within a frame time to achieve maximum update rate, the serial memory has to be a certain speed.

Table 24. TRANSFER TIME ESTIMATE

Frame Time	SPI Clock	Transfer Time to 2 KB
33.3 ms	4.5 MHz	1 ms

OVERLAY ADJUSTMENT

To ensure a correct position of the overlay to compensate for assembly deviation, the overlay can be adjusted with assistance from the overlay statistics engine:

- The overlay statistics engine supports a windowed 8−bin luma histogram, either row− wise (vertical) or column−wise (horizontal)
- The example calibration statistics firmware patch can be used to perform an automatic successive−approximation search of a cross−hair target within the scene
- On the first frame, the firmware performs a coarse horizontal search, followed by a coarse vertical search in the second frame
- In subsequent frames, the firmware reduces the region−of−interest of the search to the histogram bins containing the greatest accumulator values, thereby refining the search
- The resultant X, Y location of the cross−hair target can be used to assign a calibration value of offset selected overlay graphic image positions within the output image
- The calibration statistics patch also supports a manual mode, which allows the host to access the raw accumulator values directly

NOTE: For the overlay calibration feature to work, load the appropriate patch. See Statistics Engine document.

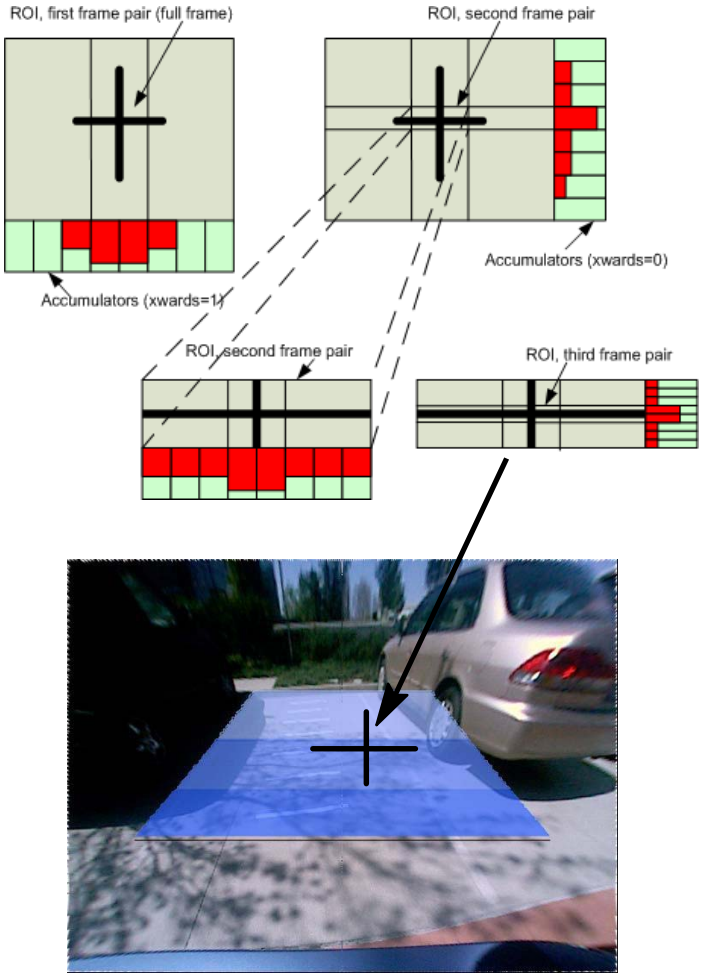


Figure 33. Overlay Calibration

The position of the target will be used to determine the calibration value that shifts the X,Y position of adjustable overlay graphics.

The overlay calibration is intended to be applied on a device by device basis “in system,” which means after the camera has been installed. ON Semiconductor provides basic programming scripts that may reside in the SPI Flash memory to assist in this effort.

OVERLAY CHARACTER GENERATOR

In addition to the four overlay layers, a fifth layer exists for a character generator overlay string.

There are a total of:

- 16 alphanumeric characters available
- 22 characters maximum per line
- 16 x 32 pixels with 1−bit color depth

Any update to the character generator string requires the string to be passed in its entirety with the Host Command. Character strings have their own control properties aside from the Overlay bitmap properties.

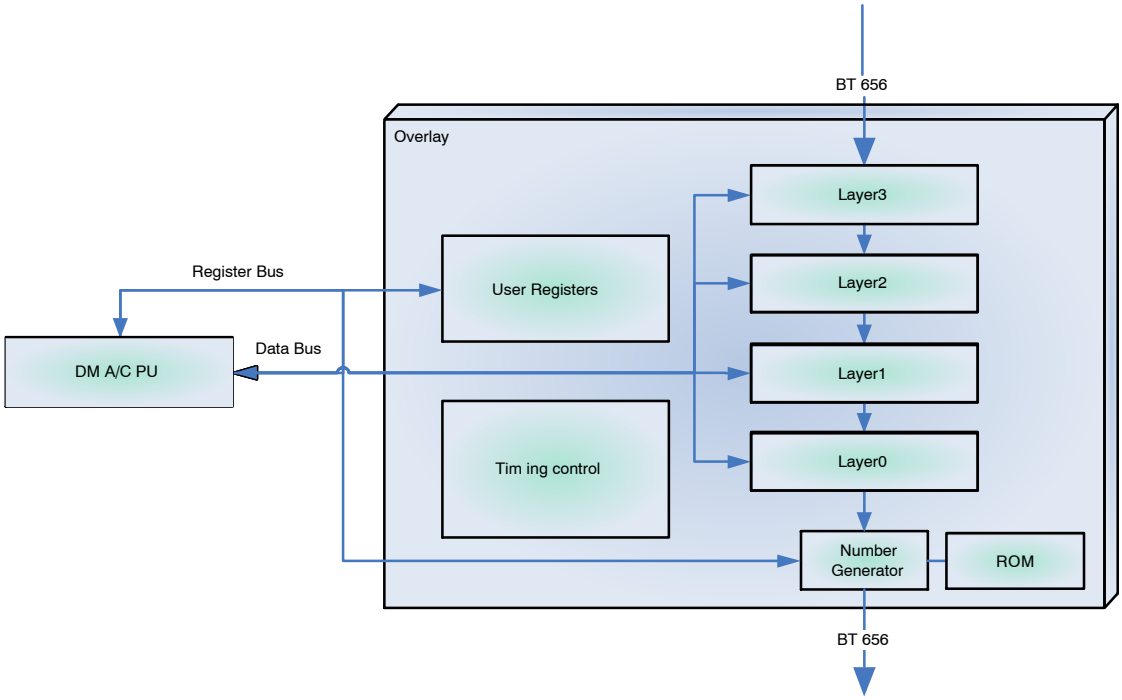


Figure 34. Internal Block Diagram Overlay

Character Generator

The character generator can be seen as the fifth top layer, but instead of getting the source from RLE data in the memory buffers, it has a predefined 16 characters stored in ROM.

All the characters are 1−bit depth color and are sharing the same YCbCr look up table.

ROM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x06	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x08	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x0a	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x0c	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0
0x0e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x10	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x12	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x14	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x16	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x18	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1a	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1c	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x1e	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x20	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x22	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x24	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x26	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
0x28	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	0
0x2a	0	0	1	1	1	0	0	0	0	0	0	1	1	1	1	0
0x2c	0	0	1	1	1	0	0	0	0	0	0	1	1	1	0	0
0x2e	0	0	1	1	1	1	0	0	0	0	0	1	1	1	0	0
0x30	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
0x32	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0
0x34	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
0x36	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0
0x38	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0x3a	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3c	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x3e	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
…																

Figure 35. Example of Character Descriptor 0 Stored in ROM

It can show a row of up to 22 characters of 16 x 32 pixels resolution (32 x 32 pixels when blended with the BT 656 data).

Character Generator Details

Table 25 shows the characters that can be generated.

Table 25. CHARACTER GENERATOR DETAILS

Item	Quantity	Description
16−bit character	22	Coder for one of these characters: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, /, (space), :, –, (comma), (period)
1 bpp color	1	Depth of the bit map is 1 bpp

It is the responsibility of the user to set up proper values in the character positioning to fit them in the same row (that is one of the reasons that 22 is the maximum number of characters).

NOTE: No error is generated if the character row overruns the horizontal or vertical limits of the frame.

Full Character Set for Overlay

Figure 36 shows all of the characters that can be generated by the MT9V127.

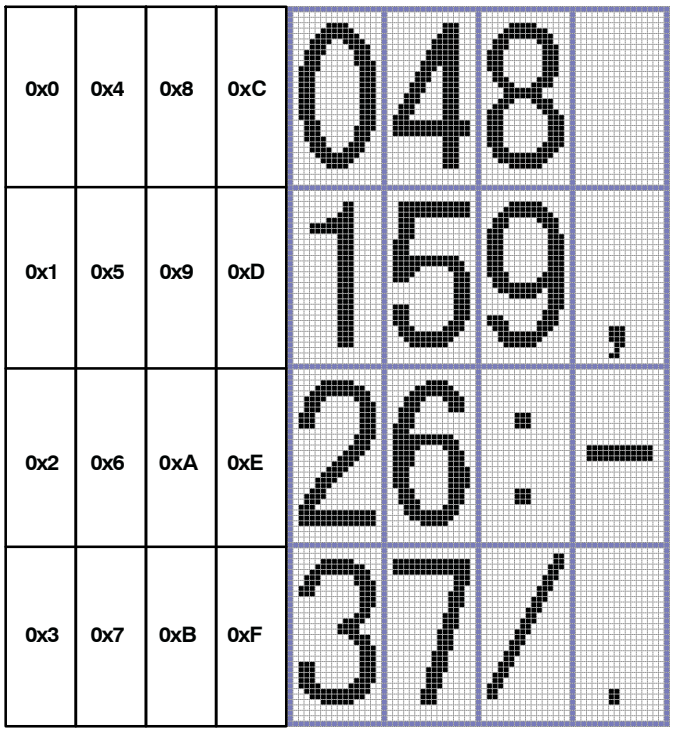


Figure 36. Full Character Set for Overlay

MODES AND TIMING

This section provides an overview of the typical usage modes and related timing information for the MT9V127.

Composite Video Output

The external pin D_{OUT}_LSB0 can be used to configure the device for default NTSC or PAL operation. This and other video configuration settings are available as register settings accessible through the serial interface.

NTSC

Both differential and single−ended connections of the full NTSC format are supported. The differential connection that uses two output lines is used for low noise or long distance applications. The single−ended connection is used for PCB tracks and screened cable where noise is not a concern. The NTSC format has three black lines at the bottom of each image for padding (which most LCDs do not display).

PAL

The PAL format is supported with 576 active image rows.

NTSC or PAL with External Image Processing

The on−chip video encoder and DAC can be used with external data stream input (DIN[7:0] port). Correct NTSC or PAL formatted CCIR656 data is required for correct composite video output.

The on−chip overlay may be put on top of the overlay generated by the external overlay generator.

Single−Ended and Differential Composite Output

The composite output can be operated in a single−ended or differential mode by simply changing the external resistor configuration. For single−ended termination, see Figure 37. The differential schematic is shown in Figure 38.

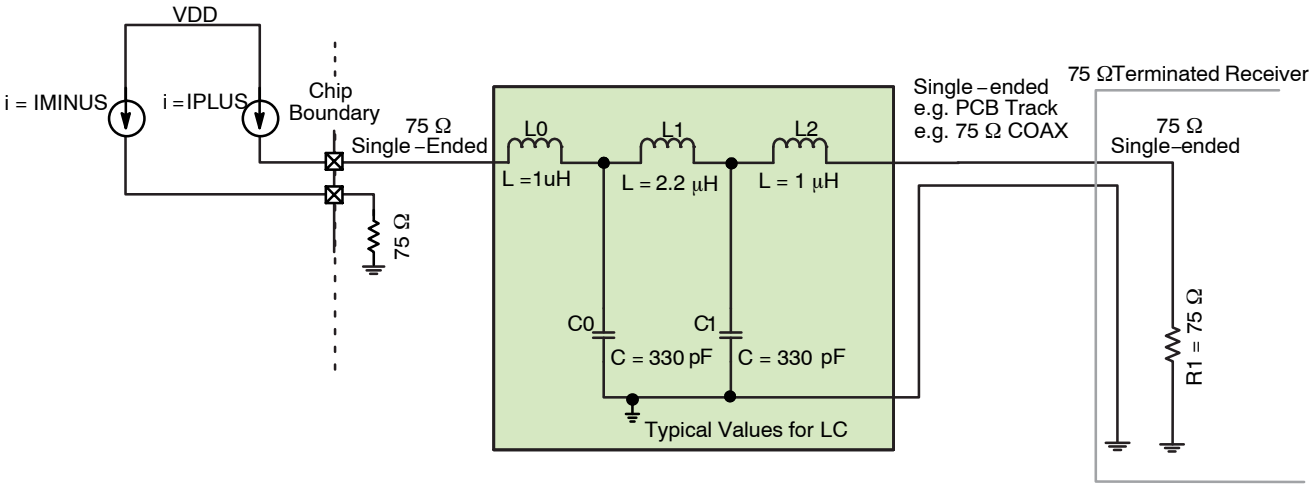


Figure 37. Single−Ended Termination

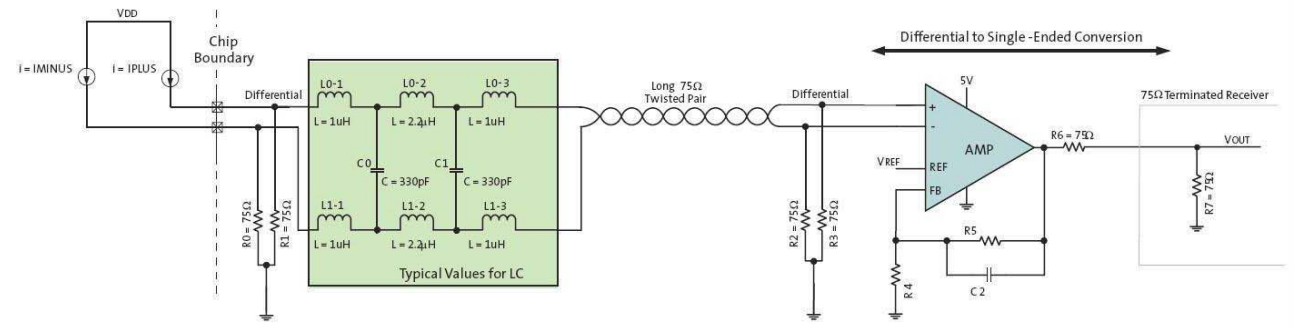


Figure 38. Differential Connection—Grounded Termination

Parallel Output (D_{OUT})

The $D_{OUT}[7:0]$ port supports both progressive and Interlaced mode. Progressive mode (with FV and LV signal) include raw bayer(8 or 10 bit), YCbCr, RGB. Interlaced mode is CCIR656 compliant.

Figure 39 shows the data that is output on the parallel port for CCIR656. Both NTSC and PAL formats are displayed. The blue values in Figure 39 represent NTSC (525/60). The red values represent PAL (625/50).

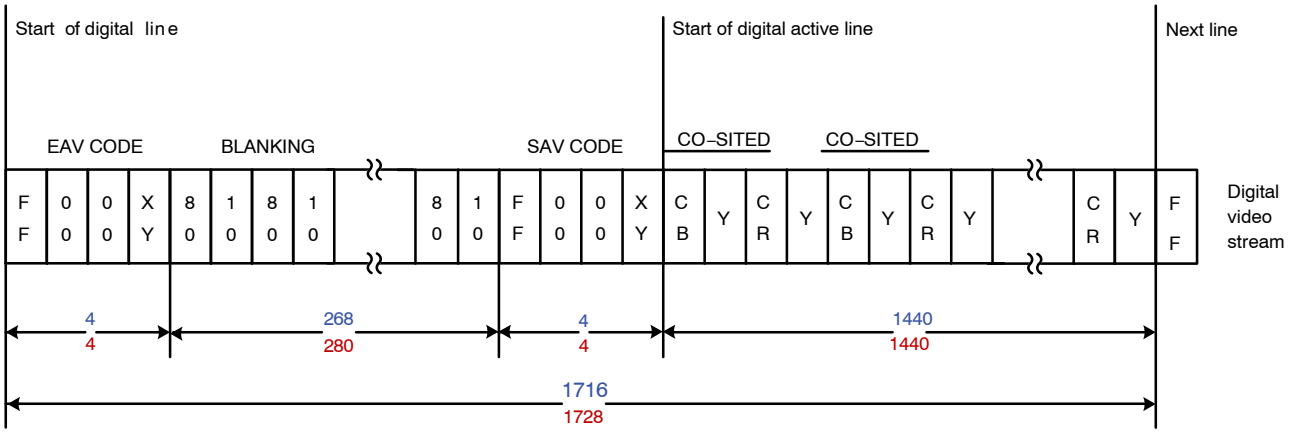


Figure 39. CCIR656 8−Bit Parallel Interface Format for 525/60 (625/50) Video Systems

Figure 40 shows detailed vertical blanking information for NTSC timing. See Table 26 for data on field, vertical blanking, EAV, and SAV states.

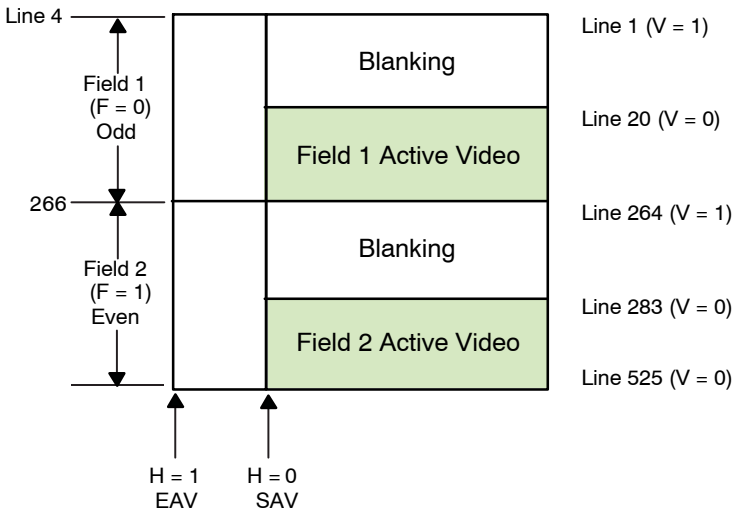


Figure 40. Typical CCIR656 Vertical Blanking Intervals for 525/60 Video System

Table 26. FIELD, VERTICAL BLANKING, EAV, AND SAV STATES 525/60 VIDEO SYSTEM

Line Number	F	V	H (EAV)	H (SAV)
1–3	1	1	1	0
4–9	0	1	1	0
20–263	0	0	1	0
264–265	0	1	1	0
266–282	1	1	1	0
283–525	1	0	1	0

Figure 41 shows detailed vertical blanking information for PAL timing. See Table 27 for data on field, vertical blanking, EAV, and SAV states.

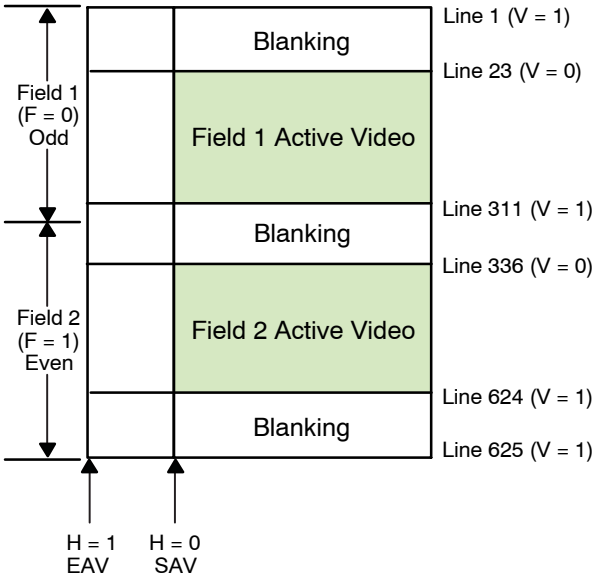


Figure 41. Typical CCIR656 Vertical Blanking Intervals for 625/50 Video System

Table 27. FIELD, VERTICAL BLANKING, EAV, AND SAV STATES FOR 625/50 VIDEO SYSTEM

Line Number	F	V	H (EAV)	H (SAV)
1–22	0	1	1	0
23–310	0	0	1	0
311–312	0	1	1	0
313–335	1	1	1	0
336–623	1	0	1	0
624–625	1	1	1	0

Parallel Input (D_{IN})

The data−in port allows external CCIR656 data to be multiplexed into the NTSC or PAL output data. Figure 42 shows the timing of the data−in (DIN[7:0]) signals. Table 28 describes timing values for the parallel input waveform. Both mode 0 and mode 1 wave− forms are supported.

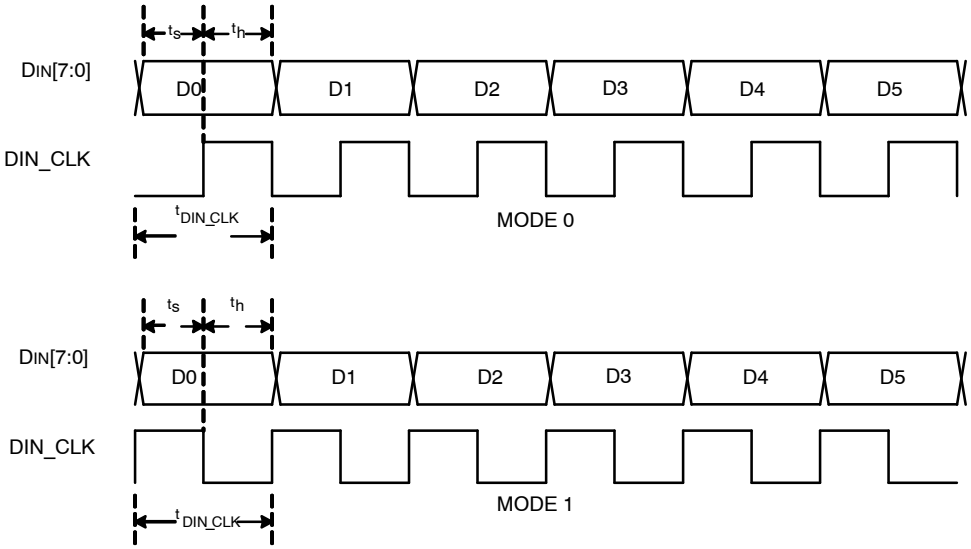


Figure 42. Parallel Input Data Timing Waveform Using D_{IN}_CLK

Table 28. PARALLEL INPUT DATA TIMING VALUES USING D_{IN}_CLK

Name	Conditions	Min	Typical	Max	Parameter
tDIN_CLK	Max ±100 ppm	–	37	–	DIN_CLK Period
t_s		8	–	18.5	DIN Setup Time
t_h		8	–	18.5	DIN Hold Time

5. Setup and hold times are measured with respect to the rising or falling edge of DIN_CLK, which can be programmed by R0x0016[13].

Reset and Clocks

Reset

Power−up reset is asserted or de−asserted with the RESET_BAR pin, which is active LOW. In the reset state, all control registers are set to default values. See “Device Configuration” for more details on Auto, Host, and Flash configurations.

Soft reset is asserted or de−asserted by the two−wire serial interface program. In soft− reset mode, the two−wire serial interface and the register bus are still running. All control registers are reset using default values.

Clocks

The MT9V127 has three primary clocks:

- A master clock coming from the EXTCLK signal
- In default mode, a pixel clock (PIXCLK) running at 2 × EXTCLK. In raw Bayer bypass mode, PIXCLK runs at the same frequency as EXTCLK.
- DIN_CLK that is associated with the parallel DIN port.

When the MT9V127 operates in sensor stand−alone mode, the image flow pipeline clocks can be shut off to conserve power.

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal blanking and vertical blanking are influenced by the sensor configuration, and are also a function of certain image flow pipeline functions. The relationship of the primary clocks is depicted in Figure 43.

The image flow pipeline typically generates up to 16 bits per pixel−for example, YCbCr or 565RGB−but has only an 8−bit port through which to communicate this pixel data.

To generate NTSC or PAL format images, the sensor core requires a 27 MHz clock.

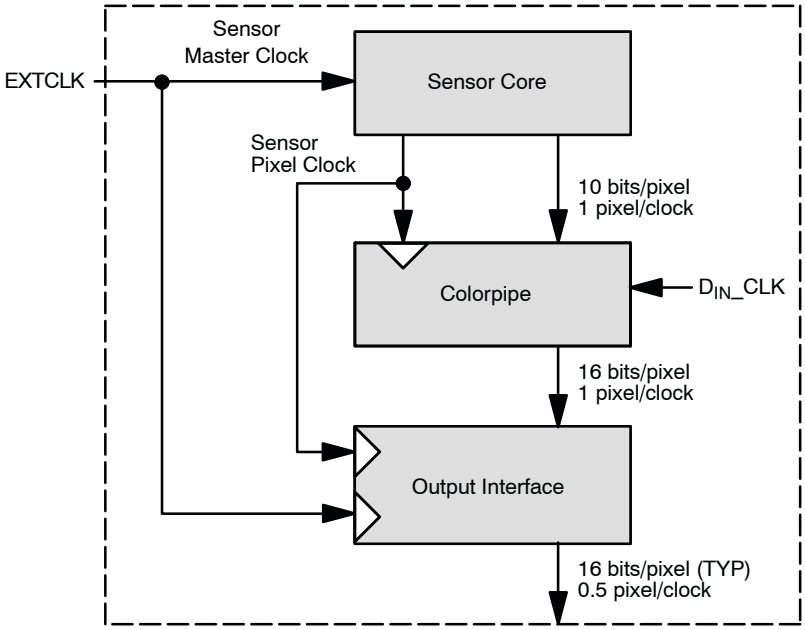


Figure 43. Primary Clock Relationships

Floating Inputs

The following MT9V127 pins cannot be floated:

- DIN_CLK (tie to GND if not used)
- SDATA–This pin is bidirectional and should not be floated
- FRAME_SYNC
- TRST_N

Output Data Ordering

Table 29. OUTPUT DATA ORDERING IN D_{OUT} RGB MODE

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

6. PIXCLK is 54 MHz when EXTCLK is 27 MHz.

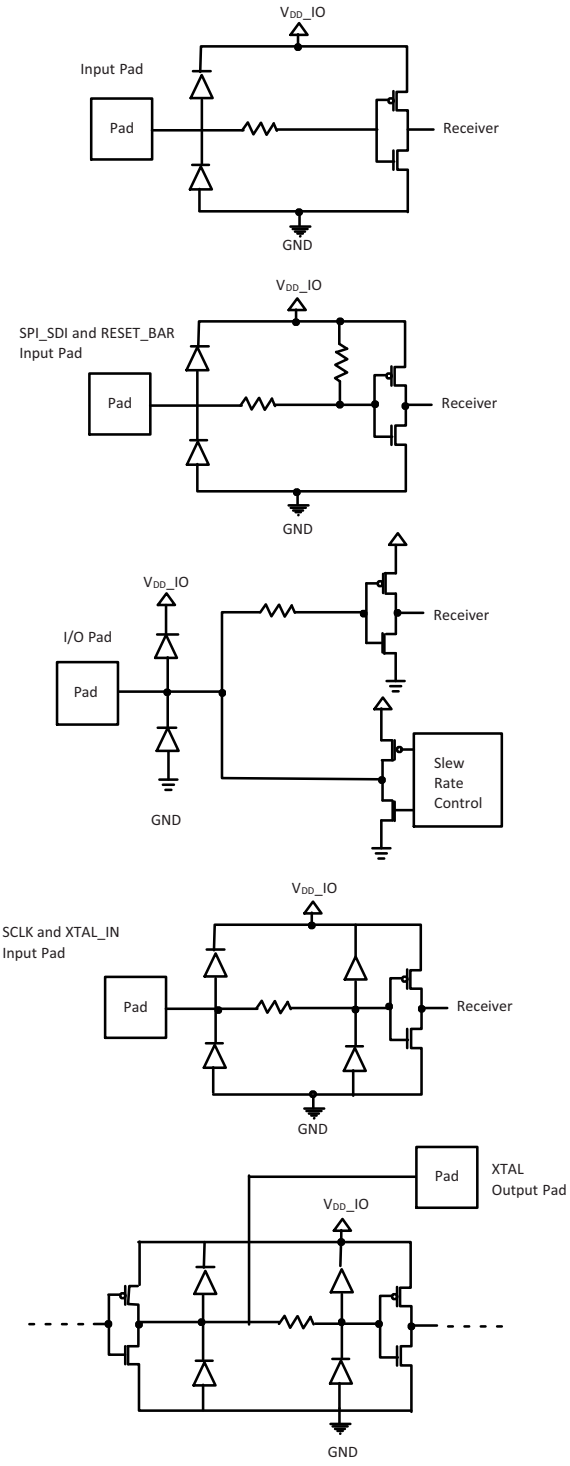
Table 30. OUTPUT DATA ORDERING IN SENSOR STAND−ALONE MODE

Mode	D7	D6	D5	D4	D3	D2	D1	D0	D_{OUT}_LSB1	D_{OUT}_LSB0
10−bit Output	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

7. PIXCLK is 27 MHz when EXTCLK is 27 MHz.

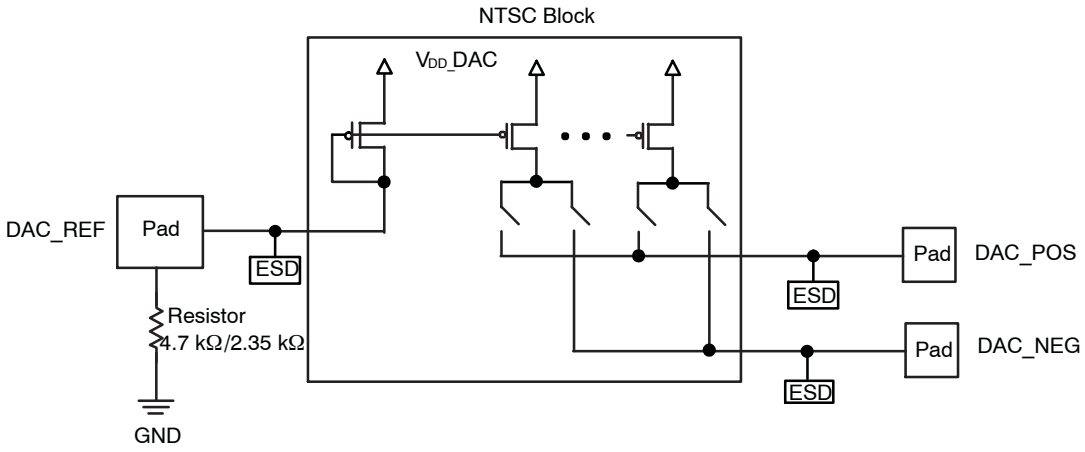
I/O Circuitry

Figure 44 illustrates typical circuitry used for each input, output, or I/O pad.



NOTE: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 44. Typical I/O Equivalent Circuits



NOTE: All I/O circuitry shown above is for reference only. The actual implementation may be different.

Figure 45. NTSC Block

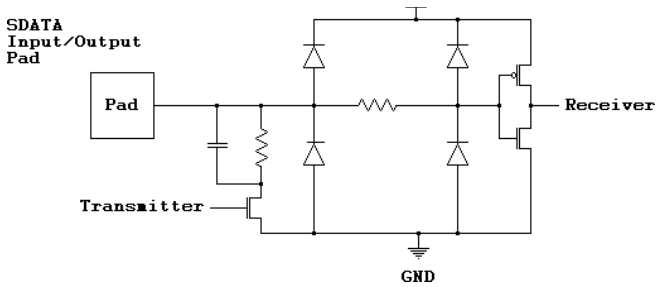


Figure 46. Serial Interface

I/O Timing

Digital Output

By default, the MT9V127 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in Figure 47.

As an option, the polarity of the PIXCLK can be inverted from the default by programming R0x0016[14].

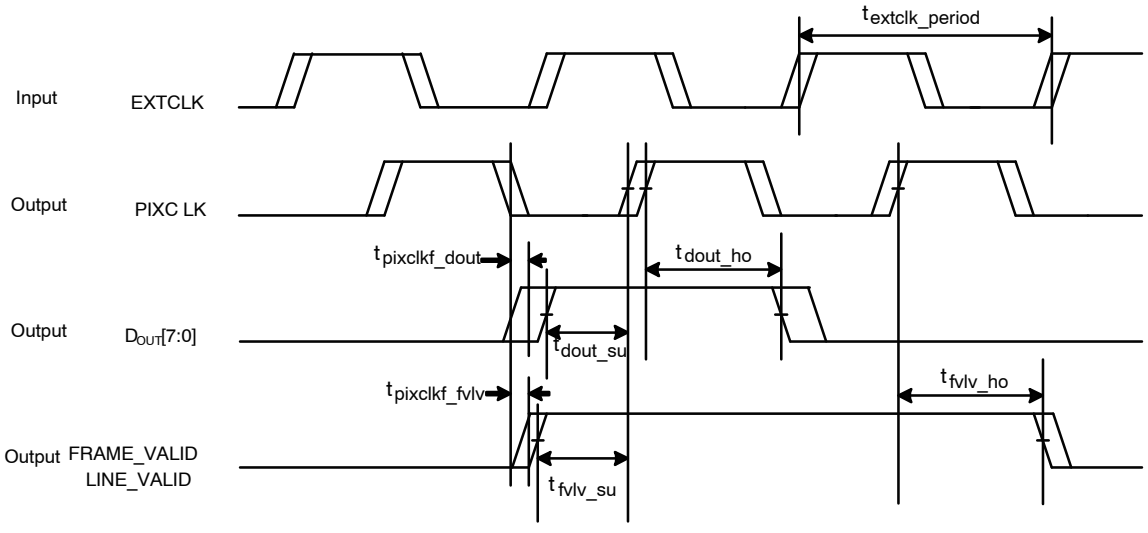


Figure 47. Digital Output I/O Timing

Table 31. PARALLEL DIGITAL OUTPUT I/O TIMING

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V; Default slew rate

Signal	Parameter	Conditions	Min	Typ	Max	Unit
EXTCLK	^{f}extclk	max ±100 ppm	–	27	–	MHz
	^{t}extclk_period		–	37	–	ns
	Duty cycle		45	50	55	%
PIXCLK[1]	^{f}pixclk		–	27	–	MHz
	^{t}pixclk_period		–	37	–	ns
	Duty cycle		45	50	55	%
DATA[7:0]	^{t}pixclkf_dout		–2	0	2	ns
	^{t}dout_su		8	–	18.5	ns
	^{t}dout_ho		8	–	18.5	ns
FV/LV	^{t}pixclkf_fvlv		–2	0	2	ns
	^{t}fvlv_su		8	–	18.5	ns
	^{t}fvlv_ho		8	–	18.5	ns

8. PIXCLK can be inverted from the default by programming R0x0016[14].

Slew Rate

Table 32. SLEW RATE FOR PIXCLK AND D_{OUT}

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V; T = 25°C; CLOAD = 40 pF

PIXCLK			DOUT[7:0]			
R0x30 [10:8]	Typical Rise Time	Typical Fall Time	R0x30 [2:0]	Typical Rise Time	Typical Fall Time	Unit
000	6.5	6.3	000	6.5	6.3	ns
001	4.8	4.6	001	4.8	4.6	ns
010	3.9	3.8	010	3.9	3.8	ns
011	3.7	3.7	011	3.7	3.7	ns
100	3.6	3.6	100	3.6	3.6	ns
101	3.5	3.5	101	3.5	3.5	ns
110	3.4	3.4	110	3.4	3.4	ns
111	3.3	3.3	111	3.3	3.3	ns

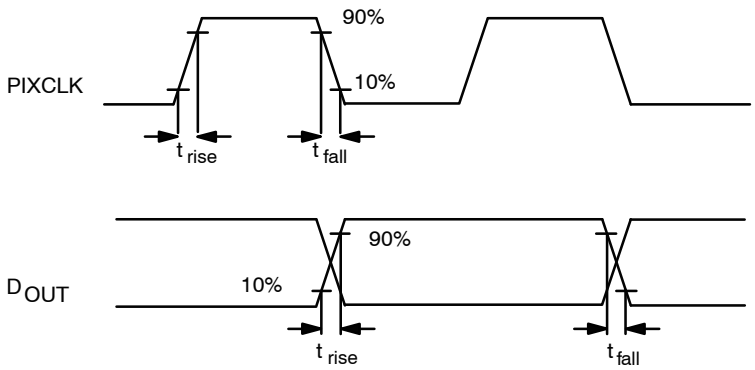


Figure 48. Slew Rate Timing

Configuration Timing

During start−up, the D_{OUT}_LSB0, LV and FV are sampled. Setup and hold timing for the RESET_BAR signal with respect to D_{OUT}_LSB0, LV, and FV are shown in Figure 49 and Table 33. These signals are sampled once by the on−chip firmware, which yields a long tHold time.

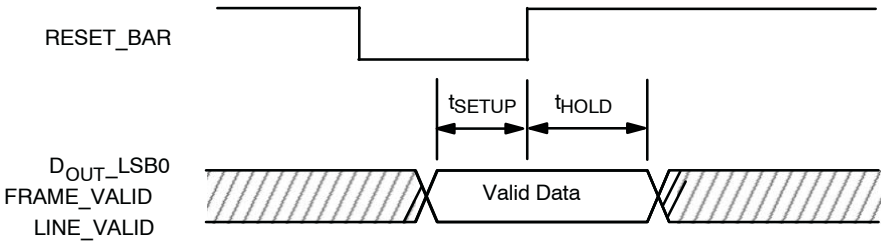
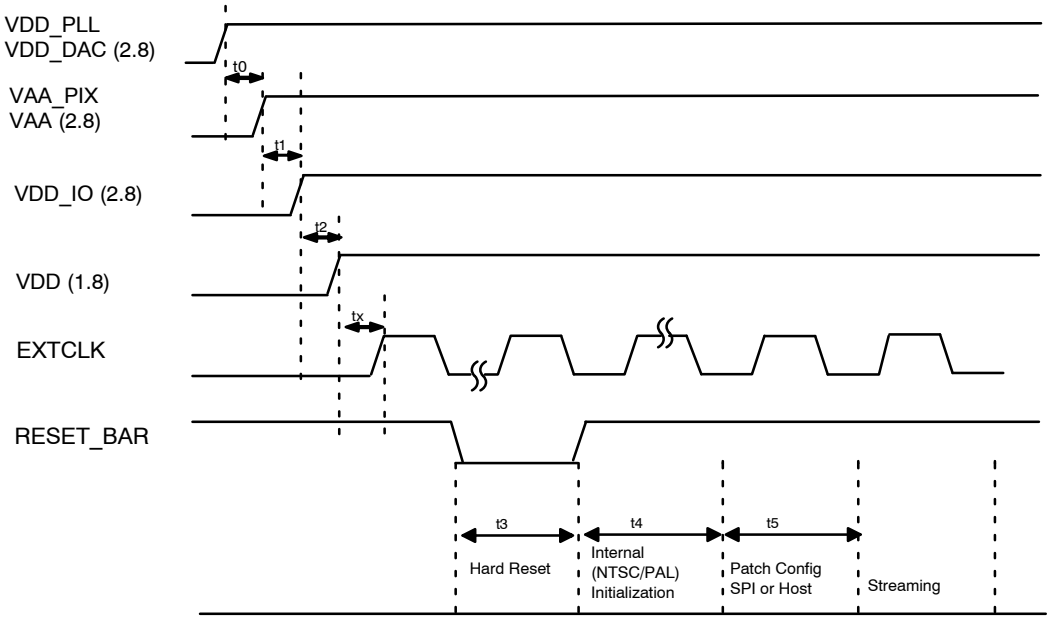


Figure 49. Configuration Timing

Table 33. CONFIGURATION TIMING

Signal	Parameter	Min	Typ	Max	Unit
DOUT_LSB0, FRAME_VALID, LINE_VALID	tSETUP	0			µs
	tHOLD	50			µs



NOTES:

9. RESET_BAR may not exceed VDD_IO + 0.3 V.
10. The 2.8 V plane (VAA, VAA_PIX, VDD_PLL, VDD_DAC, VDD_IO) must remain at a higher voltage than the 1.8 V core voltage at all times.

Figure 50. Power Up Sequence

Table 34. POWER UP SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD_PLL to VAA/VAA_PIX	t0	0	–	–	µS
VAA/VAA_PIX to VDD_IO	t1	0	–	–	µS
VDD_IO to VDD	t2	0	–	–	µS
Xtal settle time	tx	–	30 (Note 11)	–	mS

Table 34. POWER UP SEQUENCE (continued)

Definition	Symbol	Minimum	Typical	Maximum	Unit
Hard Reset	t3	10 (Note 12)	–	–	Clock cycle
Internal Initialization	t4	50	–	–	mS
Patch Load (SPI or I²C)	t5	–	400 (Note 13)	–	mS

11. Xtal settling time is component−dependent (Xtal, Oscillator, etc) and usually takes about 10 mS~100 mS.
12. Hard reset time is the minimum time required after power rails are settled. Ten clock cycles are required for the sensor itself, assuming all power rails are settled. In a circuit where Hard reset is performed by the RC circuit, then the RC time must include the all power rail settle time and Xtal.
13. This is required to load necessary patches via Flash mode (SPI) or Host mode (two−wire serial interface). Loading time varies depending on the number of patches and bus speed.

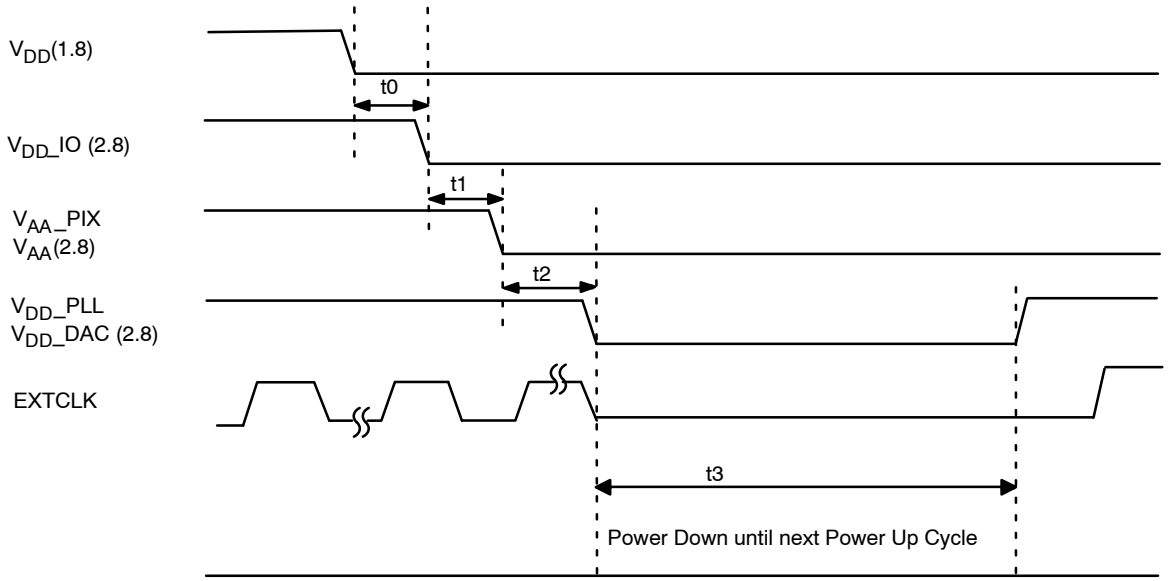


Figure 51. Power Down Sequence

Table 35. POWER DOWN SEQUENCE

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD to VDD_IO	t0	0	–	–	µS
VDD_IO to VAA/VAA_PIX	t1	0	–	–	µS
VAA/VAA_PIX to VDD_PLL/DAC	t2	0	–	–	µS
Power Down until Next Power Up Time	t3	100 (Note 14)	–	–	ms

14. t3 is required between power down and next power up time, all decoupling caps from regulators must completely discharged before next power up.

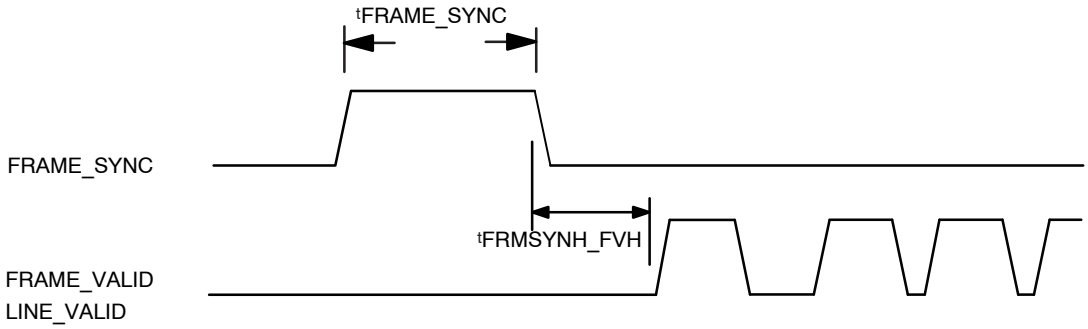


Figure 52. FRAME_SYNC to FRAME_VALID/LINE_VALID

Table 36. FRAME_SYNC TO FRAME_VALID/LINE_VALID PARAMETERS

Parameter	Name	Conditions	Min	Typ	Max	Unit
FRAME_SYNC to FV/LV	tFRMSYNC_FVH	Auto Config mode	4	–	–	ms
tFRAME_SYNC	tFRAMESYNC		30			ms

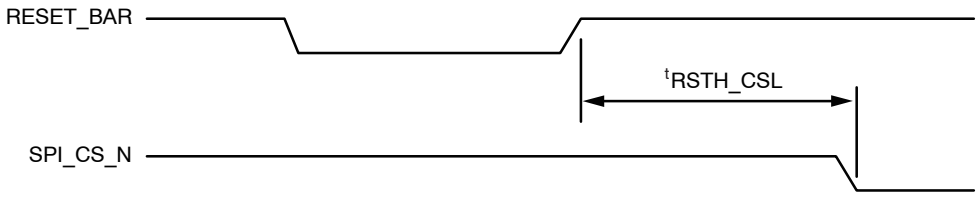


Figure 53. Reset to SPI Access Delay

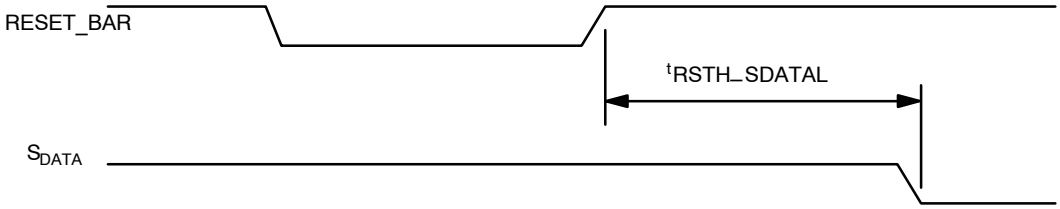


Figure 54. Reset to Serial Access Delay

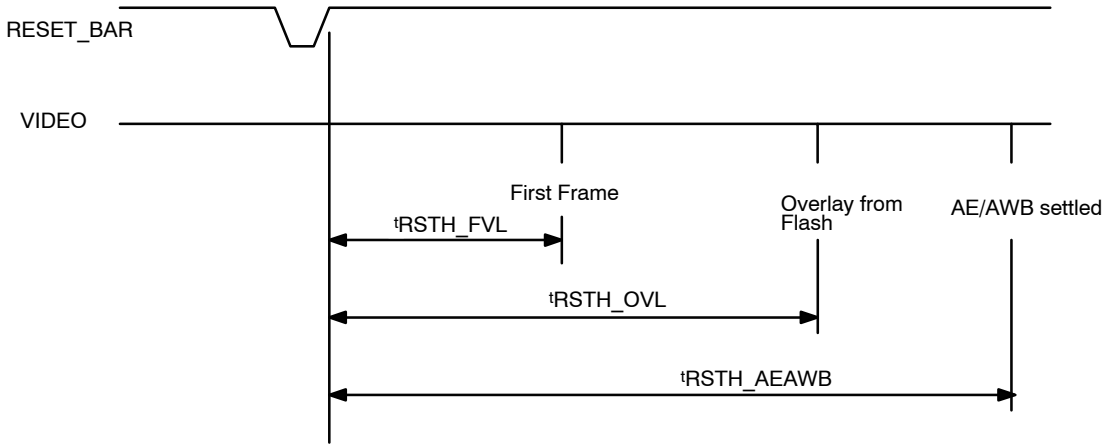


Figure 55. Reset to AE/AWB Image

Table 37. RESET_BAR DELAY PARAMETERS

Parameter	Name	Conditions	Min	Typ	Max	Unit
Power up delay 2.8 V to 1.8 V			0.1	–	–	ms
RESET_BAR HIGH to SPI_CS_N LOW	tRSTH_CSL		18	–	–	ms
RESET_BAR HIGH to SDATA LOW	tRSTH_SDATAL		1.8	–	–	ms
RESET_BAR HIGH to FRAME_VALID	tRSTH_FVL		235	–	–	ms
RESET_BAR HIGH to first Overlay	tRSTH_OVL		235	–	–	ms
RESET_BAR HIGH to AE/AWB settled	tRSTH_AEAWB		–	400	–	ms

ELECTRICAL SPECIFICATIONS

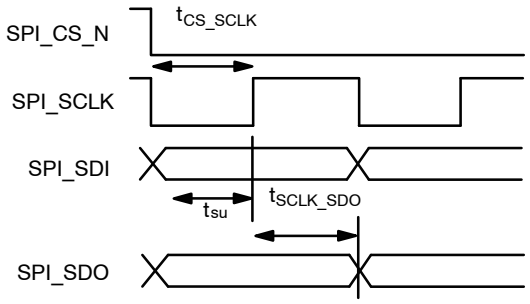


Figure 56. SPI Output Timing

Table 38. SPI DATA SETUP AND HOLD TIMING

Parameter	Description	Min	Typ	Max	Units
^{f}SPI_SCLK	SPI_SCLK Frequency	1.6875	4.5	18	MHz
^{t}su	Setup time	–	–	110	ns
^{t}SCLK_SDO	Hold time			110	ns
^{t}CS_SCLK	Delay from falling edge of SPI_CS_N to rising edge of SPI_SCLK	–	230	–	ns

Table 39. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Unit
		Min	Max	
VDD	Digital power (1.8 V)	–0.3	2.4	V
VDD_IO	I/O power (2.8 V)	–0.3	4	V
VAA	VAA Analog power (2.8 V)	–0.3	4	V
VAA_PIX	Pixel array power (2.8 V)	–0.3	4	V
VDD_PLL	PLL power (2.8 V)	–0.3	4	V
VDD_DAC	DAC power (2.8 V)	–0.3	4	V
VIN	DC Input Voltage	–0.3	VDD_IO+0.3	V
VOUT	DC Output Voltage	–0.3	VDD_IO+0.3	V
TSTG	Storage temperature	–50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 40. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Parameter (Note 15)	Condition	Min	Typ	Max	Unit
Core digital voltage (VDD)	–	1.7	1.8	1.9	V
IO digital voltage (VDD_IO)	–	2.66	2.8	2.94	V
Video DAC voltage (VDD_DAC)	–	2.66	2.8	2.94	V
PLL Voltage (VDD_PLL)	–	2.66	2.8	2.94	V
Analog voltage (VAA)	–	2.66	2.8	2.94	V
Pixel supply voltage (V_{AA}_PIX)	–	2.66	2.8	2.94	V
Leakage current	EXTCLK: HIGH or LOW			10	µA

Table 40. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS (continued)

Parameter (Note 15)	Condition	Min	Typ	Max	Unit
Imager operating temperature (Note 16)	–	–40		+105	°C
Functional operating temperature (Note 17)		–40		+85	°C
Storage temperature	–	–50		+150	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

15. V_{AA} and VAA_PIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.
16. The imager operates in this temperature range, but image quality may degrade if it operates beyond the functional operating temperature range.
17. Image quality is not guaranteed at temperatures equal to or greater than this range.

Table 41. VIDEO DAC ELECTRICAL CHARACTERISTICS–SINGLE−ENDED MODE

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Parameter	Condition	Min	Typ	Max	Unit
Resolution		–	10	–	bits
DNL		–	0.2	0.4	bits
INL		–	0.7	3.5	bits
Output local load	Output pad (DAC_POS)	–	75	–	Ω
	Unused output (DAC_NEG)	–	0	–	Ω
Output voltage	Single−ended mode, code 000h	–	.02	–	V
	Single−ended mode, code 3FFh	–	1.30	–	V
Output current	Single−ended mode, code 000h	–	0.26	–	mA
	Single−ended mode, code 3FFh	–	17.33	–	mA
Supply current	Estimate	–	–	25.0	mA
DAC_REF	DAC Reference	–	1.15 +/−0.2	–	V
R DAC_REF	DAC Reference	–	4.7	–	KΩ

Table 42. VIDEO DAC ELECTRICAL CHARACTERISTICS–DIFFERENTIAL MODE

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Parameter	Condition	Min	Typ	Max	Unit
DNL		–	0.2	0.25	Bits
INL		–	0.8	2.5	Bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω
Output voltage	Differential mode, code 000h, pad dacp	–	.02	–	V
	Differential mode, code 000h, pad dacn	–	1.30	–	V
	Differential mode, code 3FFh, pad dacp	–	1.30	–	V
	Differential mode, code 3FFH, pad dacn	–	.02	–	V
Output current	Differential mode, code 000h, pad dacp	–	.53	–	mA
	Differential mode, code 000h, pad dacn	–	34.7	–	mA
	Differential mode, code 3FFh, pad dacp	–	34.7	–	mA
	Differential mode, code 3FFH, pad dacn	–	.53	–	mA
Differential output, midlevel		–	0.65	–	V
Supply current	Estimate	–	–	50	mA

Table 42. VIDEO DAC ELECTRICAL CHARACTERISTICS–DIFFERENTIAL MODE (continued)
^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Parameter	Condition	Min	Typ	Max	Unit
DAC_REF	DAC Reference	–	1.15 +/–0.2		V
R DAC_REF	DAC Reference		2.35		KΩ

Table 43. DIGITAL I/O PARAMETERS T_A = Ambient = 25°C; All supplies at 2.8 V

Signal	Parameter	Definitions	Condition	Min	Typ	Max	Unit
All Outputs		Load capacitance		1	–	30	pF
		Output signal slew	2.8 V, 30 pF load	–	–	–	V/ns
			2.8 V, 5 pF load	–	–	–	V/ns
	V_{OH}	Output high voltage		–	VDD_IO	–	V
	V_{OL}	Output low voltage		–0.3	–	–	V
	I_{OH}	Output high current	VDD = 2.8 V, V_{OH} = 2.4 V	–	–	8	mA
	I_{OL}	Output low current	VDD = 2.8 V, V_{OL} = 0.4V	–	–	8	mA
All Inputs	V_{IH}	Input high voltage	VDD = 2.8 V	0.7 × VDD_IO	–	VDD_IO + 0.3	V
	V_{IL}	Input low voltage	VDD = 2.8 V	–0.3	–	0.3 × VDD_IO	V
	I_{IN}	Input leakage current		–2	–	2	µA
	Signal CAP	Input signal capacitance		–	3.5	–	pF

18. All inputs are protected and may be active when All supplies (2.8 V and 1.8 V) are turned off.

Power Consumption, Operating Mode

Table 44. POWER CONSUMPTION – CONDITION 1
^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD} _IO = 2.8 V; V_{AA} =2.8 V; V_{AA}_PIX = 2.8 V; V_{DD} _PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Power Plane	Supply	Condition 1	Typ Power	Max Power	Unit
VDD	1.8		140.4	162	mW
VDD_IO	2.8	Parallel off	4.2	8.4	mW
VAA	2.8		89.6	112	mW
VAA_PIX	2.8		1.96	5.04	mW
VDD_DAC	2.8	Single 75 (Note 19)	39.2	44.8	mW
VDD_PLL	2.8		13.44	16.8	mW
		Total	288.8	349.04	mW

19. Analog output uses single−ended mode: DAC_Pos = 75 Ω, DAC_Neg = open, parallel output is disabled.

Table 45. POWER CONSUMPTION – CONDITION 2
^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} =2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Power Plane	Supply	Condition 2	Typ Power	Max Power	Unit
VDD	1.8		140.4	162	mW
VDD_IO	2.8	Parallel on	42	50.4	mW
VAA	2.8		89.6	112	mW
VAA_PIX	2.8		1.96	5.04	mW
VDD_DAC	2.8	Single 75 (Note 20)	39.2	44.8	mW

Table 45. POWER CONSUMPTION – CONDITION 2 (continued)

[f]EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} =2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Power Plane	Supply	Condition 2	Typ Power	Max Power	Unit
VDD_PLL	2.8		13.44	16.8	mW
		Total	326.6	391.04	mW

20. Analog output uses single−ended mode: DAC_Pos = 75 Ω, DAC_Neg = open, parallel output is enabled.

NTSC Signal Parameters

Table 46. NTSC SIGNAL PARAMETERS

[f]EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Line Frequency		15734.25	15734.27	15734.28	Hz	
Field Frequency		59.94	59.94	59.94	Hz	
Sync Rise Time		148	148	148	ns	
Sync Fall Time		148	148	148	ns	
Sync Width		4.74	4.74	4.74	µs	
Sync Level		38	40	42	IRE	22, 24
Burst Level		38	40	42	IRE	22, 24
Sync to Setup (with pedestal off)		9.44	9.44	9.44	µs	
Sync to Burst Start		5.33	5.33	5.33	µs	
Front Porch		1.33	1.33	1.33	µs	
Black Level			7.5		IRE	21, 22, 24
White Level			100		IRE	21, 22, 23, 24

21. Black and white levels are referenced to the blanking level.
22. NTSC convention standardized by the IRE (1 IRE = 7.14 mV).
23. Encoder contrast setting R0x011 = R0x001 = 0.4.
24. DAC ref = 2.35 kΩ, load = 37.5 Ω.

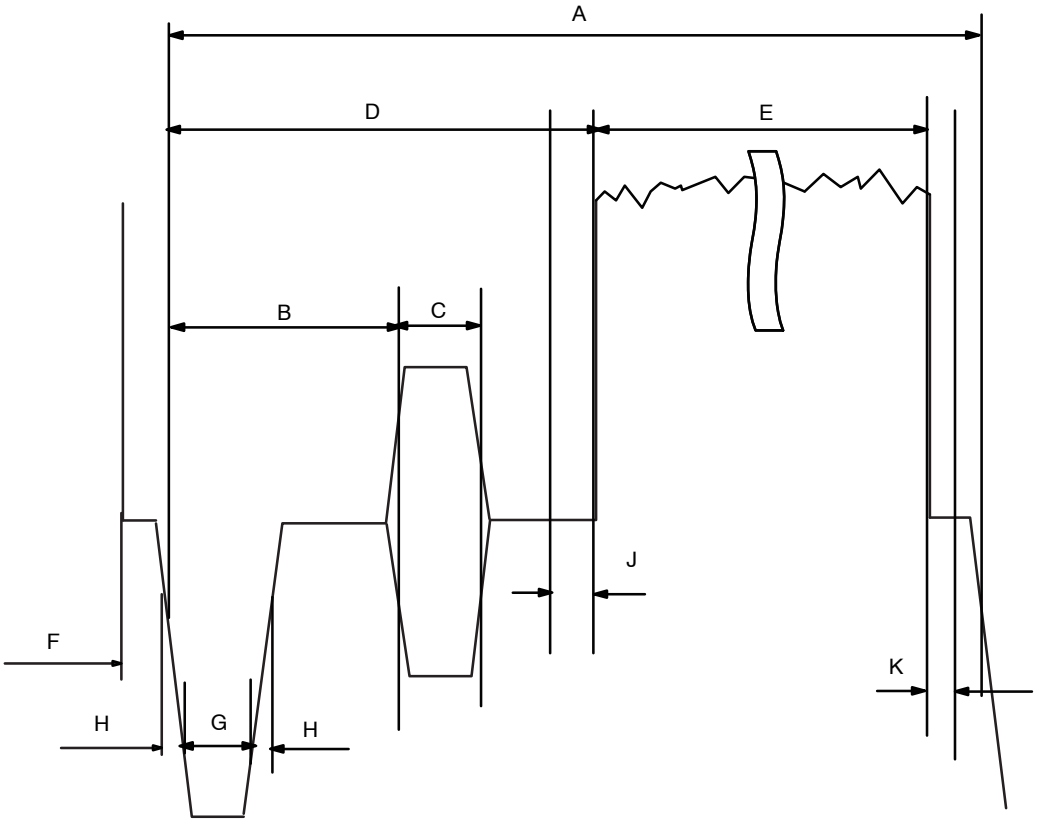


Figure 57. Video Timing

Table 47. VIDEO TIMING

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
A	H Period	1716	1728	Clocks
B	Hsync to burst	144	153	Clocks
C	burst	63	66	Clocks
D	Hsync to Signal	255	279	Clocks
E	Video Signal	1423	1413	Clocks
F	Front	36	39	Clocks
G	Hsync Period	128	128	Clocks
H	Sync rising/falling edge	4	4	Clocks
J	Back overscan (BOS)	9	14	Clocks
K	Front overscan (FOS)	8	13	Clocks

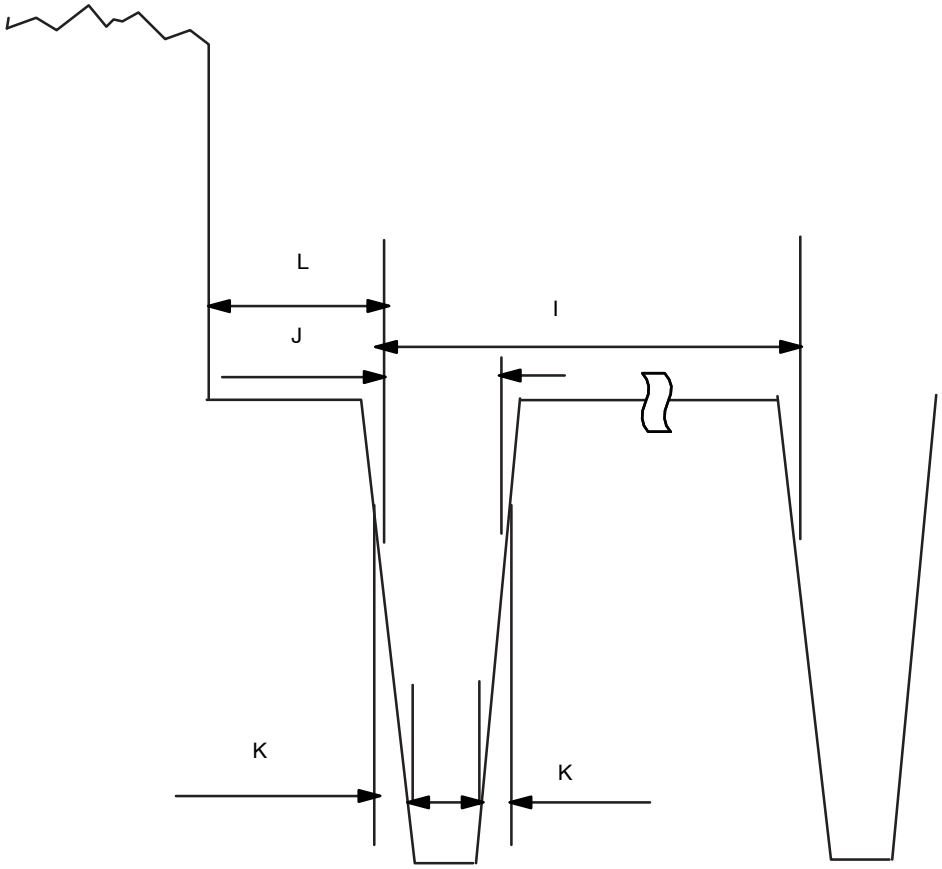


Figure 58. Equivalent Pulse

Table 48. EQUIVALENT PULSE

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
I	H/2 Period	858	864	Clocks
J	Pulse width	64	64	Clocks
K	Pulse rising/falling edge	4	4	Clocks
L	Signal to pulse	38	41	Clocks

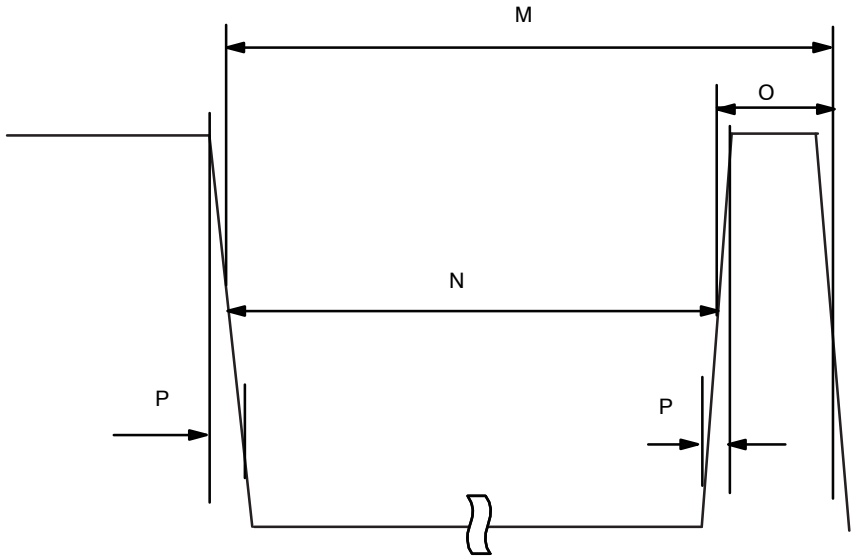


Figure 59. V Pulse

Table 49. V PULSE

	Signal	NTSC 27 MHz	PAL 27 MHz	Units
M	H/2 Period	858	864	Clocks
N	Pulse width	730	736	Clocks
O	V pulse interval	128	128	Clocks
P	Pulse rising/falling edge	4	4	Clocks

Two−Wire Serial Bus Timing

Figure 60 and Table 50 describe the timing for the two−wire serial interface.

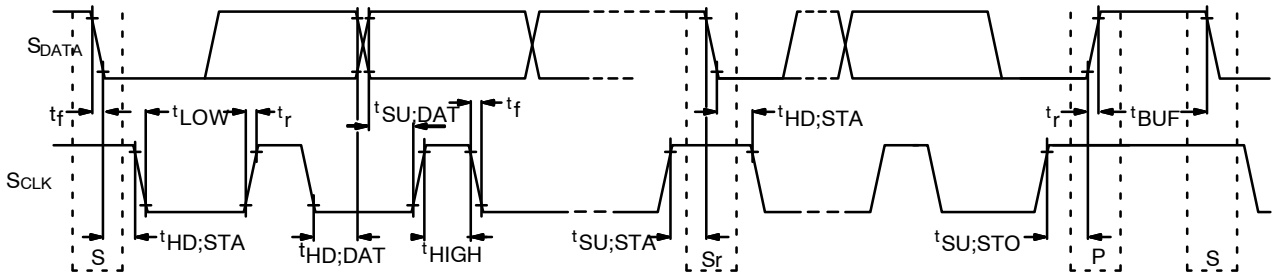


Figure 60. Two−Wire Serial Bus Timing Parameters

Table 50. TWO−WIRE SERIAL BUS CHARACTERISTICS

^{f}EXTCLK = 27 MHz; V_{DD} = 1.8 V; V_{DD}_IO = 2.8 V; V_{AA} = 2.8 V; V_{AA}_PIX = 2.8 V; V_{DD}_PLL = 2.8 V; V_{DD}_DAC = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
SCLK Clock Frequency	^{f}SCL	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	^{t}HD;STA	4.0	–	0.6	–	μS
LOW period of the SCLK clock	^{t}LOW	4.7	–	1.3	–	μS
HIGH period of the SCLK clock	^{t}HIGH	4.0	–	0.6	–	μS
Set−up time for a repeated START condition	^{t}SU;STA	4.7	–	0.6	–	μS
Data hold time:	^{t}HD;DAT	04	3.45 (Note 29)	0 (Note 30)	0.9 (Note 29)	μS
Data set−up time	^{t}SU;DAT	250	–	100 (Note 30)	–	nS
Rise time of both SDATA and SCLK signals	t_r	–	1000	20 + 0.1Cb (Note 31)	300	nS
Fall time of both SDATA and SCLK signals	t_f	–	300	20 + 0.1Cb (Note 31)	300	nS
Set−up time for STOP condition	^{t}SU;STO	4.0	–	0.6	–	μS
Bus free time between a STOP and START condition	^{t}BUF	4.7	–	1.3	–	μS
Capacitive load for each bus line	Cb	–	400	–	400	pF
Serial interface input pin capacitance	CIN_SI	–	3.3	–	3.3	pF
SDATA max load capacitance	CLOAD_SD	–	30	–	30	pF
SDATA pull−up resistor	RSD	1.5	4.7	1.5	4.7	KΩ

25. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
26. Two−wire control is I²C−compatible.
27. All values referred to V_{IHmin} = 0.9 VDD and V_{ILmax} = 0.1 VDD levels. Sensor EXCLK = 27 MHz.
28. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
29. The maximum ^{t}HD;DAT has only to be met if the device does not stretch the LOW period (^{t}LOW) of the SCLK signal.
30. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement ^{t}SU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line ^{t}r max + ^{t}SU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the SCLK line is released.
31. Cb = total capacitance of one bus line in pF.

SPECTRAL CHARACTERISTICS

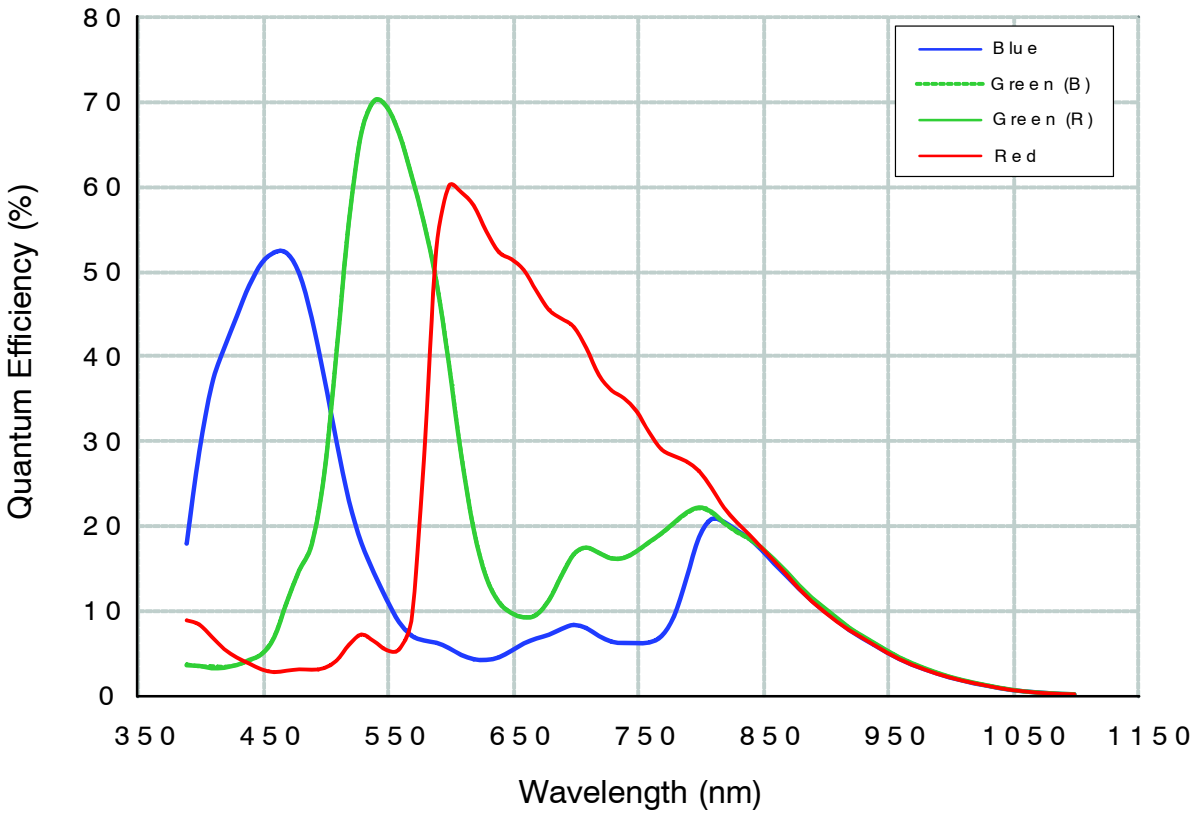


Figure 61. Quantum Efficiency

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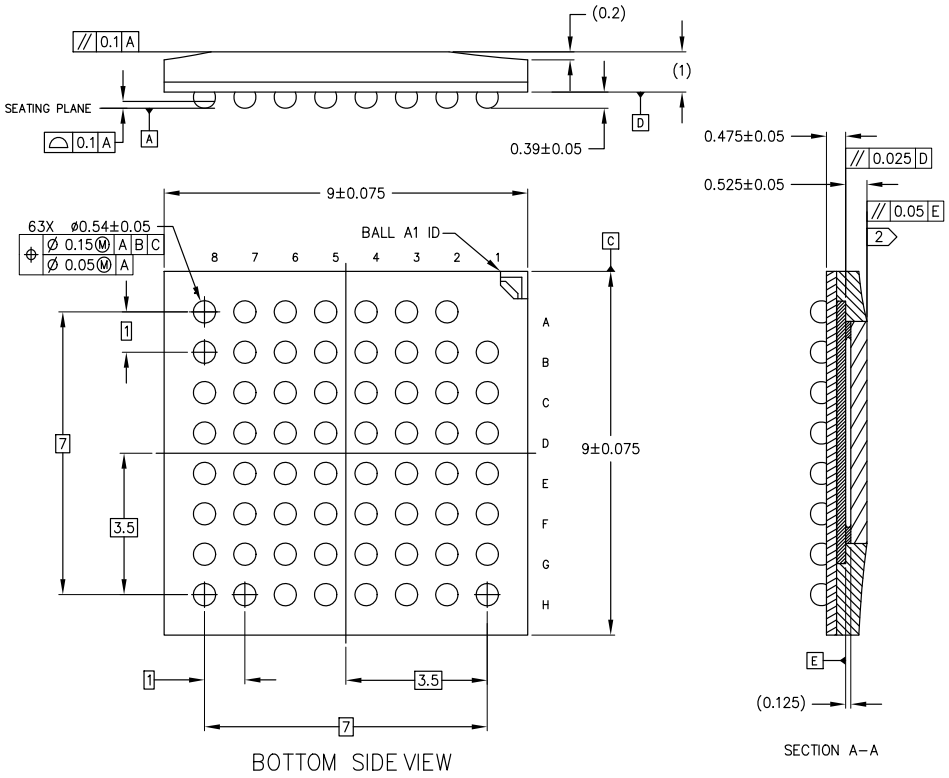

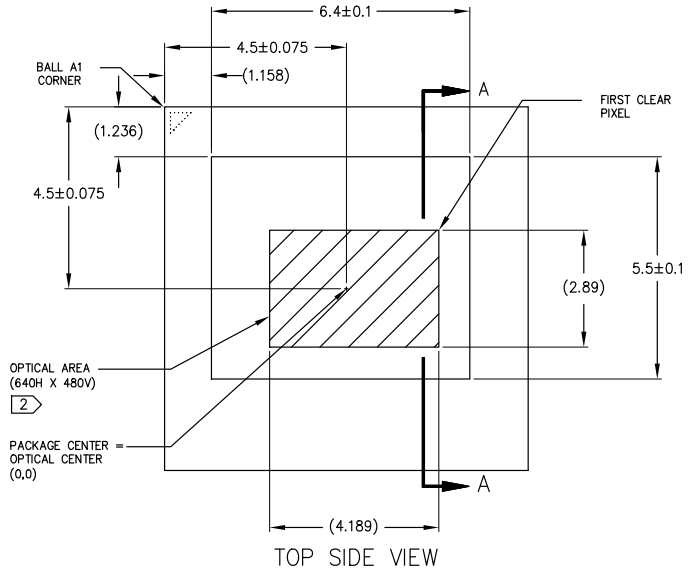

NOTES	
1	DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY.
2	MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES: 1°. MAXIMUM TILT OF OPTICAL AREA RELATIVE TO SUBSTRATE PLANE D: 25 MICRONS. MAXIMUM TILT OF COVER GLASS RELATIVE TO OPTICAL AREA PLANE E: 50 MICRONS.

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