N34TS108

Low-Voltage Digital Temperature Sensor

Description

N34TS108 is a digital-output temperature sensor with a dynamically-programmable limit window, and under- and over temperature alert functions. These features provide optimized temperature control without the need of frequent temperature readings by the controller or application processor.

The N34TS108 features SMBus ™ and two-wire interface compatibility, and allows up to three devices on one bus with the SMBus alert function.

The N34TS108 is ideal for thermal management optimization in a variety of consumer, computer, and environmental applications. The device is specified over a temperature range of –40°C to +125°C.

Features

- Dynamically-Programmable Limit Window with Under- and Over Temperature Alerts
- Accuracy:
  - ♦ ±0.75°C (max) from –20°C to +85°C
  - ♦ ±1°C (max) from –40°C to +125°C
- Low Quiescent Current:
  - ♦ 6 μA Active from –40°C to +125°C
- Supply Range: 1.4 V to 3.6 V
- Resolution: 12 Bits (0.0625°C)
- Package: 1.2-mm × 0.8-mm, 6-Ball WCSP

Typical Applications

- Smartphone and Tablet Thermal Management
- Battery Management
- Thermostat Control
- Under- and Over Temperature Protection for Environmental Monitoring and HVAC

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Supply Voltage	3.6	V
Input Voltage	–0.5 to 3.6	V
Operating Temperature	–55 to 150	°C
Junction Temperature (T_J)	150	°C
Storage Temperature (T_{stg})	–60 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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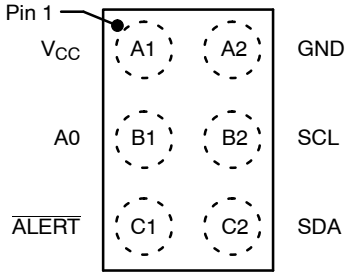
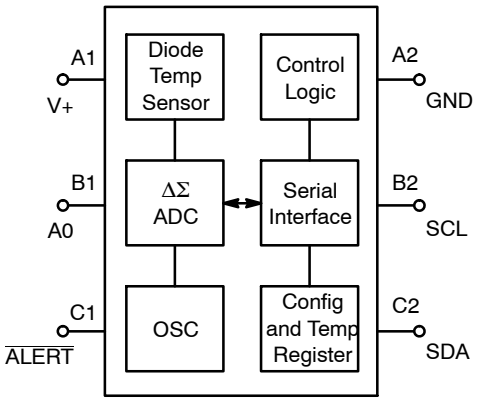
WLCSP6
C6 SUFFIX
CASE 567WQ

PIN CONFIGURATION



(Top View)

FUNCTION DIAGRAM



MARKING DIAGRAM

T = Specific Device Code
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Table 2. ESD RATINGS

ESD Rating		Value	Unit
V(ESD) Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS−001, all pins11l	±2000	V
	Charged device model (COM), per JEDEC specification JESD22−C101, all pins	±1000	V

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8 V, T_A = 25°C, unless otherwise specified)

Parameter		Conditions	Min	Typ	Max	Unit
TEMPERATURE INPUT						
Range			−40		+125	°C
Accuracy (Temperature Error)		−20°C to +85°C		±0.15	±0.75	°C
		−40°C to +125°C		±0.3	±1	°C
Accuracy vs. Supply				±0.03	±0.3	°C/V
DIGITAL INPUT/OUTPUT						
V_{IH}	Input Logic High Level		0.7 (VCC)		VCC	V
V_{IL}	Input Logic Low Level		−0.5		0.3 (VCC)	V
I_{IN}	Input Current	0 V < V_{IN} < (VCC) +0.3 V			1	μA
V_{OL}	Output Logic Low Level	VCC > 2 V, I_{OUT} = 3 mA			0.4	V
		VCC < 2 V, I_{OUT} = 3 mA			0.2 (VCC)	V
$\overline{ALERT}$ Internal Pull-up Resistor		$\overline{ALERT}$ to VCC	80	100	120	kΩ
Resolution				12		Bit
Conversion Time		One-Shot mode	17	22	28	ms
Conversion Modes		CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1 (default)		1		Conv/s
		CR1 = 1, CR0 = 0		4		Conv/s
		CR1 = 1, CR0 = 1		16		Conv/s
Timeout Time			21	30	35	ms
POWER SUPPLY						
Operating Supply Range, VCC Pin			1.4		3.6	V
I_Q	Quiescent Current	Serial bus inactive, CR1 = 0, CR0 = 1 (default)		3.1	3.6	μA
		Serial bus inactive, CR1 = 0, CR0 = 1 (default), −40°C to +125°C		6		μA
		Serial bus active, SCL frequency = 400 kHz, CR1 = 0, CR0 = 1 (default)		8		μA
		Serial bus active, SCL frequency = 3.4 MHz, CR1 = 0, CR0 = 1 (default)		41		μA
I_{SD}	Shutdown Current	Serial bus inactive		2.5	3.1	μA
		Serial bus active, SCL frequency = 400 kHz		8		μA
		Serial bus active, SCL frequency = 3.4 MHz		41		μA
TEMPERATURE						
Specified Range			−40		+125	°C
Storage Range			−55		+150	°C

Table 4. A.C. OPERATING CHARACTERISTICS (V_{CC} = 1.4 V to 3.6 V, T_A = −40°C to +125°C)

Parameter	Test Conditions	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL Operating Frequency, VCC ≥ 1.8 V	0.001	0.4	0.001	3.4	MHz
	SCL Operating Frequency, VCC < 1.8 V	0.001	0.4	0.001	2.5	MHz
$t_{(BUF)}$	Bus Free Time between Stop and Start Conditions, VCC	1300		160		ns
	Bus Free Time between Stop and Start Conditions, VCC	1300		260		ns
$t_{(HDSTA)}$	Hold Time after Repeated Start Condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated Start Condition Setup Time	600		160		ns
$t_{(SUSTO)}$	Stop Condition Setup Time	600		160		ns
$t_{(HDDAT)}$	Data Hold Time, VCC ≥ 1.8 V	0	900	0	70	ns
	Data Hold Time, VCC < 1.8 V	0	900	0	130	ns
$t_{(SUDAT)}$	Data Setup Time, VCC ≥ 1.8 V	100		10		ns
	Data Setup Time, VCC < 1.8 V	100		50		ns
$t_{(LOW)}$	SCL Clock Low Period, VCC ≥ 1.8 V	1300		160		ns
	SCL Clock Low Period, VCC < 1.8 V	1300		260		ns
$t_{(HIGH)}$	SCL Clock High Period	600		60		ns
t_R, t_F – SDA	Data Rise/Fall Time		300		80	ns
t_R, t_F – SCL	Clock Rise/Fall Time		300		40	ns
t_R	Clock/Data Rise Time for SCLK ≤ 100 kHz		1000			ns

1. For the N34TS108, the interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time-out count takes place when SCL is low in the time interval between START and STOP.
2. In a “Wired-OR” system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull-down device must be able to sink the (external) bus pull-up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} – t_{DH} – t_{SU:DAT}$, where t_{LOW} and t_{DH} are actual values (rather than spec limits). A shorter t_{DH} leaves more room for a longer SDA t_R, allowing for a more capacitive bus or a larger bus pull-up resistor.
3. The first valid temperature recording can be expected after t_{PU} at nominal supply voltage.

Table 5. PIN CAPACITANCE (V_{CC} = 3.6 V, T_A = 25°C, f = 400 kHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (SCL)	V_{IN} = 0		6	pF

Table 6. PIN DESCRIPTIONS

Pin Name	Ball Number	Description
A0	B1	Address selection pin
$\overline{\text{ALERT}}$	C1	Alert output pin
GND	A2	Ground
SCL	B2	Input clock pin
SDA	C2	Input/output data pin
VCC	A1	Supply Voltage (1.4 V to 3.6 V)

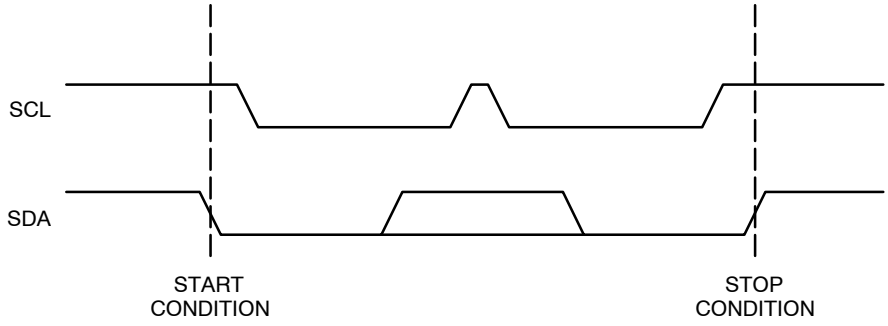


Figure 1. START/STOP Timing

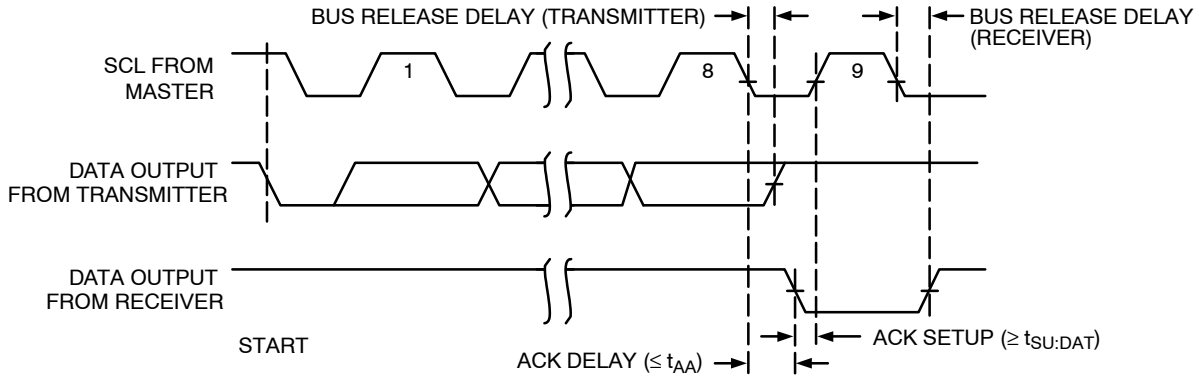


Figure 2. Acknowledge Timing

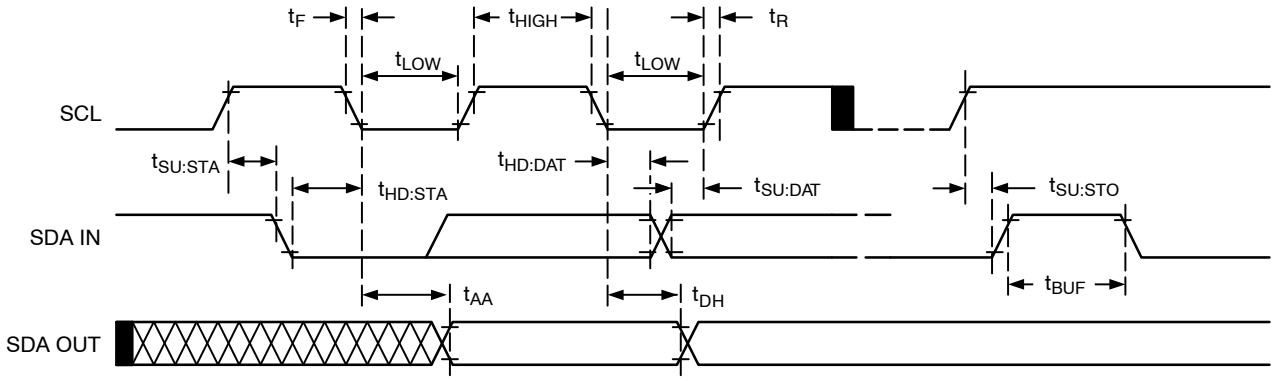


Figure 3. Bus Timing

OVERVIEW

The N34TS108 is a digital temperature sensor optimal for thermal management and thermal protection applications. The N34TS108 is two-wire and SMBus Interface compatible, and is specified over a temperature range of −40°C to +125°C.

The N34TS108 temperature sensor is the chip itself; the solder bumps provide the primary thermal path as a result of the lower thermal resistance of metal. The temperature sensor result is equivalent to the local temperature of the printed circuit board (PCB) on which the sensor is mounted.

The N34TS108 only requires pull-up resistors on SCL and SDA; although, a 0.01 μF bypass capacitor is recommended. There is an internal 100 kΩ pull-up resistor connected to supply on the $\overline{\text{ALERT}}$ pin. If required, use an external resistor of smaller value on the $\overline{\text{ALERT}}$ pin for a stronger pull-up to VCC. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than VCC through the pull-up resistors. To configure one of three different addresses on the bus, connect AO to either VCC, GND, or SDA. If AO is connected to SDA, make its pull-up supply equal to VCC.

POINTER REGISTER

Figure 4 shows the internal register structure of the N34TS108. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs (see Table 16) to identify which of the data registers respond to a read or write command. Table 7 identifies the bits of the pointer register byte. Table 8 describes the pointer address of the registers available in the N34TS108. The power-up reset value of the P1 and P0 bits is '00'.

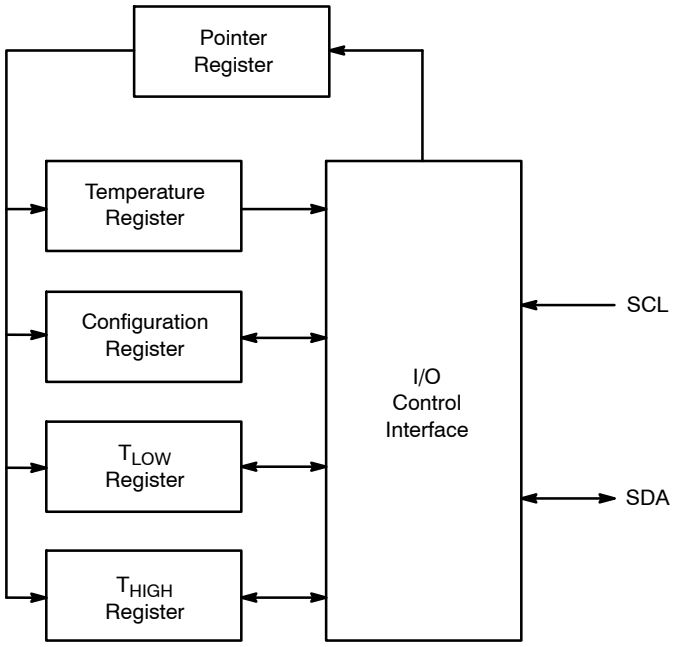


Figure 4. Internal Register Structure

Table 7. POINTER REGISTER BYTE

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

Table 8. POINTER ADDRESSES

P1	P0	Register
0	0	Temperature Register (Read Only, Default)
0	1	Configuration Register (Read/write)
1	0	T_{LOW} Register (Read/Write)
1	1	T_{HIGH} Register (Read/Write)

TEMPERATURE REGISTER

The temperature register is configured as a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, as shown in Table 9 and Table 10. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits are used to indicate temperature. There is no requirement to read the least significant byte if that information is not needed (for example, for resolution lower than 1°C). Table 5 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. The unused bits in the temperature register always read '0'.

Table 9. BYTE 1 OF TEMPERATURE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

Table 10. BYTE 2 OF TEMPERATURE REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

Table 11. TEMPERATURE DATA FORMAT (Note 4)

Temperature (°C)	Digital Output	
	Binary	Hex
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

4. The temperature sensor ADC resolution is 0.0625°C/count.

Table 11 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature.

- To convert positive temperatures to a digital data format:
  Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.
  Example: (+50°C)/(0.0625°C/count) = 800 = 320h = 0011 0010 0000
- To convert negative temperatures to a digital data format:
  Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.
  Example: (|–25°C|)/(0.0625°C/count) = 400 = 190h = 0001 1001 0000
  Twos complement format: 1110 0110 1111 + 1 = 1110 0111 0000

CONFIGURATION REGISTER

The configuration register is a 16-bit read and write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format and power-up (reset) default value of the configuration register is shown in Table 12, followed by an explanation of the register bits. Other options for the default values are available by request.

Table 12. CONFIGURATION AND POWER-UP/RESET FORMAT

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	ID	CR1	CR0	FH	FL	TM	M1	M0
	0	0	1	0	0	1	1	0
2	POL	0	HYS1	HYS0	0	0	0	0
	0	0	0	1	0	0	0	0

Hysteresis Control (HYS1 and HYS0)

When operating in comparator mode, the hysteresis control bits (HYS1 and HYS0) configure the hysteresis for the limit comparison of the N34TS108 to 0°C, 1°C, 2°C, or 4°C. The default hysteresis is 1°C. Table 13 shows the settings for HYS1 and HYS0.

Table 13. HYSTERESIS SETTINGS

HYS1	HYS2	Hysteresis
0	0	0°C
0	1	1°C (Default)
1	0	2°C
1	1	4°C

Polarity (POL)

The polarity of the $\overline{\text{ALERT}}$ pin can be programmed using the POL bit. If POL = ‘0’ (default), the $\overline{\text{ALERT}}$ is active low. For POL = ‘1’, the $\overline{\text{ALERT}}$ pin is active high, and the state of the $\overline{\text{ALERT}}$ pin is inverted.

Mode Bits (M1 and M0)

The mode bits, M1 and M0, can be set to three different modes: shutdown, one-shot, or continuous conversion.

Shutdown Mode (M1 = ‘0’, M0 = ‘0’)

Shutdown mode saves power by shutting down all device circuitry other than the serial interface, thus reducing current consumption to typically less than 2.5 μA. Shutdown mode is enabled when M1 and M0 = ‘00’. The device shuts down when current conversion is completed.

One-Shot Mode (M1 = ‘0’, M0 = ‘1’)

The N34TS108 features a *one-shot* temperature measurement mode. When the device is in shutdown mode, writing a ‘01’ to the M1 and M0 bits starts a single temperature conversion. During the conversion, the M1 and M0 bits reads ‘01’. The device returns to the shutdown state at the completion of the single conversion. After the conversion, the M1 and M0 bits read ‘00’. This feature is useful for reducing the power consumption of the N34TS108 when continuous temperature monitoring is not required.

As a result of the short conversion time, the N34TS108 can achieve a higher conversion rate. A single conversion typically takes 22 ms and a read can take place in less than 20 μs. However, when using one-shot mode, 30 or more conversions per second are possible.

Continuous Conversion Mode (M1 = ‘1’)

When the N34TS108 is in continuous conversion mode (M1 = ‘1’), a single conversion is performed at a rate determined by the conversion rate bits (CR1 and CR0 in the configuration register). The N34TS108 performs a single conversion, and then goes in standby and waits for the appropriate delay set by the CR1 and CR0 bits. See Table 14 for CR1 and CR0 settings.

Thermostat Mode (TM)

The thermostat mode bit indicates to the device whether to operate in comparator mode (TM = ‘0’) or interrupt mode (TM = ‘1’, default). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

Temperature Watchdog Flags (FL and FH)

The N34TS108 uses temperature watchdog flags in the configuration register that indicate the result of comparing the device temperature at the end of every conversion to the values stored in the temperature limit registers (T_{HIGH} and T_{LOW}). If the temperature of the N34TS108 exceeds the value in the T_{HIGH} register, then the flag-high bit (FH) in the configuration register is set to '1'. If the temperature falls below the value in the T_{LOW} register, then the flag-low bit (FL) is set to '1'. If both flag bits remain '0', then the temperature is within the temperature range set by the temperature limit registers. In interrupt mode, when any of the flags is set by an under- or over-temperature event, the SMBus $\overline{\text{ALERT}}$ Response only clears the pin and not the flags. Reading the configuration register clears both the flags and the pin unless the device is in comparator mode.

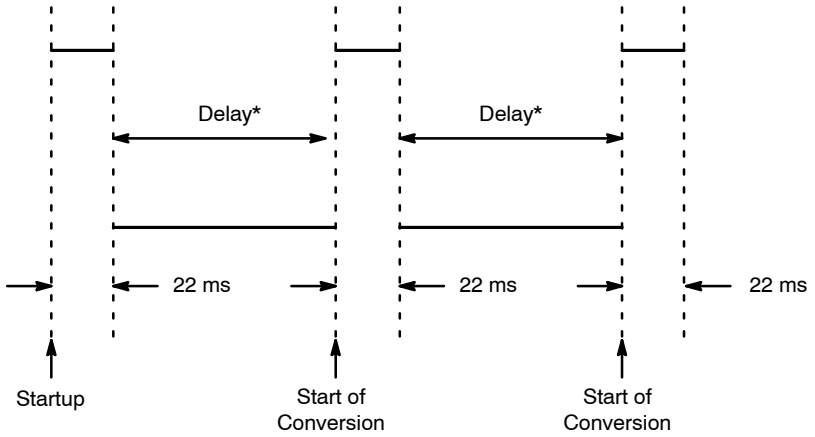
Conversion Rate

The conversion rate bits, CR1 and CR0, configure the N34TS108 for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 16 Hz. The default rate is 1 Hz. The N34TS108 has a typical conversion time of 22 ms. To achieve different conversion rates, the N34TS108 makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 14 shows the settings for CR1 and CR0.

Table 14. CONVERSION RATE SETTINGS

CR1	CR0	Conversion Rate	I_Q (Typ)
0	0	0.25 Hz	3 μA
0	1	1 Hz (Default)	4 μA
1	0	4 Hz	5 μA
1	1	16 Hz	13 μA

After power-up or a general-call reset, the N34TS108 immediately starts a conversion, as shown in Figure 5. The first result is available after 22 ms (typical). The active quiescent current during conversion is 27 μA (typical at +25°C). The quiescent current during delay is 2.5 μA (typical at +25°C).



*Delay is set by the CR1 and CR0 bits in the configuration register.

Figure 5. Conversion Start

HIGH- AND LOW-LIMIT REGISTERS

In comparator mode (TM = '0'), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register. The $\overline{\text{ALERT}}$ pin remains active until the temperature returns to a value that is within the range set by:

$$(T_{LOW} + HYS) \text{ and } (T_{HIGH} - HYS) \qquad \text{(eq. 1)}$$

Where:

HYS is the hysteresis set by the hysteresis control bits (HYS1 and HYS0).

In interrupt mode (TM = '1'), the $\overline{\text{ALERT}}$ pin becomes active when the temperature exceeds the value in the T_{HIGH} register or drops below the value in the T_{LOW} register, and remains active until a read operation of the configuration register occurs (also clears the values latched in the watchdog flags, FL and FH), or the device successfully responds to the SMBus alert response address. The $\overline{\text{ALERT}}$ pin is also cleared by resetting the device with the general call reset command.

Both operational modes are represented in Figure 6 and Figure 7.

Table 15 and Table 16 describe the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up (reset) default values are T_{HIGH} = +127.9375°C and T_{LOW} = –128°C. These values ensure that upon power-up, the limit window is set to maximum, and the $\overline{ALERT}$ pin does not become active until the desired limit values are programmed in the registers. Other default values for the temperature limits are available by request. The format of the data for T_{HIGH} and T_{LOW} is the same as for the temperature register.

Table 15. BYTES 1 AND 2 OF T_{HIGH} REGISTER

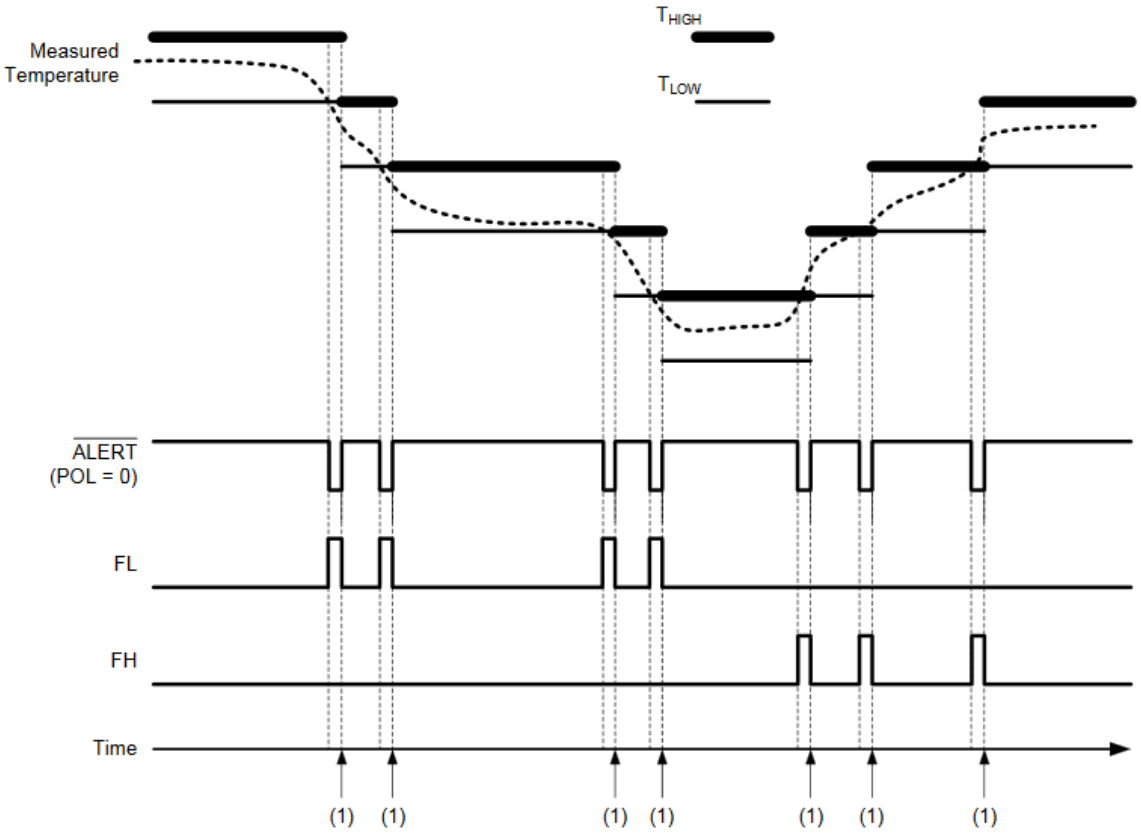
Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

Byte	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

Table 16. BYTES 1 AND 2 OF T_{LOW} REGISTER

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Byte	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0



NOTE: Update T_{HIGH} and T_{LOW} limit. Read the configuration register to clear the flags and the $\overline{ALERT}$ pin.

Figure 6. Interrupt Mode

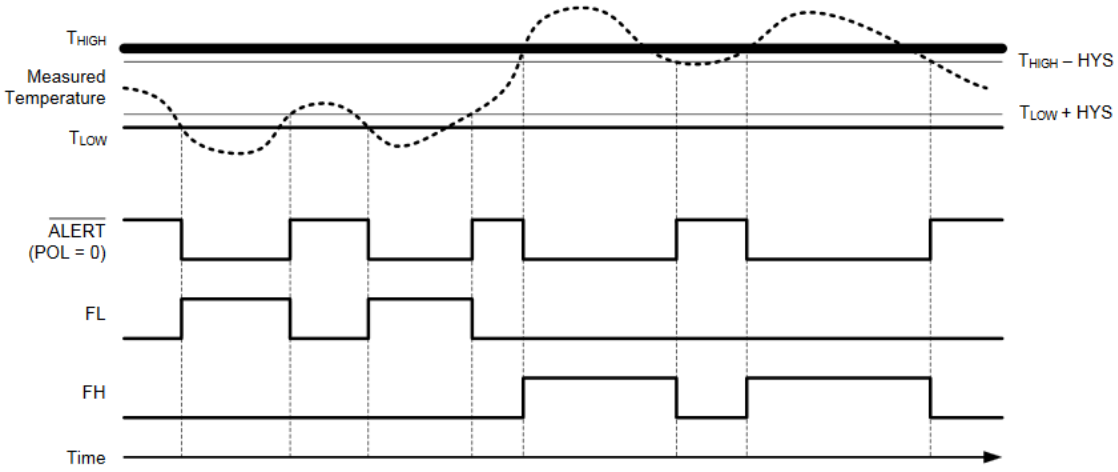


Figure 7. Comparator Mode

SERIAL INTERFACE

The N34TS108 operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The N34TS108 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted MSB first.

SERIAL BUS ADDRESS

To communicate with the N34TS108, the master must first communicate with slave devices using a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The N34TS108 features an address pin that allows up to three devices to be addressed on a single bus. The N34TS108 latches the status of the address pin at the start of a communication. Table 17 describes the pin logic levels and the corresponding address values. Other values for the fixed address bits are available by request.

Table 17. ADDRESS PIN AND SLAVE ADDRESSES

Device Two-wire Address	A0 Pin Connection
1001000	GND
1001001	VCC
1001010	SDA
1001011	SCL

BUS OVERVIEW

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the start and stop

conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte; the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the master generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

WRITING/READING OPERATION

Accessing a particular register on the N34TS108 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the N34TS108 requires a value for the pointer register.

When reading from the N34TS108, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value

must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The master can then generate a start condition and send the slave address byte with the R/W bit high to initiate the read command. If repeated reads from the same register are desired, it is not necessary to continually send the pointer register bytes because the N34TS108 stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

SLAVE MODE OPERATIONS

The N34TS108 can operate as a slave receiver or slave transmitter.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/W bit low. The N34TS108 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The N34TS108 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The N34TS108 acknowledges reception of each data byte. The master can terminate data transfer by generating a start or stop condition.

Slave Transmitter Mode:

The first byte transmitted by the master is the slave address, with the R/W bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

SMBus ALERT FUNCTION

The N34TS108 supports the SMBus alert function. When the N34TS108 operates in interrupt mode (TM = ‘1’), the $\overline{\text{ALERT}}$ pin may be connected as an SMBus alert signal. When a master senses that an alert condition is present on the $\overline{\text{ALERT}}$ line, the master sends an SMBus alert command (00011001) to the bus. If the $\overline{\text{ALERT}}$ pin is active, the device acknowledges the SMBus alert command and responds by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates whether the alert condition is caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. The LSB is high if the temperature is greater than T_{HIGH}, or low if the temperature is less than T_{LOW}.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears its alert status first. If the N34TS108 wins the arbitration, its $\overline{\text{ALERT}}$ pin becomes inactive at the completion of the SMBus alert command. If the N34TS108 loses the arbitration, its $\overline{\text{ALERT}}$ pin remains active.

GENERAL CALL

The N34TS108 responds to a two-wire general call address (0000000) if the eighth bit is ‘0’. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is

00000100, the N34TS108 latches the status of the address pin, but does not reset. If the second byte is 00000110, the N34TS108 internal registers are reset to power-up values. The N34TS108 does not support the general address acquire command.

HIGH-SPEED (Hs) MODE

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an SMBus Hs-mode master code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The N34TS108 does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4 MHz. After the Hs-mode master code has been issued, the master transmits a two-wire slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the N34TS108 switches the input and output filters back to fast-mode operation.

TIMEOUT FUNCTION

The N34TS108 resets the serial interface if SCL or SDA are held low for 30 ms (typ) between a start and stop condition. If the N34TS108 is pulled low, it releases the bus and then waits for a start condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency.

Table 18. ORDERING INFORMATION

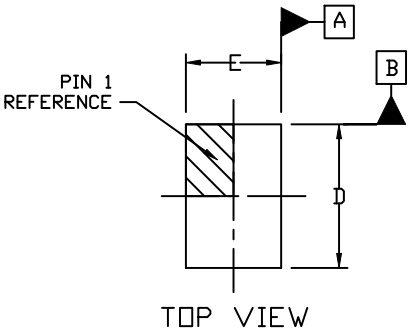
Device Order Number	Marking	Package Type	Temperature Range	Shipping†
N34TS108C6EXT5G	T	WLCSP 6-ball	−40°C to +125°C	5,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

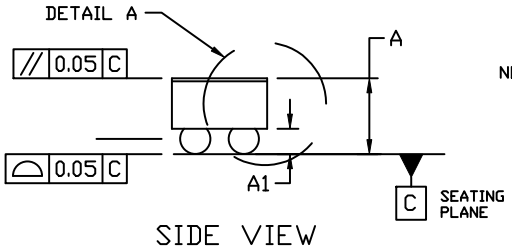
5. All packages are RoHS-compliant (Lead-free, Halogen-free).
6. The standard lead/ball finish is SnAgCu.

PACKAGE DIMENSIONS

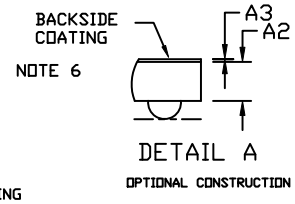
WLCSP6 1.2x0.8x0.62
CASE 567WQ
ISSUE O

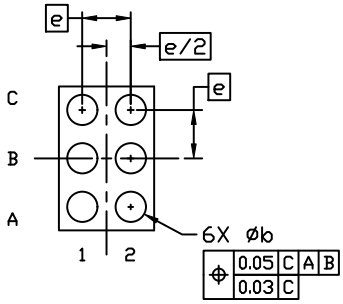


TOP VIEW



SIDE VIEW



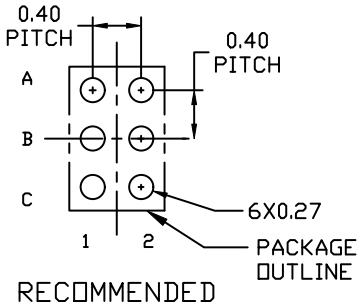


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING IS OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.62
A1	0.16	0.195	0.23
A2	0.35 REF		
A3	0.025 REF		
b	0.24	0.27	0.30
D	1.18	1.20	1.22
E	0.78	0.80	0.82
e	0.40 BSC		



RECOMMENDED
MOUNTING FOOTPRINT

SMBus is a trademark of Intel Corporation

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