N64L1603

Product Preview

16-bit Programmable LED Dimmer with I²C Interface

ON Semiconductor®

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Description

The N64L1603 is a CMOS device that provides 16−bit parallel input/output port expander optimized for LED dimming control. The N64L1603 outputs can drive directly 16 LEDs in parallel. Each individual LED may be turned ON, OFF, or blinking at one of two programmable rates. The device provides a simple solution for dimming LEDs in 256 brightness steps for backlight and color mixing applications. The N64L1603 is suitable in I²C and SMBus compatible applications where it is necessary to limit the bus traffic or free−up the bus master's timer.

The N64L1603 contains an internal oscillator and two OSC signals that drive the LED outputs. The user can program the period for each individual OSC signal. A command from the bus master is turns each individual open drain output ON, OFF, or cycle at Blink Rate 1 or Blink Rate 2. Each output has an individual 8−bit PWM controller that can be programmed with a duty cycle between 0% and 99.6%. An open drain LED output can provide a maximum output current of 25 mA. The total current sunk by all I/Os must not exceed 400 mA.

Features

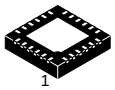
- 16 LED Drivers with Dimming Control
- 256 Brightness Steps
- 16 Open Drain Outputs Drive 25 mA Each
- 2 Selectable Programmable Blink Rates:
  - Frequency: 0.593 Hz to 152 Hz
- 8−bit Programmable Duty Cycle for Each Output
- I/Os can be Used as GPIOs
- 400 kHz I²C Bus Compatible
- 2.3 V to 5.5 V Operation
- 5 V Tolerant I/Os
- Active Low Reset Input
- 24−pad WQFN (4 x 4 mm) Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Backlighting
- RGB Color Mixing
- Sensors−Control
- Power Switches
- Alarm Systems

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM

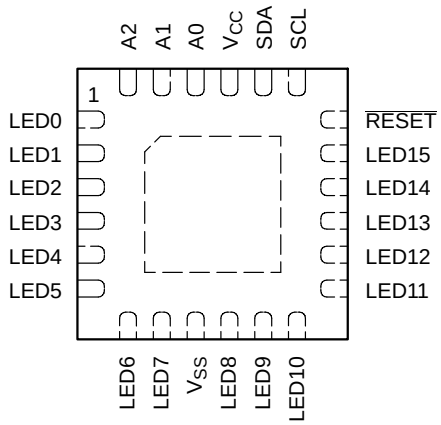


WQFN24
HV6 SUFFIX
CASE 485BG

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.



TQFN (HV6)
(Top View)

Figure 1. Pin Configuration

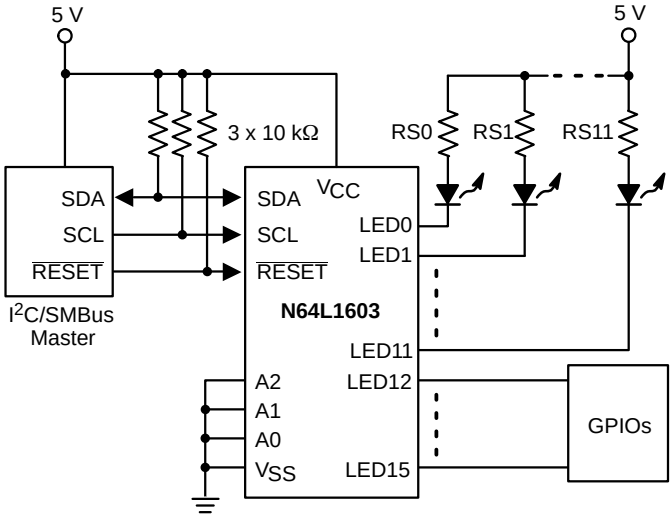


Figure 2. Typical Application Circuit

Table 1. ORDERING INFORMATION

Device Order Number	Lead Finish	Package	Shipping†
N64L1603MNDTG	NiPdAu	WQFN24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 2. PIN DESCRIPTION

WQFN	Pad Name	Function
1−8	LED0 − LED7	LED Driver Output 0 to 7, I/O Port 0 to 7
9	V_{SS}	Ground
10−17	LED8 − LED15	LED Driver Output 8 to 15, I/O Port 8 to 15
18	$\overline{\text{RESET}}$	Reset Input
19	SCL	Serial Clock
20	SDA	Serial Data
21	V_{CC}	Power Supply
22	A0	Address Input 0
23	A1	Address Input 1
24	A2	Address Input 2

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	−0.3 to +7.0	V
Voltage on Any Pin with Respect to Ground	−0.3 to +5.5	V
DC Current on I/Os	±25	mA
Supply Current	400	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C
Lead Soldering Temperature (10 seconds)	300	°C
Operating Ambient Temperature	−40 to +85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 to 5.5 V, V_{SS} = 0 V; T_A = −40°C to +85°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply Voltage		2.3	−	5.5	V
I_{CC}	Supply Current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	−	250	550	μA
I_{stb}	Standby Current	Standby mode; V_{CC} = 5.5 V; no load; V_I = V_{SS} or V_{CC}, f_{SCL} = 0 kHz	−	2.1	7.0	μA
ΔI_{stb}	Additional Standby Current	Standby mode; V_{CC} = 5.5 V; every LED I/O = V_{IN} = 4.3 V, f_{SCL} = 0 kHz	−	−	2	mA
V_{POR} (Note 1)	Power−on Reset Voltage	V_{CC} = 3.3 V, No load; V_I = V_{CC} or V_{SS}	−	1.5	2.2	V
SCL, SDA, A0, A1, A2						
V_{IL} (Note 2)	Low Level Input Voltage		−0.3	−	0.3 V_{CC}	V
V_{IH} (Note 2)	High Level Input Voltage		0.7 V_{CC}	−	5.5	V
I_{OL}	Low Level Output Current	V_{OL} = 0.4 V	3	−	−	mA
I_{IL}	Leakage Current	V_I = V_{CC} = V_{SS}	−1	−	+1	μA
C_I (Note 3)	Input Capacitance	V_I = V_{SS}	−	−	6	pF
C_O (Note 3)	Output Capacitance	V_O = V_{SS}	−	−	8	pF
I/Os						
V_{IL} (Note 2)	Low Level Input Voltage		−0.3	−	0.3 V_{CC}	V
V_{IH} (Note 2)	High Level Input Voltage		0.7 V_{CC}	−	5.5	V
I_{OL} (Note 4)	Low Level Output Current	V_{OL} = 0.4 V; V_{CC} = 2.3 V	9	−	−	mA
		V_{OL} = 0.4 V; V_{CC} = 3.0 V	12	−	−	
		V_{OL} = 0.4 V; V_{CC} = 5.0 V	15	−	−	
		V_{OL} = 0.7 V; V_{CC} = 2.3 V	15	−	−	
		V_{OL} = 0.7 V; V_{CC} = 3.0 V	20	−	−	
		V_{OL} = 0.7 V; V_{CC} = 5.0 V	25	−	−	
I_{IL}	Input Leakage Current	V_{CC} = 3.6 V; V_I = V_{SS} or V_{CC}	−1	−	1	μA
$C_{I/O}$ (Note 3)	Input/Output Capacitance		−	−	8	pF
$\overline{\text{RESET}}$						
V_{IL} (Note 2)	Low Level Input Voltage		−0.3	−	0.3 V_{CC}	V
V_{IH} (Note 2)	High Level Input Voltage		0.7 V_{CC}	−	5.5	V
I_{IL}	Input Leakage Current	V_I = V_{CC} or V_{SS}	−1	−	1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. V_{CC} must be lowered to 0.2 V in order to reset the device.
2. V_{IL} min and V_{IH} max are reference values only and are not tested.
3. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
4. The output current must be limited to a maximum 25 mA per each I/O; the total current sunk by all I/O must be limited to 400 mA.

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified) (Note 5)

Symbol	Parameter	Standard I^2C		Fast I^2C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 6)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 6)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		50		50	ns
PORT TIMING						
t_{PV}	Output Data Valid				200	ns
t_{PS}	Input Data Setup Time			100		ns
t_{PH}	Input Data Hold Time			1		μs
RESET						
t_W (Note 6)	Reset Pulse Width			20		ns
t_{REC}	Reset Recovery Time			0		ns
t_{RESET} (Note 7)	Time to Reset			400		ns

5. Test conditions according to “AC Test Conditions” table.
6. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
7. The full delay to reset the part will be the sum of t_{RESET} and the RC time constant of the SDA line.

Table 6. AC TEST CONDITIONS

Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}
Input Rise and Fall Times	≤5 ns
Input Reference Voltage	0.3 V_{CC}, 0.7 V_{CC}
Output Reference Voltage	0.5 V_{CC}
Output Load	Current source: I_{OL} = 3 mA; 400 pF for $f_{SCL(max)}$ = 400 kHz

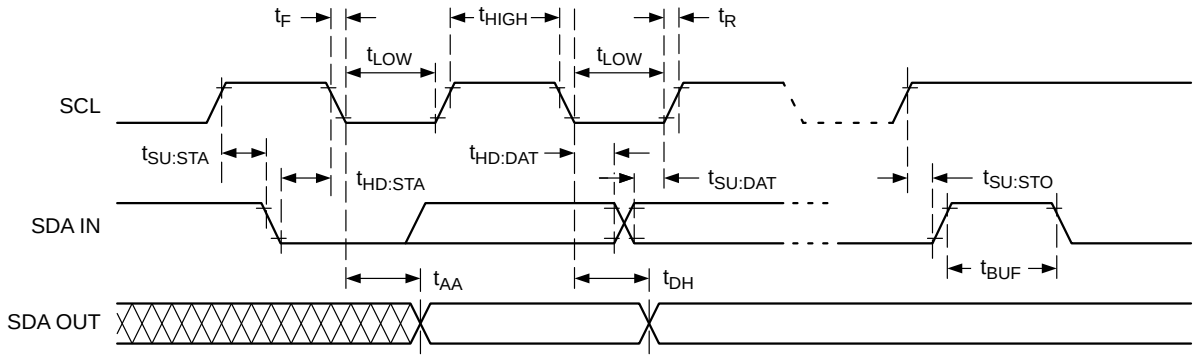


Figure 3. 2−Wire Serial Interface Timing

PIN DESCRIPTION

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{CC}.

LED0 to LED15: LED Driver Outputs / General Purpose I/Os

The pins are open drain outputs used to drive directly LEDs. Any of these pins can be programmed to drive the LED ON, OFF, Blink Rate1 or Blink Rate2. When not used for controlling the LEDs, these pins may be used as general purpose parallel input/output.

$\overline{\text{RESET}}$: External Reset Input

Active low Reset input is used to initialize the N64L1603 internal registers and the I^2C state machine. The internal registers are held in their default state while Reset input is active. An external pull−up resistor of maximum 25 kΩ is required when this pin is not actively driven.

FUNCTIONAL DESCRIPTION

The N64L1603 is a 16−bit I/O bus expander that provides a programmable LED dimmer, controlled through an I^2C compatible serial interface.

The N64L1603 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The N64L1603 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 4).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The N64L1603 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the N64L1603 for a read or write operation. The four most significant bits of the slave address are fixed as binary 1101 (Figure 5). The N64L1603 uses the next three bits as address bits.

The address bits A2, A1 and A0 are used to select which device is accessed from maximum eight devices on the same bus. These bits must compare to their hardwired input pins. The 8th bit following the 7−bit slave address is the R/W bit

that specifies whether a read or write operation is to be performed. When this bit is set to “1”, a read operation is initiated, and when set to “0”, a write operation is selected.

Following the START condition and the slave address byte, the N64L1603 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The N64L1603 then performs a read or a write operation depending on the state of the R/W bit.

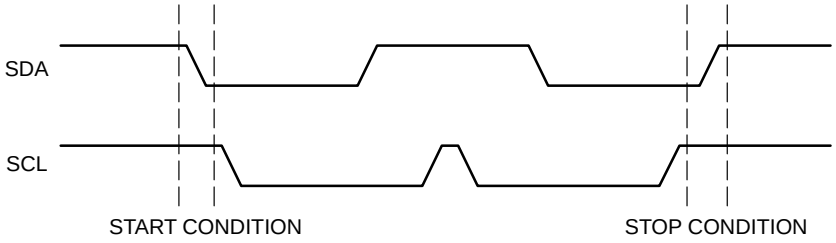


Figure 4. Start/Stop Timing

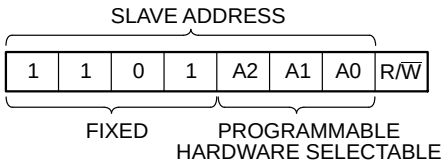


Figure 5. N64L1603 Slave Address

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 6).

The N64L1603 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8− bit byte.

When the N64L1603 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the N64L1603 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the N64L1603 to the standby power mode and place the device in a known state.

Registers and Bus Transactions

After the successful acknowledgement of the slave address, the bus master will send a command byte to the N64L1603 which will be stored in the Control Register. The format of the Control Register is shown in Figure 7.

The Control Register acts as a pointer to determine which register will be written or read. The five least significant bits, B0, B1, B2, B3 and B4 are used to select which internal register is accessed, according to the Table 7.

If the auto increment flag (AI) is set, the five least significant bits of the Control Register are automatically incremented after a read or write operation. This allows the user to access the N64L1603 internal registers sequentially. The content of these bits will rollover to “00000” after the last register is accessed.

Table 7. INTERNAL REGISTERS SELECTION

B4	B3	B2	B1	B0	Register Name	Type	Description
0	0	0	0	0	INPUT0	READ	Input Register 0
0	0	0	0	1	INPUT1	READ	Input Register 1
0	0	0	1	0	PSCA	READ/WRITE	Frequency Prescaler A
0	0	0	1	1	PSCB	READ/WRITE	Frequency Prescaler B
0	0	1	0	0	PWM0	READ/WRITE	Duty Cycle Control LED0
0	0	1	0	1	PWM1	READ/WRITE	Duty Cycle Control LED1
0	0	1	1	0	PWM2	READ/WRITE	Duty Cycle Control LED2
0	0	1	1	1	PWM3	READ/WRITE	Duty Cycle Control LED3

Table 7. INTERNAL REGISTERS SELECTION

B4	B3	B2	B1	B0	Register Name	Type	Description
0	1	0	0	0	PWM4	READ/WRITE	Duty Cycle Control LED4
0	1	0	0	1	PWM5	READ/WRITE	Duty Cycle Control LED5
0	1	0	1	0	PWM6	READ/WRITE	Duty Cycle Control LED6
0	1	0	1	1	PWM7	READ/WRITE	Duty Cycle Control LED7
0	1	1	0	0	PWM8	READ/WRITE	Duty Cycle Control LED8
0	1	1	0	1	PWM9	READ/WRITE	Duty Cycle Control LED9
0	1	1	1	0	PWM10	READ/WRITE	Duty Cycle Control LED10
0	1	1	1	1	PWM11	READ/WRITE	Duty Cycle Control LED11
1	0	0	0	0	PWM12	READ/WRITE	Duty Cycle Control LED12
1	0	0	0	1	PWM13	READ/WRITE	Duty Cycle Control LED13
1	0	0	1	0	PWM14	READ/WRITE	Duty Cycle Control LED14
1	0	0	1	1	PWM15	READ/WRITE	Duty Cycle Control LED15
1	0	1	0	0	LS0	READ/WRITE	LED 0−3 Selector
1	0	1	0	1	LS1	READ/WRITE	LED 4−7 Selector
1	0	1	1	0	LS2	READ/WRITE	LED 8−11 Selector
1	0	1	1	1	LS3	READ/WRITE	LED 12−15 Selector

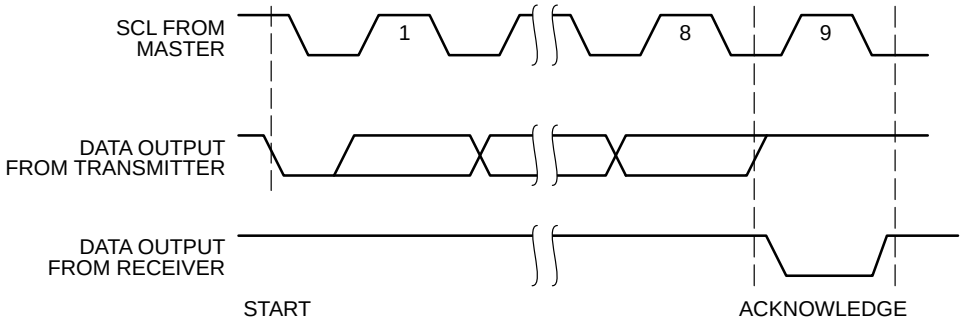


Figure 6. Acknowledge Timing

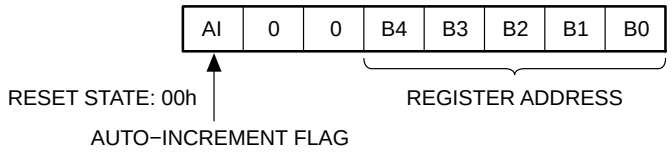


Figure 7. Control Register

The Input Register 0 and Input Register 1 reflect the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output. These registers are read only ports. Writes to the input registers will be acknowledged but will have no effect.

Table 8. INPUT REGISTER 0 AND INPUT REGISTER 1

INPUT0								
	LED 7	LED 6	LED 5	LED 4	LED 3	LED 2	LED 1	LED 0
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X
INPUT1								
	LED 15	LED 14	LED 13	LED 12	LED 11	LED 10	LED 9	LED 8
bit	7	6	5	4	3	2	1	0
default	X	X	X	X	X	X	X	X

The Frequency Prescaler A and Frequency Prescaler B registers (PSCA, PSCB) are used to program the period of the pulse width modulated signals BLINK0 and BLINK1 respectively:

T_BLINK0 = (PSCA + 1) / 152;
T_BLINK1 = (PSCB + 1) / 152

Table 9. FREQUENCY PRESCALER 0 AND FREQUENCY PRESCALER 1 REGISTERS

PSCA								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
PSCB								
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The PWM X Registers (PWMx) are used to program the duty cycle of each LED.

Duty Cycle_BLINK_X = PWMx / 256

The outputs that are configured to blink will be low (LED on) when an internal 8−bit counter's value is less than the value programmed into the PWM register. The LED will be off when the counter value is greater or equal to the value written in the PWM register.

Table 10. PWM REGISTER 0 AND PWM REGISTER 1

PWMx								
bit	7	6	5	4	3	2	1	0
default	1	0	0	0	0	0	0	0

Every LED driver output can be programmed to one of four states, LED OFF, LED ON, LED blinks at BLINK0 rate and LED blinks at BLINK1 rate using the LED Selector Registers (Table 11).

Table 11. LED SELECTOR REGISTERS

LS0								
	LED 3		LED 2		LED 1		LED 0	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS1								
	LED 7		LED 6		LED 5		LED 4	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS2								
	LED 11		LED 10		LED 9		LED 8	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0
LS3								
	LED 15		LED 14		LED 13		LED 12	
bit	7	6	5	4	3	2	1	0
default	0	0	0	0	0	0	0	0

The LED output (LED0 to LED15) is set by the 2 bits value from the corresponding LSx Register (x = 0 to 3):

00 = LED Output set Hi−Z (LED Off – Default)
01 = LED Output set LOW (LED On)
10 = LED Output blinks at BLINK0 Rate
11 = LED Output blinks at BLINK1 Rate. The duty cycle for a blinking LED is set by its individual PWM register.

Write Operations

Data is transmitted to the N64L1603 registers using the write sequence shown in Figure 8.

If the AI bit from the command byte is set to “1”, the N64L1603 internal registers can be written sequentially. After sending data to one register, the next data byte will be sent to the next register sequentially addressed. After the last register is accessed, the next register to be accessed will be the “00000” register.

Read Operations

The N64L1603 registers are read according to the timing diagrams shown in Figure 9 and Figure 11. Data from the register, defined by the command byte, will be sent serially on the SDA line.

After the first byte is read, additional data bytes may be read when the auto−increment flag, AI, is set. The additional data byte will reflect the data read from the next register sequentially addressed by the (B4 B3 B2 B1 B0) bits of the command byte. After the last register is accessed, the next register to be accessed will be the “00000” register.

When reading Input Port Registers (Figure 11), data is clocked into the register on the failing edge of the acknowledge clock pulse. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

LED Pins Used as General Purpose I/O

Any LED pins not used to drive LEDs can be used as general purpose input/output, GPIO.

When used as input, the user should program the corresponding LED pin to Hi−Z (“00” for the LSx register bits). The pin state can be read via the Input Register according to the sequence shown in Figure 11.

For use as output, an external pull−up resistor should be connected to the pin. The value of the pull−up resistor is calculated according to the DC operating characteristics. To set the LED output high, the user has to program the output Hi−Z writing “00” into the corresponding LED Selector (LSx) register bits. The output pin is set low when the LED output is programmed low through the LSx register bits (“01” in LSx register bits).

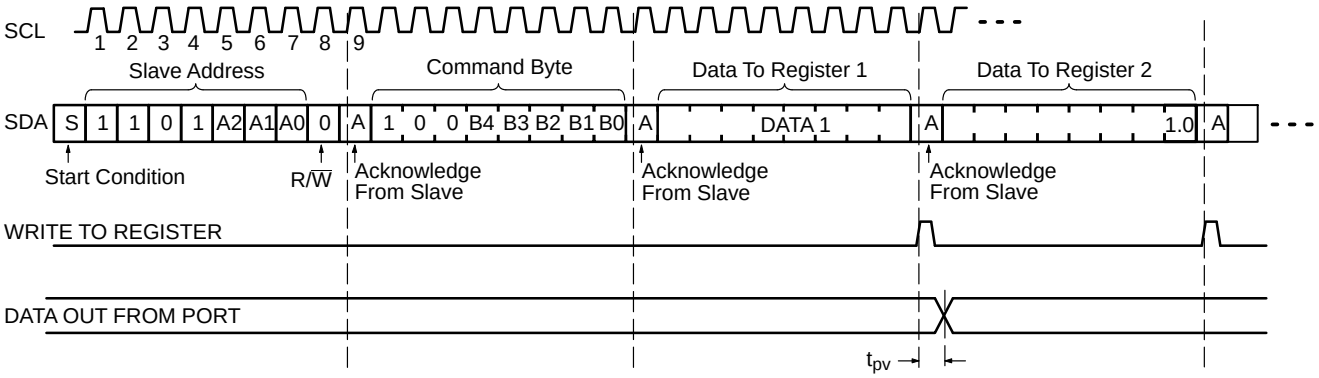


Figure 8. Write to Register Timing Diagram

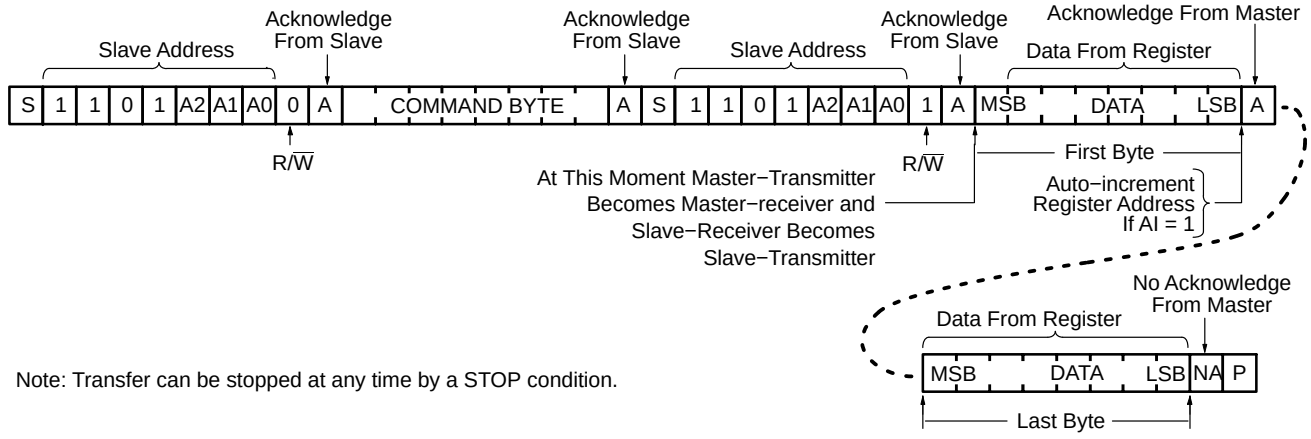


Figure 9. Read from Register Timing Diagram

External Reset Operation

The N64L1603 registers and the I^2C state machine are initialized to their default state when the RESET input is held low for a minimum of t_W. The external Reset timing is shown in Figure 12.

LED Output Operation

Figure 10 shows typical current values for LED pin voltages at various case temperatures.

Power−On Reset Operation

The N64L1603 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device is in a reset state for V_{CC} less than the internal POR threshold level (V_{POR}). When V_{CC} exceeds the V_{POR} level, the reset state is released and the N64L1603 internal state machine and registers are initialized to their default state.

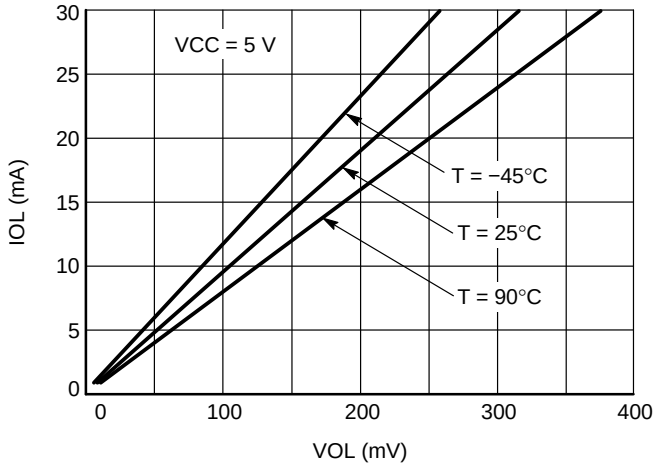


Figure 10. IOL vs VOL for LED Pin

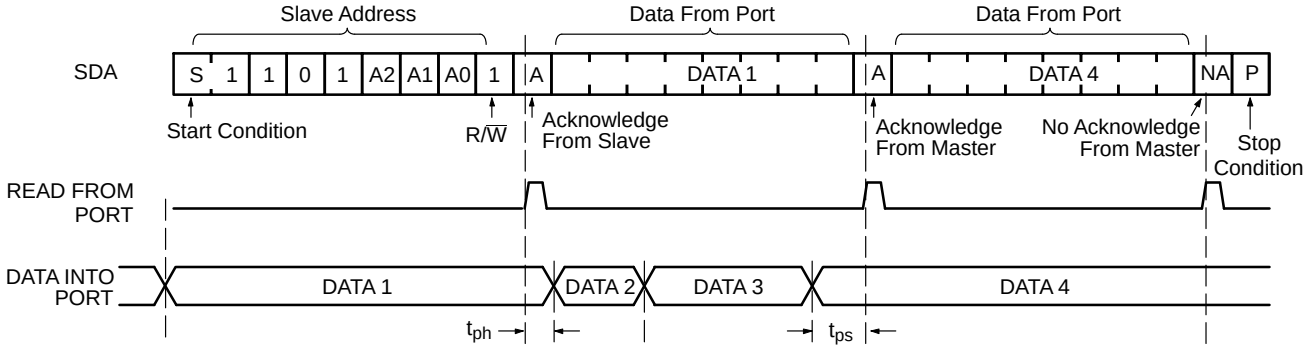


Figure 11. Read Input Port Register Timing Diagram

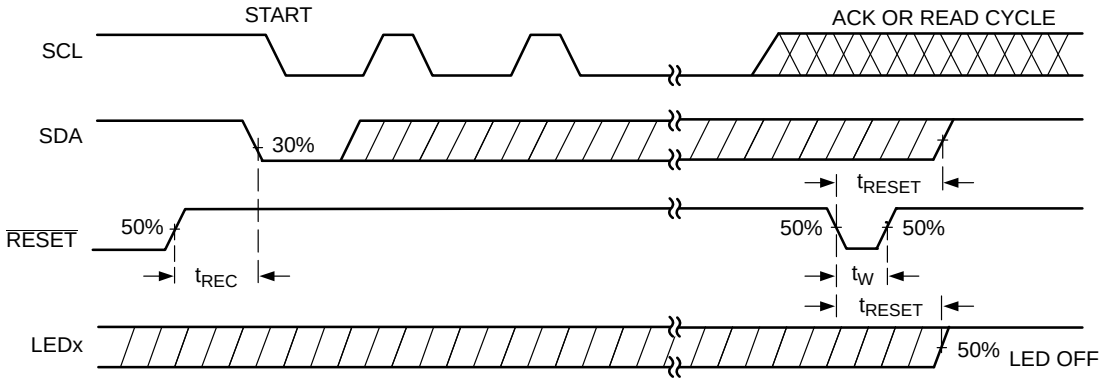
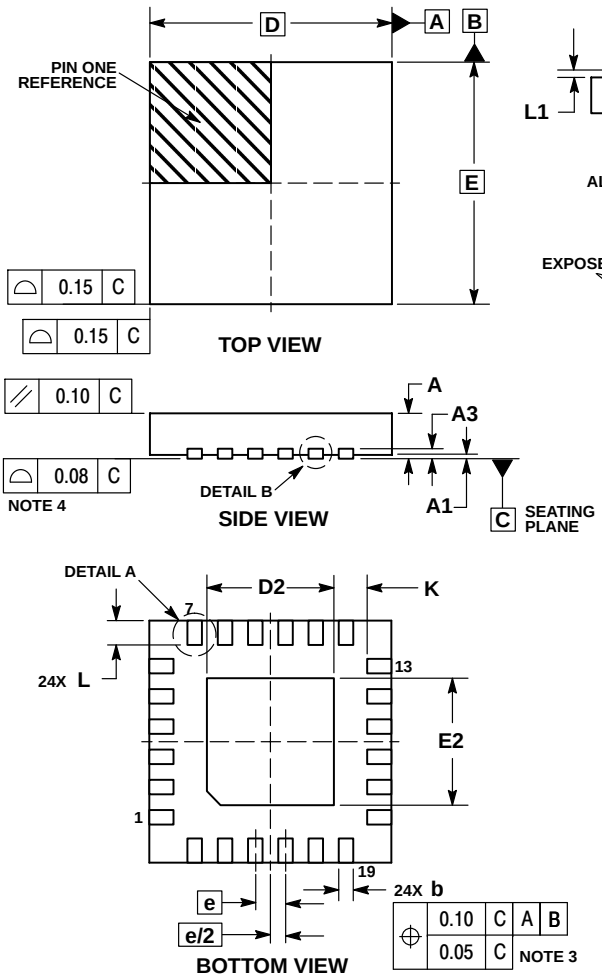
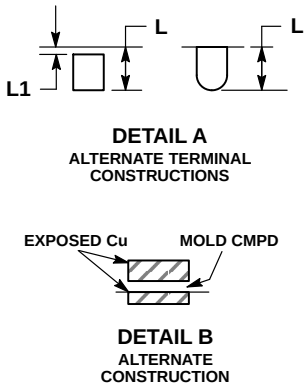


Figure 12. $\overline{\text{RESET}}$ Timing Diagram

PACKAGE DIMENSIONS

WQFN24 4x4, 0.5P
CASE 485BG
ISSUE A

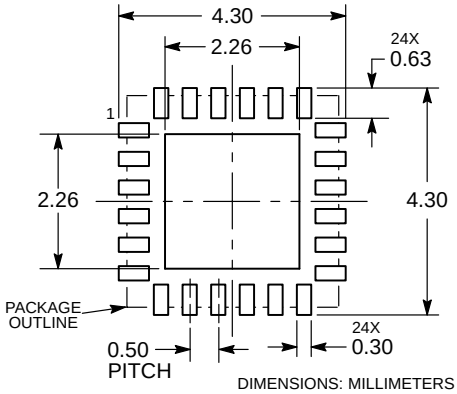




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.00	2.20
E	4.00 BSC	
E2	2.00	2.20
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.15

MOUNTING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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