# **3.3 V OmniClock Generator with Single Ended (LVCMOS) Output**

The NB3H60113GH1, which is a member of the OmniClock family, is a low power PLL-based clock generator. The device accepts a 1.28 MHz / 1.54 MHz single ended (LVCMOS) reference clock as input. It generates one single ended (LVCMOS) output of 4x / 5x of Input Clock. CLKSEL (LVCMOS) control signal selects 4x / 5x Clock at the output. The device can be powered down using the Power Down pin (PDB).

# Features

- Member of the OmniClock Family of Programmable Clock Generators
- Operating Power Supply:  $3.3 \text{ V} \pm 0.3 \text{ V}$
- I/O Standards
  - Input: 1.28 MHz / 1.54 MHz Reference Clock (LVCMOS)
  - Output: 4x / 5x of Input Clock (LVCMOS)
- Output Drive Current for Single Ended Output: 16 mA
- Power Saving Mode through Power Down Pin
- Temperature Range –40°C to 85°C
- Packaged in 8–Pin WDFN
- These are Pb–Free Devices

### **Typical Application**

• Industrial



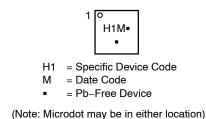
# **ON Semiconductor®**

www.onsemi.com



WDFN8 CASE 511AT

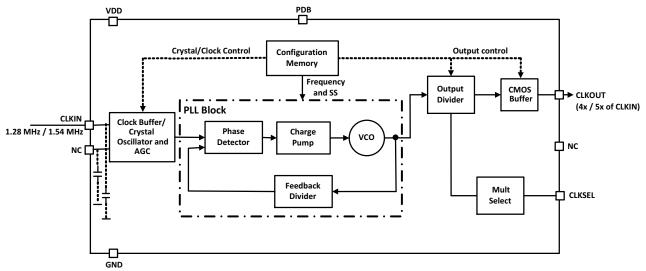
# MARKING DIAGRAM



### **ORDERING INFORMATION**

See detailed ordering and shipping information on page 6 of this data sheet.

# **BLOCK DIAGRAM**





# **PIN FUNCTION DESCRIPTION**

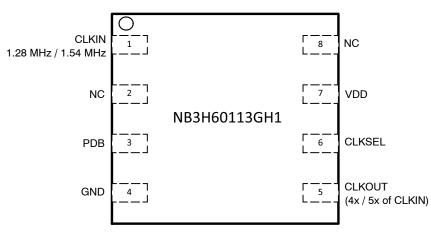


Figure 2. Pin Connections (Top View) – WDFN8

#### **Table 1. PIN DESCRIPTION**

Pin No.	Pin Name	Pin Type	Description
1	CLKIN	Input	1.28 MHz / 1.54 MHz single-ended external reference input clock (LVCMOS)
2	NC	-	No Connection. Not to be connected to any circuit
3	PDB	Input	Asynchronous LVCMOS input. Active Low Master Reset to disable the device and set outputs Low. Internal pull-down resistor. This pin needs to be pulled High for normal Operation of the chip.
4	GND	Ground	Power supply ground
5	CLKOUT	Output	4x / 5x of Input Clock Single-ended (LVCMOS) output
6	CLKSEL	Input	Output Clock multiplier Selection input (LVCMOS). Selects 4x / 5x of CLKIN
7	VDD	Power	3.3 V Power Supply
8	NC	-	No Connection. Not to be connected to any circuit

#### Table 2. POWER DOWN FUNCTION TABLE

PDB	Function			
0	Device Powered Down			
1	Device Powered Up			

NOTE: PDB has internal pull down resistor.

#### **Table 4. ATTRIBUTES**

Characteristic	Value
ESD Protection Human Body Model	2 kV
Internal Input Default State Pull up/ down Resistor	50 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)	MSL1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	130 k
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

# Table 5. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter		Rating	Unit
VDD	Positive power supply with respect to Ground	-0.5 to +4.6	V	
VI	Input Voltage with respect to chip ground	-0.5 to VDD + 0.5	V	
T <sub>A</sub>	Operating Ambient Temperature Range (Industrial Grade)	-40 to +85	°C	
T <sub>STG</sub>	Storage temperature		–65 to +150	°C
T <sub>SOL</sub>	Max. Soldering Temperature (10 sec)		265	°C
$\theta_{JA}$		0 lfpm 0 lfpm	129 84	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-case)		35 to 40	°C/W
TJ	Junction temperature		125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

 Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power). ESD51.7 type board. Back side Copper heat spreader area 100 sq mm, 2 oz (0.070 mm) copper thickness.

# Table 3. OUTPUT CLOCK SELECTION

CLKSEL	CLKOUT
0	4x CLKIN
1	5x CLKIN

### Table 6. RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Min	Тур	Max	Unit
V <sub>DD</sub>	Core Power Supply Voltage	3.3 V operation	3.0	3.3	3.6	V
CL	Clock output load capacitance for LVCMOS clock				15	pF
fclkin	Reference Clock Frequency	Single ended Clock input (LVCMOS)	1.2	1.28 / 1.54	1.6	MHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# Table 7. DC ELECTRICAL CHARACTERISTICS (V\_{DD} = 3.3 V $\pm$ 0.3 V; GND = 0 V, T\_A = -40°C to +85°C)

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I <sub>DD_3.3 V</sub>	Power Supply current	fout = 4x / 5x of CLKIN		10		mA
I <sub>PD</sub>	Power Down Supply Current	PDB is Low to make all outputs OFF			80	μA
VIH	Input HIGH Voltage	Pin CLKIN, CLKSEL	0.65 V <sub>DD</sub>		V <sub>DD</sub>	V
		Pin PDB	0.85 V <sub>DD</sub>		V <sub>DD</sub>	
V <sub>IL</sub>	Input LOW Voltage	Pin CLKIN, CLKSEL	0		0.35 V <sub>DD</sub>	V
		Pin PDB	0		0.15 V <sub>DD</sub>	
Cin	Input Capacitance	Pin PDB		4	6	pF

V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = 3.3 V	I <sub>OH</sub> = 16 mA	0.75*V <sub>DD</sub>		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = 3.3 V	I <sub>OL</sub> = 16 mA		0.25*V <sub>DD</sub>	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# Table 8. AC ELECTRICAL CHARACTERISTICS (V\_{DD} = 3.3 V $\pm$ 0.3 V, GND = 0 V, T\_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
fout	Single Ended Output Frequency			4x / 5x of CLKIN		MHz
t <sub>PU</sub>	Stabilization time from Power-up	V <sub>DD</sub> = 3.3 V		3.0		ms
t <sub>PD</sub>	Stabilization time from Power Down	Time from falling edge on PDB pin to tri-stated outputs (Asynchronous)		3.0		ms
Eppm	Synthesis Error			0		ppm

# SINGLE ENDED OUTPUT (V\_DD = 3.3 V $\pm$ 0.3 V, GND = 0 V, T\_A = -40°C to 85°C)

t <sub>r</sub> / t <sub>f</sub>	Rise/Fall Time	Measured between 20% to 80% with 15 pF load, $f_{out}$ = 4x / 5x of CLKIN, $V_{DD}$ = 3.3 V		1		ns
t <sub>DC</sub>	Output Clock Duty Cycle	V <sub>DD</sub> = 3.3 V; Duty Cycle of Ref clock is 50% PLL Clock	45	50	55	%

# PARAMETER MEASUREMENT TEST CIRCUIT

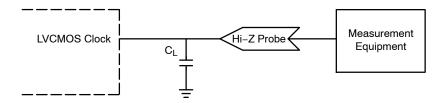
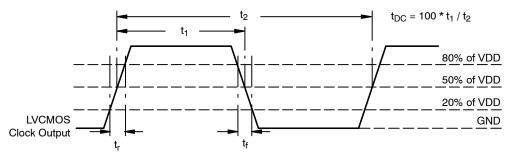


Figure 3. LVCMOS Clock Parameter Measurement

# TIMING MEASUREMENT DEFINITIONS





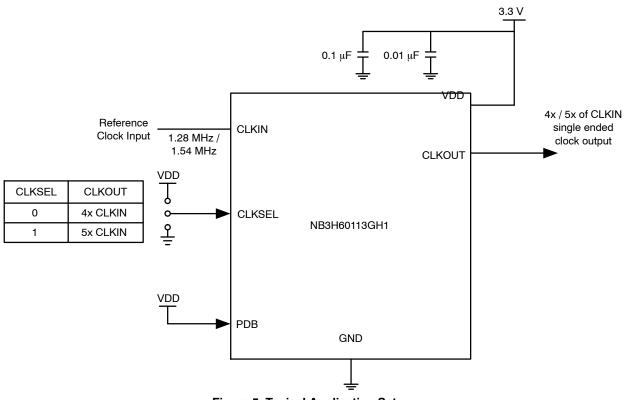


Figure 5. Typical Application Setup

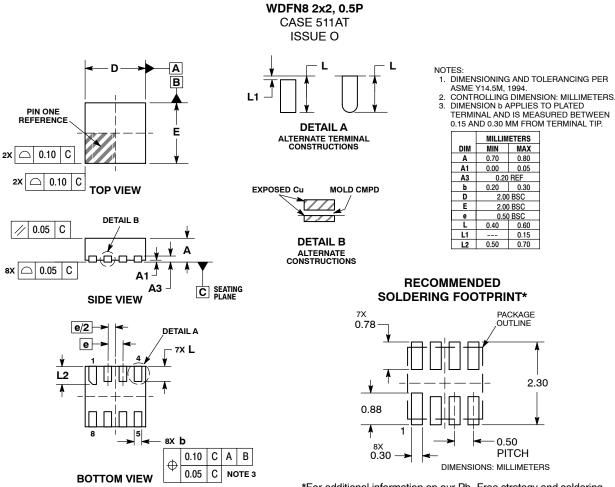
#### **ORDERING INFORMATION**

Device	Case	Package	Shipping <sup>†</sup>
NB3H60113GH1MTR2G	511AT	DFN-8 (Pb-Free)	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Please contact your ON Semiconductor sales representative for information on un-programmed versions of this device.

#### PACKAGE DIMENSIONS



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns me rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdt/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor dates sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights or the rights of others. ON Semiconductor and the support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expe

Phone: 421 33 790 2910

#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support: ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative