NB7VPQ7011M

Product Preview

1.8 V USB 3.1 Single Channel Linear Redriver

ON Semiconductor®

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Description

The NB7VPQ7011M is a 1.8 V single channel linear redriver for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7VPQ7011M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter.

After power up, the NB7VPQ7011M periodically checks both of the TX output pairs for a receiver connection. When the receiver is detected on both channels the RX termination becomes enabled and the NB7VPQ7011M is set to perform the redriver function.

The NB7VPQ7011M comes in a small, ultra−thin 1.6 x 1.6 mm UQFN12 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

Features

- 1.8 V ± 0.1 V Power Supply
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic Receiver Termination Detection
- Integrated Input and Output Termination
- Selectable Equalization and Flat Gain
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range: –40°C to 85°C
- Small 1.6 x 1.6 x 0.4 mm Pitch UQFN12 Package
- This is a Pb−Free Device

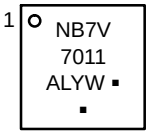
Typical Applications

- USB3.1 Type−C Signal Routing
- Mobile Phone and Tablet
- Computer and Laptop
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

UQFN12
CASE 523AV

MARKING DIAGRAM



NB7V7011 = = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NB7VPQ7011MMUTXG	UQFN12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

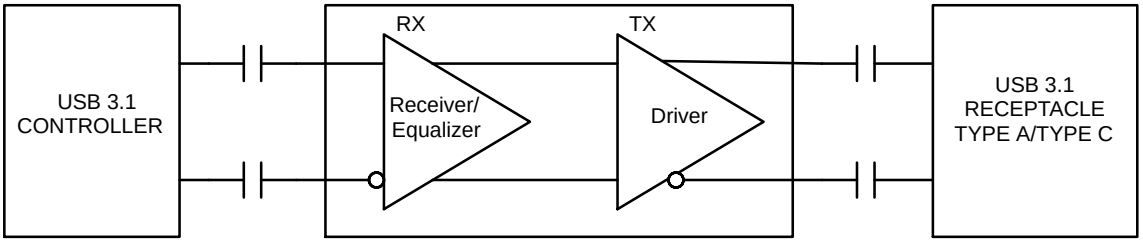


Figure 1. Typical Application

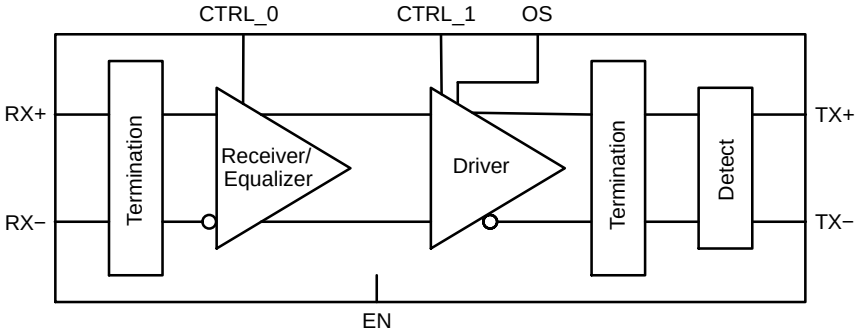


Figure 2. Logic Diagram of NB7VPQ7011M

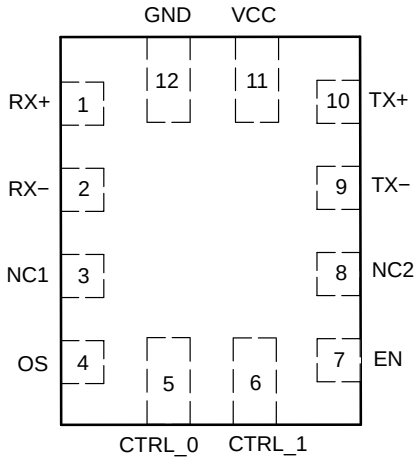


Figure 3. UQFN12 Package Pinout
(Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	RX+	DIFF IN	Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
2	RX−		
3	OS	LVCMOS IN	Linear Output Swing Pin, 4−state input with integrated 100 kΩ pull−up and 200 kΩ pull−down resistors. Default is ‘Float’ when left open
5, 6	CTRL_0, CTRL_1	LVCMOS IN	Control Pins for equalization and flat gain on the RX. 4−state input with integrated 100 kΩ pull−up and 200 kΩ pull−down resistors. Defaults to ‘Float’ when left open. Refer Table 2 for options.
7	EN	LVCMOS IN	Chip enable input (active high), internal 200 kΩ pull−up resistor. Low to power down.
9	TX−	DIFF OUT	Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
10	TX+		
11	VCC	Power	1.8 V power supply. VCC pins must be externally connected to power supply to guarantee proper operation.
12	GND	GND	Reference Ground. GND pins must be externally connected to power supply to guarantee proper operation.
3, 8	NC1, NC2		No Connection – float Pin

DEVICE CONFIGURATION

Table 2. CONTROL PINS FOR EQ/FG SETTINGS:

Settings	CTRL_0	CTRL_1		EQ	FG
1	L	L		3 dB	−1.5 dB
2		R		6 dB	−1.5 dB
3		F		9 dB	−1.5 dB
4		H		12 dB	−1.5 dB
5	R	L		15 dB	−1.5 dB
6		R		6 dB	0 dB
7		F		9 dB	0 dB
8		H		12 dB	0 dB
9	F	L		15 dB	0 dB
10		R		18 dB	0 dB
11		F		3 dB	0 dB
12		H		3 dB	+1.5 dB
13	H	L		6 dB	+1.5 dB
14		R		9 dB	+1.5 dB
15		F		12 dB	+1.5 dB
16		H		15 dB	+1.5 dB

L = Low, R = Ext Resistor, F = Float, H = High, Default Control Pins float

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	> 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{CC}	−0.5	2.5	V
Voltage range at any input or output terminal	Differential I/O	−0.5	1.89	V
	LVCMOS inputs	−0.3	V_{CC} + 0.3	V
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Operating Ambient Temperature Range, T_A		−40	85	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 3)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 5. RECOMMENDED OPERATING CONDITIONS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Nom	Max	Unit
V_{CC}	Main power supply	1.70	1.80	1.90	V
T_A	Operating free−air temperature	−40		+85	°C
C_{AC}	External AC Coupling Capacitor	75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. POWER SUPPLY CHARACTERISTICS (Note 4)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{CC}	Active	Link in U0 with Super Speed Plus data transmission		75		mA
	U2/U3	Link in U2 or U3 power saving state		2.5		mA
	No USB Connection	No connection state, termination disabled		500		μA

4. TYP values use V_{CC} = 1.8 V, T_A = 25°C.

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS 4−State LVCMOS Inputs (CTRL_0, CTRL_1, OS)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IL}	DC Input Setting “L”	Input pin connected to GND		GND		V
V_{IR}	DC Input Setting “R”	A specified resistor must be applied between pin and GND		0.33*V_{CC}		V
V_{IF}	DC Input Setting “F”	Input pin is left floating (Note 5)		0.66*V_{CC}		V
V_{IH}	DC Input Setting “H”	Input pin connected to V_{CC}		V_{CC}		V
R_{PU}	Internal pull−up resistance			100		KΩ
R_{PD}	Internal pull−down resistance			200		KΩ
I_{IH}	High−level input current	V_{IN} = 1.9 V			+20	μA
I_{IL}	Low−level input current	V_{IN} = GND, V_{CC} = 1.9 V	−20			μA
R_{ext}	External Resistor for input setting “R”			68		KΩ

5. Floating refers to a pin left in an open state, with no external connections

Table 8. LVCMOS CONTROL PIN CHARACTERISTICS 2−State LVCMOS Inputs (EN)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IL}	DC Input Setting “L”	Input pin connected to GND		GND		V
V_{IH}	DC Input Setting “H”	Input pin connected to V_{CC}		V_{CC}		V
R_{PU}	Internal pull−up resistance			200		KΩ
I_{IH}	High−level input current	V_{IN} = 1.9 V			+20	μA
I_{IL}	Low−level input current	V_{IN} = GND, V_{CC} = 1.9 V	−20			μA

6. Floating refers to a pin left in an open state, with no external connections

Table 9. RECEIVER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{RX-DIFF-pp}$	Input differential voltage swing	AC−coupled, peak−to−peak	100		1200	mV_{PP}
V_{RX-CM}	Common−mode voltage bias in the receiver (DC)			V_{CC}		V
$Z_{RX-DIFF}$	Differential input impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{RX-CM}	Common−mode input impedance (DC)	Present after an USB device is detected on TX+/TX−	20	25	30	Ω
$Z_{RX-HIGH-IMP}$	Common−mode input impedance with termination disabled (DC)	Present when no USB device is detected on TX+	25	190		kΩ
$V_{TH-LFPS-pp}$	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Output voltage is considered squelched below this threshold voltage	100	200	300	mV_{PP}
V_{TH-AM}	Active Mode detector threshold	Signal threshold in Active and Slumber mode	50		150	mV_{PPd}

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 10. TRANSMITTER AC/DC CHARACTERISTICS Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{SW_100M}	−1 dB compression point output swing at 100 MHz	OS = GND OS = R OS = Float OS = V_{CC}		900 1000 1100 1200		mV_{PPd}
V_{SW_5G}	−1 dB compression point output swing at 5 GHz	OS = GND OS = R OS = Float OS = V_{CC}		600 700 800 900		mV_{PPd}
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX-DIFF}$	Differential output impedance (DC)	Present after an USB device is detected on TX+/TX−	80	100	120	Ω
Z_{TX-CM}	Common−mode output impedance (DC)	Present after an USB device is detected on TX+/TX−	20		30	Ω
I_{TX-SC}	TX short circuit current	TX+ or TX− shorted to GND		60		mA
V_{TX-CM}	Common−mode voltage bias in the transmitter (DC)			Vcc – 0.675	Vcc	V
$V_{TX-CM-ACpp}$	AC common−mode peak−to−peak voltage swing in active mode	Within U0 and within LFPS			100	mV_{PP}
$V_{TX-IDLE-DIFF-ACpp}$	Differential voltage swing during electrical idle	Tested with a high−pass filter	0		10	mV_{PP}
$V_{TX-RXDET}$	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise, fall time	20% − 80% of differential voltage measured 1 inch from the output pin		40		ps
t_{RF-MM}	Output rise, Fall time mismatch	20% − 80% of differential voltage measured 1 inch from the output pin			5	ps
$t_{diff-LH}$, $t_{diff-HL}$	Differential propagation delay	Propagation delay between 50% level at input and output		150		ps
$t_{idleEntry}$, $t_{idleExit}$	Idle entry and exit times			10		ns

Table 11. TIMING AND JITTER CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
TIMING						
t_{READY}	Time from power applied until RX termination is enabled	Apply 0 V to V_{CC}, connect USB termination to TX±, apply 1.8 V to V_{CC}, and measure when $Z_{RX-DIFF}$ is enabled		110		ms
JITTER FOR 5 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 7, 8)	CTRL Pins are float		0.5		UI (Note 9)
D_{JTX}	Deterministic jitter (Note 8)			0.25		UI
R_{JTX}	Random jitter (Note 8)			0.1		UI
JITTER FOR 10 Gbps						
$T_{JTX-EYE}$	Total jitter (Notes 7, 8)	CTRL Pins are float		0.5		UI (Note 9)
D_{JTX}	Deterministic jitter (Note 8)			0.25		UI
R_{JTX}	Random jitter (Note 8)			0.1		UI

7. Includes RJ at 10^{-12}.
8. Measured at the ends of reference channel with a K28.5 pattern, VID = 1000 mVpp.
9. 5 Gbps, UI = 200 ps for 10 Gbps, UI = 100 ps

PARAMETER MEASUREMENT DIAGRAMS

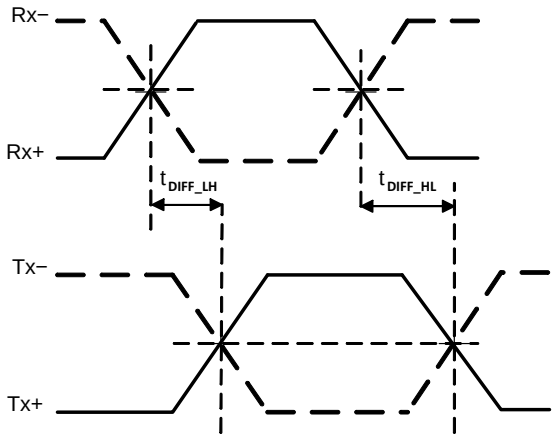


Figure 4. Propagation Delay

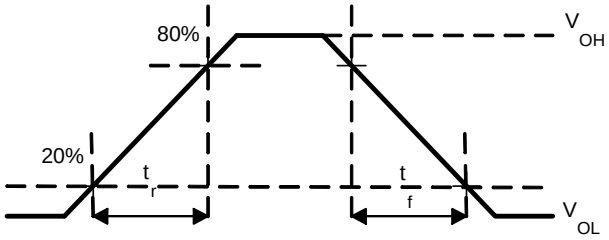
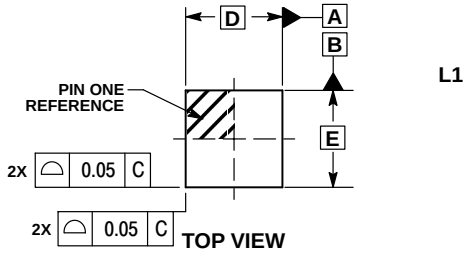


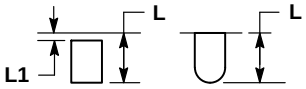
Figure 5. Output Rise and Fall Times

NB7VPQ7011M

PACKAGE DIMENSIONS

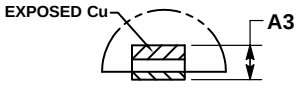
UQFN12, 1.6x1.6, 0.4P
CASE 523AV
ISSUE A

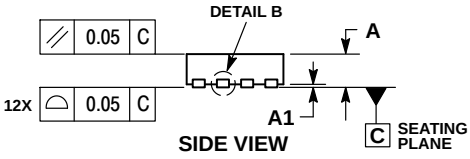


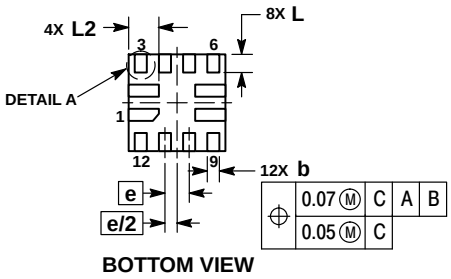


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.

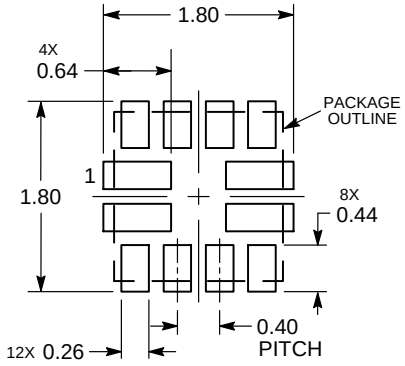
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.152 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.40 BSC	
L	0.20	0.40
L2	0.40	0.60







SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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