NC7SZ74

TinyLogic UHS D-Type, Flip-Flop with Preset and Clear

ON Semiconductor®

www.onsemi.com

US8	UQFN8 1.6x1.6, 0.5P
CASE 846AN	CASE 523AY

Description

The NC7SZ74 is a single, D−type, CMOS flip−flop with preset and clear from ON Semiconductor ultra high−speed series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive, while maintaining low static power dissipation over a very broad V_{CC} operating range of 1.65 V to 5.5 V V_{CC}. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V, independent of V_{CC} operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive−going transition of the CLK pulse.

Features

- Ultra−High Speed: t_{PD} 2.6 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High−Impedance Inputs/Outputs
- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry

CONNECTION DIAGRAMS

IEEE/IEC

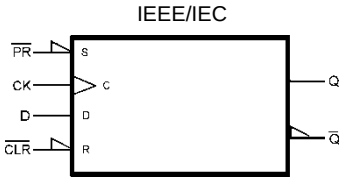


Figure 1. Logic Symbol

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Pin Configurations

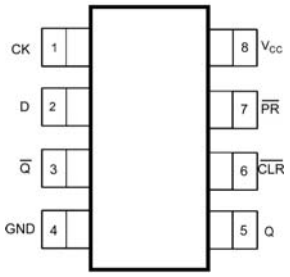


Figure 2. USB (Top View)

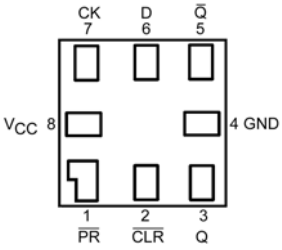


Figure 3. MicorPak™ (Top Through View)

PIN DEFINITIONS

Pin # US8	Pin # MicroPak	Name	Description
1	7	CK	Clock Pulse Input
2	6	D	Data Input
3	5	$\overline{Q}$	Flip−Flop Output
4	4	GND	Ground
5	3	Q	Flip−Flop Output
6	2	$\overline{CLR}$	Direct Clear Input
7	1	$\overline{PR}$	Direct Preset Input
8	8	VCC	Supply Voltage

ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method†
NC7SZ74K8X	SZ74	8−Lead US8, JEDEC MO−187, Variation CA 3.1mm Wide	3000 Units on Tape & Reel
NC7SZ74L8X	N9	8−Lead MicroPak, 1.6 mm Wide	5000 Units on Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

FUNCTION TABLE

Inputs				Output		Function
/CLR	/PR	D	CK	Q	/Q	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	$/Q_n$	No Change

H = HIGH Logic Level Qn = No change in data X = Immaterial ↓= Falling Edge

L = LOW Logic Level Z = High Impedance ↑ = Rising Edge

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0V		−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0V		−50	mA
I_{OUT}	DC Output Source/Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85□C			250	mW
ESD	Human Body Model, JEDEC:JESD22−A114			5000	V
	Charge Device Model: JEDEC:JESD22−C101			2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.50	5.50	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage	Active State	0	V_{CC}	V
		3−State	0	5.5	

RECOMMENDED OPERATING CONDITIONS (continued)

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_r, t_f	Input Rise and Fall Times	V_{CC} = 1.8 V, 2.5 V ± 0.2 V	0	20	ns/V
		V_{CC} = 3.3 V ± 0.3 V	0	10	
		V_{CC} = 5.0 V ± 0.5 V	0	5	
T_A	Operating Temperature		−40	+85	°C
θ_{JA}	Thermal Resistance	US8		250	°C/W
		MicroPak™ −8		280	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Vcc	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Control Input Voltage	1.65 to 1.95		0.65 V_{CC}			0.65 V_{CC}		V
		2.30 to 5.50		0.70 V_{CC}			0.70 V_{CC}		
V_{IL}	LOW Level Control Input Voltage	1.65 to 1.95				0.35 V_{CC}		0.35 V_{CC}	V
		2.30 to 5.50				0.30 V_{CC}		0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	V_{IN} = V_{IH}, I_{OH} = −100 μA	1.55	1.65		1.55		V
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.40		
		1.65	I_{OH} = −4 mA	1.29	1.52		1.29		
		2.30	I_{OH} = −8 mA	1.90	2.15		1.90		
		3.00	I_{OH} = −16 mA	2.40	2.80		2.40		
		3.00	I_{OH} = −24 mA	2.30	2.68		2.30		
		4.50	I_{OH} = −32 mA	3.80	4.20		3.80		
V_{OL}	LOW Level Control Output Voltage	1.65	V_{IN} = V_{IH}, I_{OL} = 100 μA			0.10		0.10	V
		2.30				0.10		0.10	
		3.00				0.10		0.10	
		4.50				0.10		0.10	
		1.65	I_{OL} = 4 mA		0.10	0.24		0.24	
		2.30	I_{OL} = 8 mA		0.10	0.30		0.30	
		3.00	I_{OL} = 16 mA		0.15	0.40		0.40	
		3.00	I_{OL} = 24 mA		0.22	0.55		0.55	
		4.50	I_{OL} = 32 mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5	0 ≤ V_{IN} ≤ 5.5 V			±0.1		±1.0	μA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT} = 5.5 V			1		10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN} = 5.5 V, GND			1		10	μA

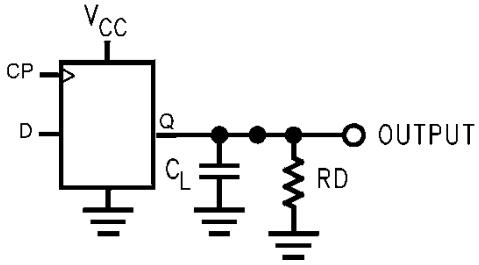
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
f_{MAX}	Maximum Clock Frequency	1.80 ± 0.15	C_L = 15 pF R_D = 1 MΩ S_1 = Open	75			75		ns	Figure 4 Figure 8
		2.50 ± 0.20		150			150			
		3.30 ± 0.30		200			200			
		5.00 ± 0.50		250			250			
		3.30 ± 0.50	C_L = 50 pF R_D = 500 Ω, S_1 = Open	175			175			
		5.00 ± 0.50		200			200			
t_{PLH}, t_{PHL}	Propagation Delay CK to Q, /Q	1.80 ± 0.15	C_L = 15pF, R_D = 1 MΩ S_1 = Open		6.5	12.5		13.0	ns	Figure 4 Figure 6
		2.50 ± 0.20			3.8	7.5		8.0		
		3.30 ± 0.30			2.8	6.5		7.0		
		5.00 ± 0.50			2.2	4.5		5.0		
		3.30 ± 0.30	C_L = 50 pF R_D = 500 Ω, S_1 = Open		3.4	7.0		7.5		
		5.00 ± 0.50			2.6	5.0		5.5		
t_{PLH}, t_{PHL}	Propagation Delay /CLR, /PR to Q, /Q	1.80 ± 0.15	C_L = 15 pF, R_L = 1 MΩ S_1 = Open		6.5	14.0		14.5	ns	Figure 4 Figure 6
		2.50 ± 0.20			3.8	9.0		9.5		
		3.30 ± 0.30			2.8	6.5		7.0		
		5.00 ± 0.50			2.2	5.0		5.5		
		3.30 ± 0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open		3.4	7.0		7.5		
		5.00 ± 0.50			2.6	5.0		5.5		
t_S	Setup Time CK to D	1.80 ± 0.15	C_L = 15 pF, R_L = 1 MΩ S_1 = Open	6.5			6.5		ns	Figure 4 Figure 7
		2.50 ± 0.20		3.5			3.5			
		3.30 ± 0.30		2.0			2.0			
		5.00 ± 0.50		1.5			1.5			
		3.30 ± 0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	2.0			2.0			
		5.00 ± 0.50		1.5			1.5			
t_H	Hold Time, CK to D	1.80 ± 0.15	C_L = 15 pF, R_L = 1 MΩ S_1 = Open	0.5			0.5		ns	Figure 4 Figure 7
		2.50 ± 0.20		0.5			0.5			
		3.30 ± 0.30		0.5			0.5			
		5.00 ± 0.50		0.5			0.5			
		3.30 ± 0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	0.5			0.5			
		5.00 ± 0.50		0.5			0.5			
t_W	Pulse Width, CK, /PR, /CLR	1.80 ± 0.15	C_L = 15 pF, R_L = 1 MΩ S_1 = Open	6.0			6.0		ns	Figure 4 Figure 8
		2.50 ± 0.20		4.0			4.0			
		3.30 ± 0.30		3.0			3.0			
		5.00 ± 0.50		2.0			2.0			
		3.30 ± 0.30	C_L=50pF, R_D=500Ω, S_1=Open	3.0			3.0			
		5.00 ± 0.50		2.0			2.0			

AC ELECTRICAL CHARACTERISTICS (continued)

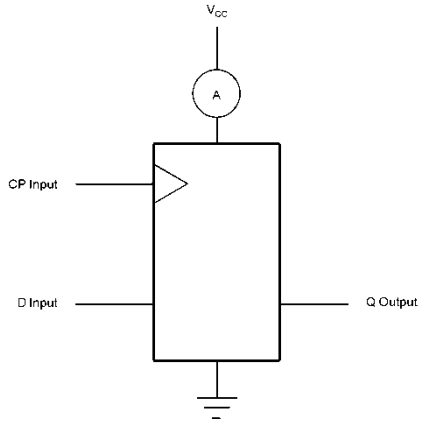
Symbol	Parameter	V_{CC}	Conditions	T_A = +25°C			T_A = −40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{REC}	Recover Time /CLR, /PR to CK	1.80 ± 0.15	C_L = 15 pF, R_L = 1 MΩ S_1 = Open	8.0			8.0		ns	Figure 7
		2.50 ± 0.20		4.5			4.5			
		3.30 ± 0.30		3.0			3.0			
		5.00 ± 0.50		3.0			3.0			
		3.30 ± 0.30	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	3.0			3.0			
		5.00 ± 0.50		3.0			3.0			
C_{IN}	Input Capacitance	0			3				pF	
C_{OUT}	Output Capacitance	0			4				pF	
C_{PD}	Power Dissipation Capacitance (Note 1)	3.30			10				pF	
		5.00			12					

1. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.



2. C_L includes load and stray capacitance. Input PRR = 1.0 MHz t_W = 500 ns.

Figure 4. AC Test Circuit



3. CP input = AC Waveforms t_r = t_f = 2.5 ns.
4. CP input PRR = 10 MHz; Duty Cycle = 50%.
5. D input PRR = 5 MHz; Duty Cycle = 50%.

Figure 5. AC Test Circuit

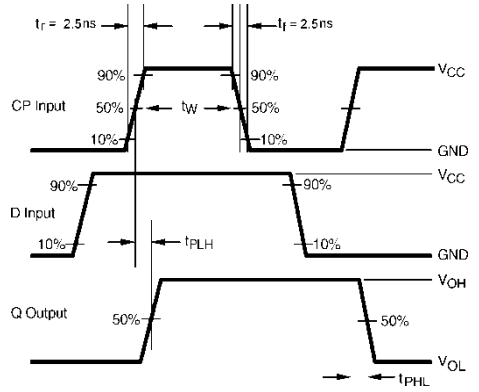


Figure 6. AC Waveforms

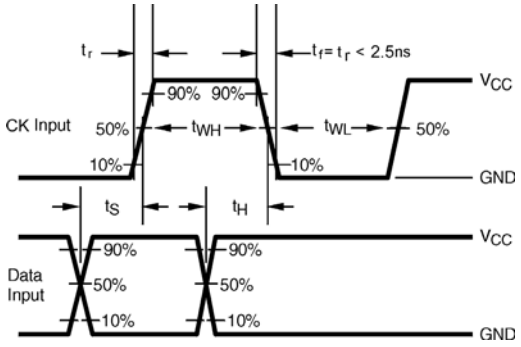


Figure 7. AC Waveforms

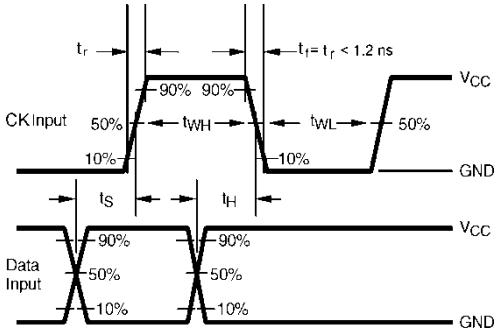
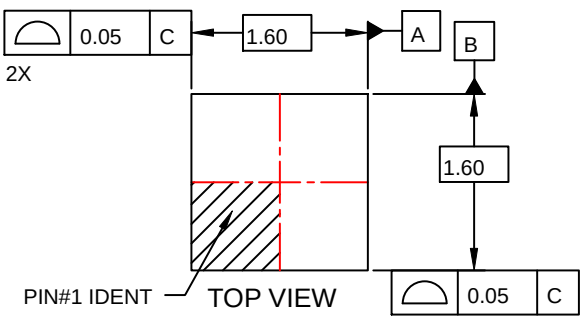
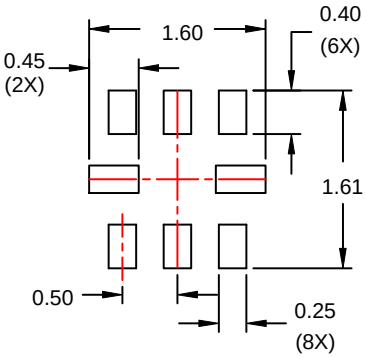


Figure 8. AC Waveforms

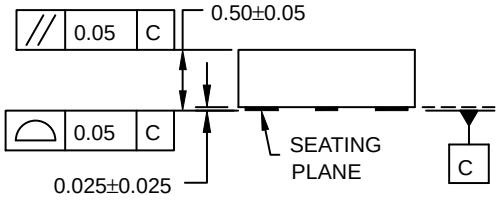
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016





RECOMMENDED
LAND PATTERN



SIDE VIEW

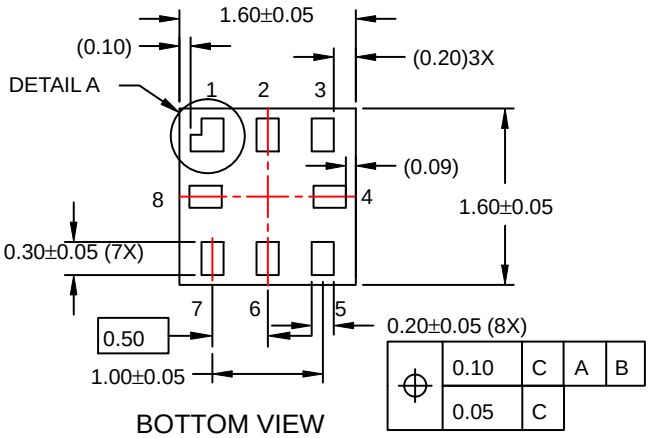
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

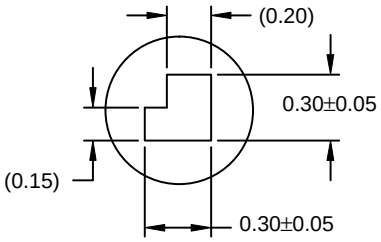
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



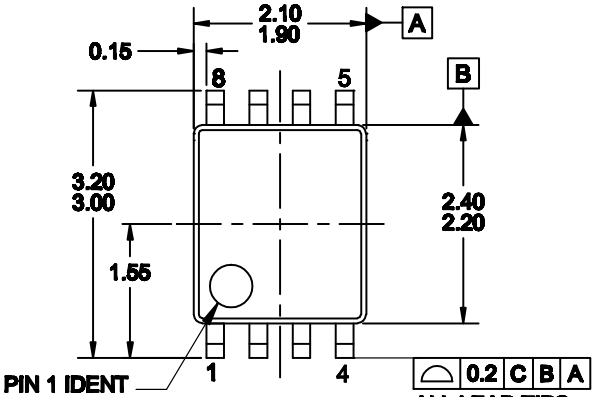
DETAIL A
SCALE : 2X

DOCUMENT NUMBER:	**98AON13591G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**UQFN8 1.6X1.6, 0.5P**		**PAGE 1 OF 2**

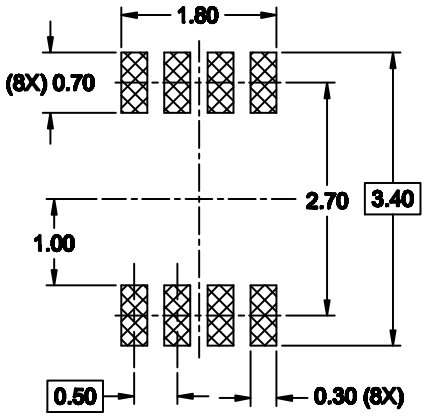
ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD MAC08A TO ON SEMICONDUCTOR. REQ. BY B. MARQUIS.	31 AUG 2016

US8
CASE 846AN
ISSUE O

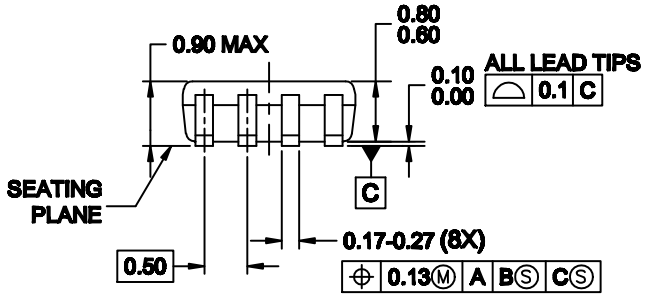
DATE 31 DEC 2016



TOP VIEW



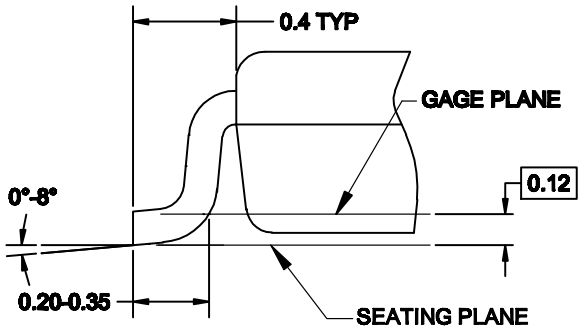
RECOMMENDED LAND PATTERN



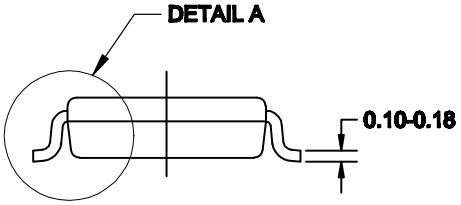
SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



DETAIL A



DOCUMENT NUMBER:	**98AON13778G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
STATUS:	**ON SEMICONDUCTOR STANDARD**		
NEW STANDARD:			
DESCRIPTION:	**US8**		**PAGE 1 OF 2**

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM FAIRCHILD MKT−MAB08A TO ON SEMI-CONDUCTOR. REQ. BY I. HYLAND.	31 DEC 2016

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

◊