NCP11184, NCP11185, NCP11186, NCP11187

Product Preview

mWSaver® Integrated Power Switcher with 800 V SJ MOSFET for Offline SMPS

NCP1118x integrates a current−mode PWM controller employing mWSaver technology with a highly robust 800 V MOSFET providing enhanced performance of flyback converters.

The mWSaver technology reduces switching frequency at light−load condition and avoid acoustic−noise problems and even enables the power supply to meet international power conservation requirements, such as Energy Star®. The standby power consumption can be under 25 mW for most power supply designs. Additionally, the NCP1118x integrates an internal high−voltage startup circuitry, frequency−hopping function and slope compensation.

Protections feature a feedback pin open−loop protection, line under−voltage protection (brownout protection) and overvoltage protection using an input−voltage sensing pin (VIN) operated with auto−recovery operation.

Features

- Integrated 800 V Super Junction MOSFET
- Build−in Start−up, Soft−Start, and Slope Compensation
- mWSaver Technology Provides Industry's Best−in−Class Standby Power
- Proprietary Asynchronous Frequency Hopping Technique to Reduce EMI
- Fixed PWM Frequency: 65/100/130 kHz
- Programmable Constant Power Limit for Entire Input−Voltage Range
- Brown−In/Out Protection with Hysteresis and Line Over−Voltage Protection to Detect Input Voltage through VIN Pin
- VDD Under−Voltage Lockout (UVLO)
- Current−Sense Short Protection (CSSP) and Abnormal Over−Current Protection (AOCP)
- Internal Thermal Shutdown (TSD) with Hysteresis
- Auto−Restart for All Protections include Feedback Open−Loop Protection (OLP), VDD Over−Voltage Protection (OVP)

Typical Applications

- Isolated Auxiliary Power Supplies
- White Good Applications

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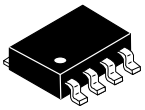
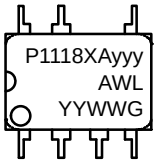
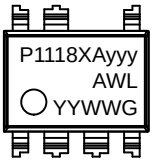
PDIP−7
(PDIP−8 LESS PIN 6)
CASE 626A



LSOP−7
(PDIP−8 LESS PIN 3)
CASE 707AA

MARKING DIAGRAMS

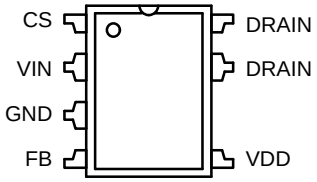




X	= $R_{DS(on)}$
A	= Auto−recovery
yyy	= Oscillator Frequency (065, 130)
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.



(Top View)

Table 1. PIN FUNCTION DESCRIPTION

PIN # DIP 7, LSOP−7	Name	Description
1	CS	Current sense. The sensed voltage is used for peak−current−mode control and cycle−by−cycle current limiting.
2	VIN	Line−voltage detection. The line−voltage detection is used for brownout protection with hysteresis. Constant output power limit over universal AC input range is also achieved using this VIN pin. It is suggested to add a low−pass filter to filter out line ripple on the bulk capacitor. Pulling VIN HIGH also triggers auto−restart protection.
3	GND	Ground
4	FB	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the currentsense signal on the SENSE pin.
5	VDD	Power supply. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
6, 7	DRAIN	This pin is connected to internal high voltage startup circuit and the drain pin of an integrated MOSFET. Typically, this pin is directly connected to one of terminals of the transformer. At initial startup or restart mode, operating voltage is powered through this pin.

Table 2. PRODUCTS INFORMATION & INDICATIVE MAXIMUM OUTPUT POWER

Part Number	PKG	Switching Frequency	Max. $R_{DS(on)}$ (Ω)	Output Power Table (W)		
				Adapter	Open Frame	
				85 ~ 265 V_{AC}	85 ~ 265 V_{AC}	230 V_{AC}
NCP11184A065PG	PDIP7	65 kHz	2.25	18	25	37
NCP11185A065PG			1.3	22	30	45
NCP11186A065PG			0.85	26	35	52
NCP11187A065PG			0.65	30	40	60
NCP11184A100PG		100 kHz	2.25	18	25	37
NCP11187A100PG			0.65	30	40	60
NCP11184A130PG		130 kHz	2.25	18	25	37
NCP11185A130PG			1.3	22	30	45
NCP11184A065LPG	LSOP−7	65 kHz	2.25	18	25	37
NCP11185A065LPG			1.3	22	30	45
NCP11187A065LPG			0.65	30	40	60
NCP11184A100LPG		100 kHz	2.25	18	25	37

Table 3. QUICK SELECTION TABLE

Device	Max. $R_{DS(ON)}$ [Ω]	Frequency [kHz]	Package
NCP11184	2.25	65	PDIP−7, LSOP−7
		100	PDIP−7, LSOP−7
		130	PDIP−7
NCP11185	1.3	65	PDIP−7, LSOP−7
		130	PDIP−7
NCP11186	0.85	65	PDIP−7
NCP11187	0.65	65	PDIP−7, LSOP−7
		100	PDIP−7

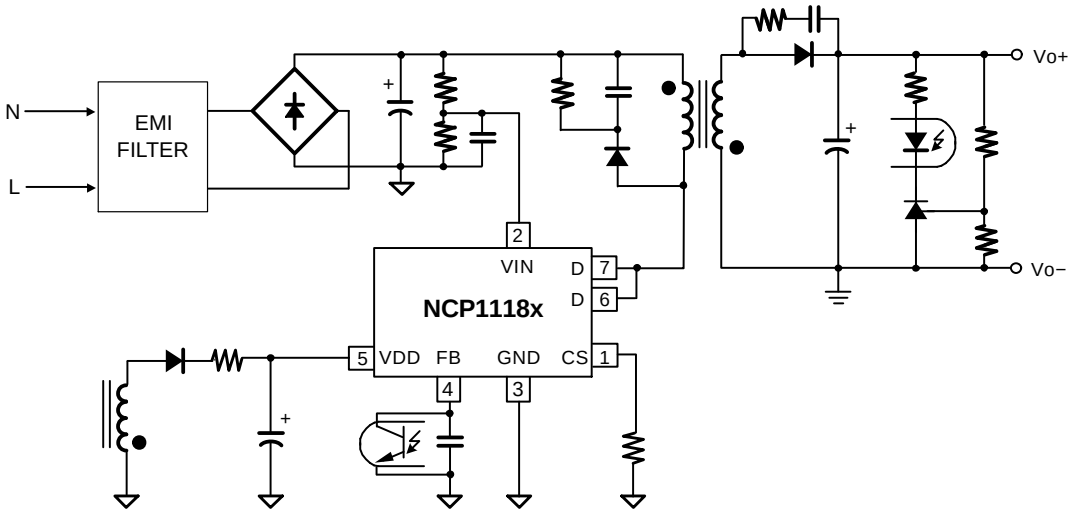


Figure 1. Typical Application, VIN Connects to Rectified Input Voltage

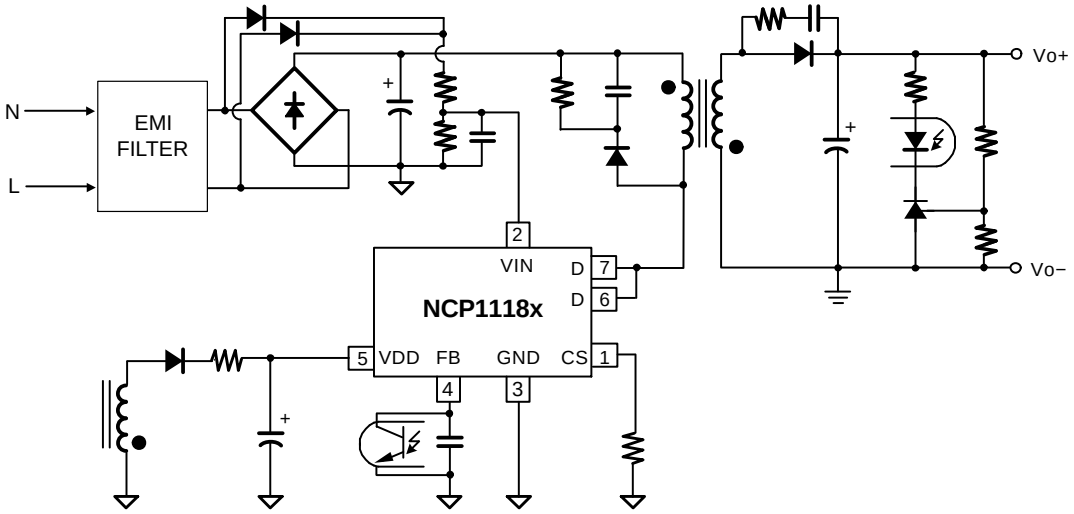


Figure 2. Typical Application, VIN Connects to AC−Side of Input Voltage

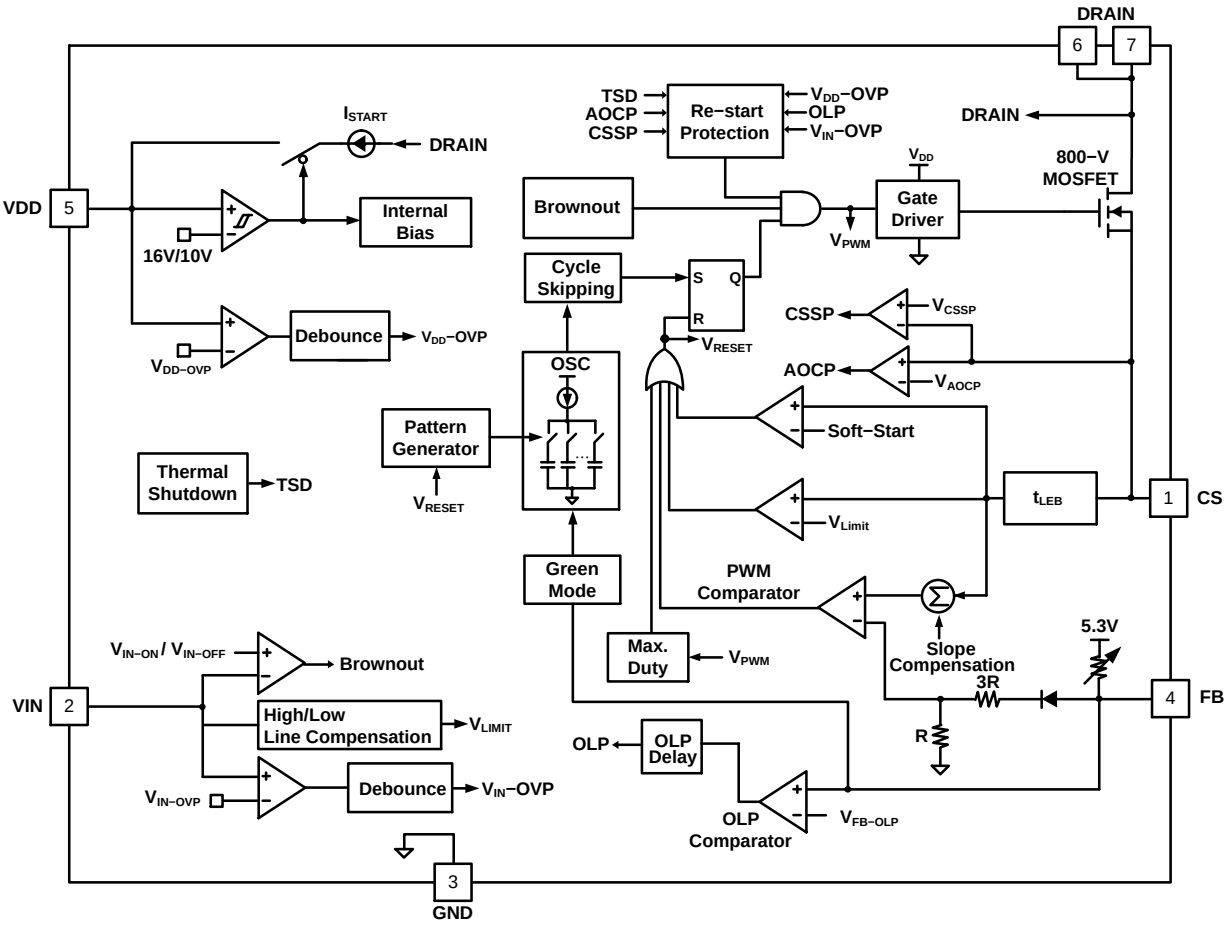


Figure 3. Simplified Internal Block Diagram

Table 4. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Junction−to−Ambience Thermal Impedance (Note 1) PDIP−7, LSOP−7, with 0.36 square inch, 2 oz. copper landing area PDIP−7, LSOP−7, with 1 square inch, 2 oz. copper landing area	$R_{\theta JA}$	TBD	°C/W
Junction−to−Lead Thermal Impedance (Note 2) PDIP−7, LSOP−7	$R_{\theta JL}$	TBD	°C/W

1. JEDEC recommended environment as noted in JESD51−2
2. Measured from pin #7 (DRAIN) since it is the surface that copper area for heat sink is connected.

Table 5. RECOMMENDED OPERATING RANGE

Rating	Symbol	Min	Max	Unit
Junction Temperature	T_J	−40	+125	°C
Maximum Working Drain Current (T_J = 100°C) NCP11184 NCP11185 NCP11186 NCP11187	I_D		 1.7 2.5 3.1 3.6	A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. MAXIMUM RATINGS TABLE (Note 3)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.3 to 30	V
FB−pin Input Voltage	V_{FB}	−0.3 to 5.5	V
CS−pin Input Voltage	V_{CS}	−0.3 to 5.5	V
VIN−pin Input Voltage	V_{VIN}	−0.5 to 5.5	V
DRAIN−pin Input Voltage	V_{DRAIN}	−0.3 to 800	V
Maximum Pulsed Drain Current (Notes 4, 5) NCP11184 NCP11185 NCP11186 NCP11187	I_{DM}	 6.0 10.8 15.9 21.3	A
Single Pulsed Avalanche Energy (Note 6) NCP11184 NCP11185 NCP11186 NCP11187	E_{AS}	 21.6 48 114 204	mJ
Power Dissipation (PDIP−7, LSOP−7)	P_D	1.25	W
Operating Junction Temperature (Note 7)	T_J	−40 to +150	°C
Storage Temperature	T_{STG}	−40 to +150	°C
Lead Temperature, Wave Soldering or IT, 10 seconds	T_L	260	°C
ESD Capability HBM, JESD22−A114 All Pins Except DRAIN Pin DRAIN Pin		 5.5 (TBD) 2.0 (TBD)	kV
ESD Capability CDM, JESD22−C101		2.0 (TBD)	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All voltage values, except differential voltages, are given with respect to the ground terminal.
4. Repetitive rating pulse width is limited by maximum junction temperature.
5. The real value of IDM will be updated with characterization result.
6. Test conditions: L = 51 mH.
7. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

Table 7. ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DRAIN AND MOSFET SECTION						
Power Switch and Start−up Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	BV_{DSS}	800			V
Power Switch and Start−up Off−State Leakage Current	CS and GND are shorted, $V_{DD} \geq V_{DD-OVP}$, V_{DRAIN} = 800 V T_J = 25°C T_J = 125°C	I_{DSS}			 TBD TBD	μA
Drain−Source On−State Resistance	V_{DD} = 15 V, T_J = 25°C NCP11184, I_D = 0.3 A NCP11185, I_D = 0.4 A NCP11186, I_D = 0.5 A NCP11187, I_D = 0.6 A	$R_{DS(on)}$		 1.87 1.05 0.71 0.53	 2.25 1.3 0.85 0.65	Ω
Rise Time (Note 8)	V_{DS} = 400 V, V_{DD} = 15 V, 10 → 90% NCP11184 NCP11185 NCP11186 NCP11187	t_r		 TBD TBD TBD TBD		ns
Fall Time (Note 8)	V_{DS} = 400 V, V_{DD} = 15 V, 90 → 10% NCP11184 NCP11185 NCP11186 NCP11187	t_f		 TBD TBD TBD TBD		ns
VDD SECTION						
Start Threshold Voltage		V_{DD-ON}		16		V
Protection Mode		V_{DD-OFF}		9.6		V
Normal Mode		V_{UVLO}		7.8		V
Operating Supply Current	V_{DD} = 15 V, V_{FB} = 3 V 65 kHz Version 100 kHz Version 130 kHz Version	I_{DD-OP}			 TBD TBD TBD	mA
Operating Supply Current without switching	V_{DD} = 15 V, V_{FB} = 0 V	I_{DD-OP2}			TBD	μA
Threshold Voltage on V_{DD} for HV JFET Turn−On after Protection Mode		V_{DD-OLP}		7.4		V
Internal Sink Current after Protection Mode	V_{DD-OLP} + 0.1 V	I_{DD-OLP}		90		μA
Threshold Voltage to release from Latch Protection	Latch version	V_{DD-LH}		6.9		V
Additional Sink Current after Latch−Mode Protection	Latch version, V_{DD} = 7 V	I_{DD-LH}		30		μA
V_{DD} Over−Voltage Protection		V_{DD-OLP}		26		V
V_{DD} Over−Voltage Protection Debounce Counting Number	65−kHz version 100/130−kHz version	N_{VDDOVP}		6 12		pulse
V_{DD} Level for I_{START1} to I_{START2} Transition		$V_{DD-INHIB}$		2.1		V
Startup Current Flowing out of V_{DD} Pin	V_{DRAIN} = > 40 V, V_{DD} = 0 V	I_{START1}		0.5		mA
Startup Current Flowing out of V_{DD} Pin	V_{DRAIN} = > 40 V, $V_{DD} = V_{DD-ON} - 0.5$ V	I_{START2}		4.5		mA
Threshold Voltage to Force Z_{FB} Reset	$V_{FB} < V_{FB-ZDC}$, V_{DD} falling	V_{DD-ZFB}		10		V

8. Tested on a Flyback power converter. Result of just one golden sample.
9. Guaranteed by design.

Table 7. ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION						
Switching Frequency	V_{FB} = 4.5 V (V_{FB-OLP}) 65−kHz Version 100−kHz Version 130−kHz Version	f_{OSC}		 65 100 130		kHz
Frequency Modulation Range	V_{FB} = 4.5 V (V_{FB-OLP}) 65−kHz Version 100−kHz Version 130−kHz Version	f_M		 ±5.2 ±8.0 ±10.4		kHz
Hopping Period		t_{HOP}		12.5		ms
Green−Mode Entry Frequency	V_{FB} = 3 V (V_{FB-OLP}) 65−kHz Version 100−kHz Version 130−kHz Version	f_{OSC-N}		 58.5 90 117		kHz
Green−Mode Ending Frequency	V_{FB} = 2.4 V (V_{FB-OLP}) 65−kHz Version 100−kHz Version 130−kHz Version	f_{OSC-G}		 25.6 28 29		kHz
Entering−Burst Frequency	V_{FB} = V_{FB-ZDC}	$f_{OSC-ZDC}$		23		kHz
Frequency Variation vs. V_{DD} Deviation	V_{DD} = 11 V to 22 V	f_{DV}			5	%
Frequency Variation vs. Temperature Deviation (Note 9)	T_A = T_J =−40 to 125°C	f_{DT}			5	%
VIN SECTION						
PWM Turn−On (Brown−in) Threshold Voltage		V_{IN-ON}		0.9		V
PWM Turn−Off (Brownout) Threshold Voltage	Default Option	V_{IN-OFF}		0.70 0.80		V
Brown−out Timer	V_{FB} = $V_{FB-OPEN}$ 65−kHz Version 100−kHz Version	$t_{D-VINOFF}$		 62.5 81.25		ms
Threshold Voltage of V_{IN} Over−Voltage Protection	Default Option A	V_{IN-OVP}		3.85 4.15		V
Hysteresis for Recovery Level of V_{INOVP} Comparator	Default Option A	$V_{IN-OVPHYS}$		0.2 0.5		V
Debounce Time of V_{IN} Over−Voltage Protection	65−kHz version 100/130−kHz version	t_{VINOVP}		6 12		pulse
CURRENT SENSE SECTION						
Threshold Voltage for Current Limit	V_{IN} = 1 V V_{IN} = 3 V	V_{LIMIT}		0.83 0.70		V
Current Limit Delay Time		t_{CLD}		100		ns
Leading−Edge Blanking Time	Soft Start (100/130−kHz version) Steady State	t_{LEB}		150 300		ns
Threshold of Abnormal Over−Current Protection	Enable after t_{SS}	V_{AOCP}		1.25		V
Debounce time for pulse of AOCP to be Counted		$t_{ON-AOCP}$		110		ns
Delay Time of Abnormal Over−Current Protection	Counting GATE Pulses	N_{AOCP}		3		Pulses
Treshold Voltage for CSSP	V_{IN} = 1 V V_{IN} = 3 V	V_{CSSP}		90 180		mV

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9. Guaranteed by design.

Table 7. ELECTRICAL CHARACTERISTICS (T_J = −40°C to +125°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION						
Minimum On−time of PWM Signal to Trigger CSSP	65−kHz version 100−kHz version 130−kHz version	$t_{ON-CSSP}$		4.6 3.0 2.3		μs
Delay Time of CSSP when CSSP Condition is met	Counting GATE Pulses	N_{CSSP}		4		Pulses
Period During Soft−Start Time	$V_{FB} = V_{FB-OPEN}$ 65/130−kHz Version 100−kHz Version	t_{SS}		 5.5 7.15		ms
Maximum Duty Cycle		D_{MAX}		80		%
Slope Compensation (Note 9)	Normalized to CS Signal 65−kHz Version 100−kHz Version 130−kHz Version	S_E		 30 46 60		mV/μs
FEEDBACK INPUT SECTION						
Internal FB Voltage Attenuation		A_V		1/4.0		–
Input Impedance	V_{FB} = 4 V	Z_{FB}		15.25		kΩ
Input Impedance in Burst Mode	$V_{FB} < V_{FB-ZDC}$, $V_{DD} > V_{DD-ZFB}$	Z_{FB-ZDC}		75		kΩ
Time Duration of Switching from Z_{FBZDC} to Z_{FB}		t_{ZFB}		6.4		ms
The Maximum Clamp of FB Voltage	FB Pin Open	$V_{FB-OPEN}$		5.1		V
FB Open−Loop Protection Triggering Level		V_{FB-OLP}		4.5		V
Delay Time of FB Pin Open−loop Protection	$V_{FB} = V_{FB-OPEN}$ 65/130−kHz Version 100−kHz Version	t_{D-OLP}		 62.5 81.25		ms
Green−Mode Entry FB Voltage		V_{FB-N}		3.0		V
Green−Mode Ending FB Voltage		V_{FB-G}		2.4		V
FB Threshold Voltage for Zero−Duty Recovery		$V_{FB-ZDCR}$		1.8		V
FB Threshold Voltage for Zero−Duty		V_{FB-ZDC}		1.6		V
ZDC Hysteresis	$V_{FB-ZDCR} - V_{FB-ZDC}$	$V_{FB-ZDCHYS}$		0.2		V
THERMAL SHUT DOWN SECTION						
Protection Junction Temperature (Note 9)		T_{TSD}	128			°C
Hysteresis of Restarting Junction Temperature		$T_{TSD-HYS}$		50		°C

8. Tested on a Flyback power converter. Result of just one golden sample.
9. Guaranteed by design.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Functional Descriptions

Startup & Soft−Start

At startup, an internal high−voltage current source connecting the DRAIN pin supplies internal bias and charges the external capacitor connected to the V_{DD} pin. When V_{DD} is lower than $V_{DD-INHIB}$, the charging is a smaller I_{START1}. When V_{DD} exceeds $V_{DD-INHIB}$, charging current becomes a larger I_{START2}. The lower charging current is designed to reduce power dissipation when V_{DD} is shorted to GND.

When V_{DD} level reaches V_{DD-ON}, the internal startup current source deactivates. At this moment, only the V_{DD} capacitor supplies an operating current to NCP1118X before the auxiliary winding of the main transformer provides the operating current. Moreover, the IC includes a function of soft−start to minimize the inrush current at startup. The built−in soft−start circuit significantly reduces the startup current spike and output voltage overshoot.

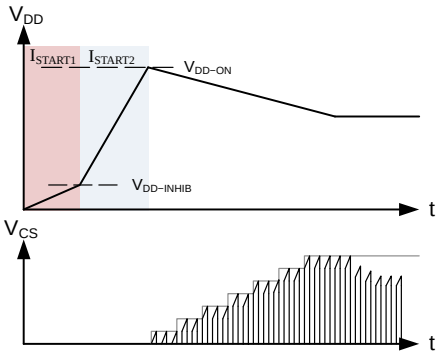


Figure 4. Startup and Soft Start

Under−Voltage Lockout (UVLO)

The turn−on and turn−off thresholds are fixed internally at 16 V and 7.8 V in normal mode as shown in Figure 5. During startup, the hold−up capacitor must be charged to 16 V through the internal high−voltage current source to enable the IC. The hold−up capacitor continues to supply V_{DD} before the energy can be delivered from auxiliary winding of the main transformer. V_{DD} must not drop below 7.8 V during startup. This large UVLO hysteresis window helps reducing size of the hold−up capacitor.

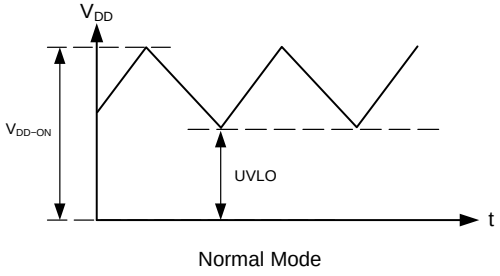


Figure 5. V_{DD} Behavior at Normal Mode

Auto Restart Operation

NCP1118x offers auto restart operation for the protections like feedback open−loop protection (OLP), V_{DD} over−voltage protection (V_{DD} OVP), and over−temperature protection (OTP). Once one of the protections is trigger, the IC stops operation immediately and V_{DD} starts to decrease. When V_{DD} decreased to V_{DD-OFF}, biaing current drawn from V_{DD} pin is reduced to I_{DD-OLP}, which stretches delay time for restart. When V_{DD} decreases to V_{DD-OLP}, the internal high−voltage startup circuit charges V_{DD} again to re−initiate operation.

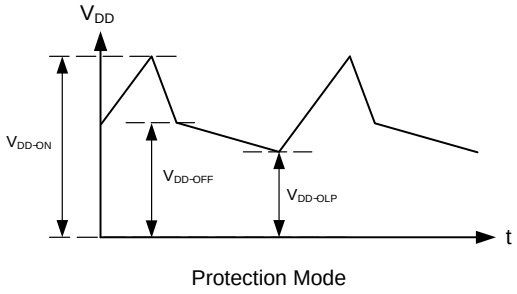


Figure 6. V_{DD} Behavior at Protection Mode

Operating Current

Operating current of NCP1118x is below 2 mA, and it is even lower in burst−mode operation. The low operating current enables better efficiency and reduces the requirement of V_{DD} hold−up capacitance.

Green−Mode Operation

The proprietary green−mode function provides reduced switching frequency in light−load and no−load conditions. V_{FB}, which is derived from the voltage feedback loop, is taken as a reference signal for green−mode operation. Once V_{FB} is decreased, switching frequency is also decreased to the minimum green−mode frequency V_{FB-ZDC}.

Current Sensing / PWM Current Limiting

Peak−current−mode control is utilized to regulate output voltage and provide pulse−by−pulse current limiting. The switching current is detected using the current−sensing resistor connecting at CS pin. The PWM duty cycle is determined by comparing this current sense signal V_{CS} with the feedback voltage V_{FB}. When V_{CS} reaches around $V_{COMP} = (V_{FB}–0.6)/4$, the PWM comparator generates a signal of the switch turns−off immediately.

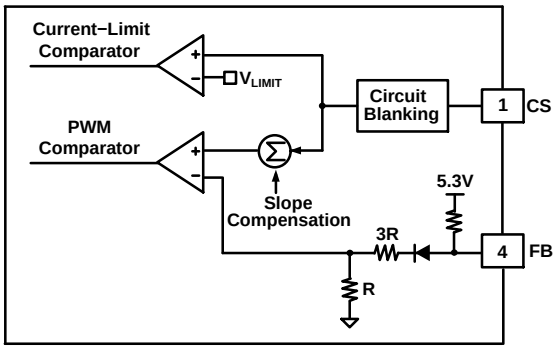


Figure 7. Current Limit & PWM Comparator

A current−limit comparator is used to set highest peak current through the power switch. For constant output power limit over universal input−voltage range, the peak−current threshold is adjusted by the voltage of V_{IN} pin. V_{IN} pin is connected to the rectified AC input line voltage through the resistive divider. The threshold voltage decreases as V_{IN} increases. Different V_{LIMIT} compensates the different maximum output power due to propagation delay.

Figure 8 shows V_{Limit} variation depending on V_{IN}.

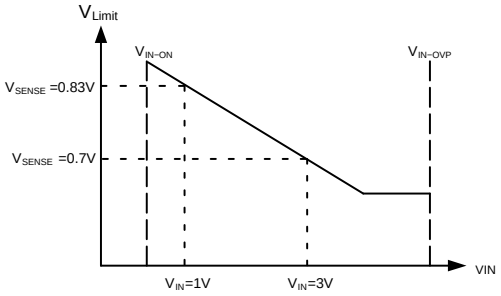


Figure 8. V_{IN} vs. V_{CS}

Leading−Edge Blanking (LEB)

Whenever the integrated MOSFET is turned on, a leading edge current occurs on the sense resistor. To avoid premature termination of the gate turn−on signal, a leading−edge blanking time is employed. During this blanking period, the current−limit comparator is disabled and the gate turn−on signal is maintained.

Slope Compensation

NCP1118x has built−in slope compensation to prevent sub−harmonic oscillator and improve stability. A sawtooth signal is generated when PWM pulse width exceeds t_{D-SE}. Initial voltage of the sawtooth waveform is 0.7 V. A weighted sum is then performs on current−sense signal and the sawtooth signal with weighting of 5/6 and 1/6 for each signal.

Slope of the sawtooth signal is 0.149 V/μs for 65−kHz version and 0.298 V/μs for 130−kHz version. The delay time t_{D-SE} is 6 μs for 65−kHz version and 3 μs for 130−kHz version, which is around 40% of duty cycle when operating at rated frequency.

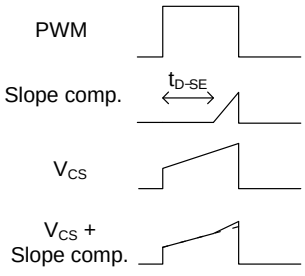


Figure 9. Slope Compensation

V_{DD} Over−Voltage Protection

V_{DD} over−voltage protection prevents damage due to abnormal conditions. Once the V_{DD} voltage is over the over−voltage protection voltage (V_{DD-OVP}), and lasts for $t_{D-VDDOVP}$, the PWM will be disabled. When the V_{DD} voltage drops below the V_{DD-OLP}, the internal startup circuit turns on, and V_{DD} is charged to V_{DD-ON} to restart IC.

Burst Mode and Feedback Impedance Switching

NCP1118X actively varies FB−pin impedance (Z_{FB}) in burst mode to reduce no−load power consumption. This technique can further reduce operating current of the controller when FB−pin voltage drops below V_{FB-ZDC}.

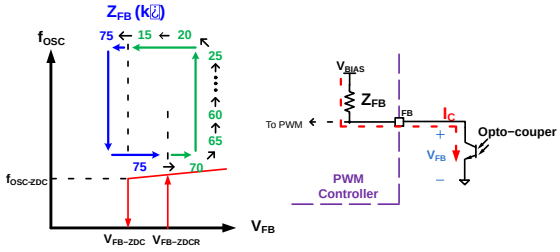


Figure 10. Z_{FB} Switching

Brownout Protection

Since the V_{IN} pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If V_{IN} is less than 0.7 V, the PWM output is shut off. When V_{IN} reaches over 0.9 V, the PWM output is turned on again. The hysteresis window for ON/OFF is around 0.2 V. The brownout voltage setting is determined by the potential divider formed with R_{Upper} and R_{Lower}. Equations to calculate the resistors are shown below:

$$V_{IN} = \frac{R_{Lower}}{R_{Lower} + R_{Upper}} \times V_{AC} \cdot \sqrt{2} \qquad \text{(eq. 1)}$$

Input−Voltage Over−Voltage Protection

VIN pin is also used to realize over−voltage protection for AC input. More, while VIN voltage has been higher than V_{IN-OVP} when V_{DD} reaches V_{DD-ON} by HV start−up, switching operation will not be initiated.

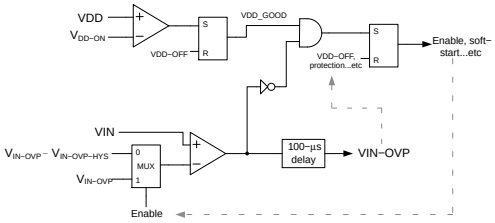


Figure 11. VIN OVP

Abnormal Over−Current Protection (AOCP)

When conditions like shorted output, shorted secondary−side rectifier, and shorted transformer are met, an extremely high current can flow through power switch during leading−edge blanking time. Even though NCP1118x has over−load protection, it may not survive from such a severe current stress for the delay time of

over−load protection. AOCP is designed to protect NCP1118x from this kind of fault. If current−sensing signal exceeds AOCP threshold level for three consecutive switching periods, switching operation will be shut down to protect the power switch.

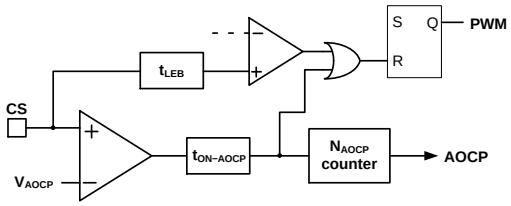


Figure 12. AOCP Logic

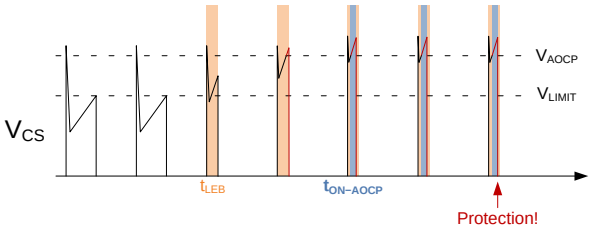


Figure 13. AOCP Waveform

Current−Sense Short Protection

When CS pin is shorted to GND pin due to soldering defect, current−sense signal is not properly obtained. It causes current−mode PWM being not able to operate as designed. In this situation, PWM on−time will be large while current−sense gets no signal. Drain current will be out of control.

To protect power switch from this condition, NCP1118x shuts down by current−sense short protection (CSSP) when current−sense signal is kept low while PWM on−time is large enough. Treshold voltage of judging CSSP condition varies with VIN−pin voltage.

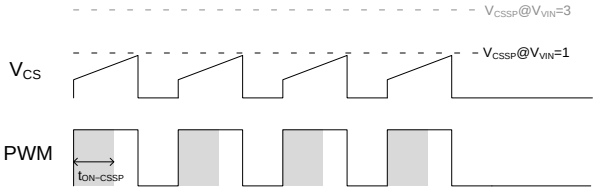


Figure 14. CSSP Waveform

Thermal Shutdown

Thermal shutdown limits total power dissipation on chip. When the junction temperature exceeds T_{TSD}, the thermal sensor signals the shutdown logic and turns off most of the internal circuitry. The chip will resume operation if junction temperature drops below $T_{TSD}−T_{TSD−HYS}$. Thermal shutdown is designed to protect the NCP1118X in the event of a fault condition. For continual operation, the controller should not exceed the absolute maximum junction temperature of T_J = +125°C.

Over−Load Protection and Limited Power Control

The FB voltage is saturated HIGH when the power supply output voltage drops below its nominal value and shunt regulator (ex. KA431) does not draw current through the opto−coupler. This occurs when the output feedback loop is open or output is short circuited. If the FB voltage is higher than a built−in threshold $V_{FB−OLP}$ for longer than $t_{D−OLP}$, PWM output is turned off. As PWM output is turned off, V_{DD} begins decreasing since no more energy is delivered from the auxiliary winding.

As the protection is triggered, V_{DD} enters into auto−restart UVLO mode, which extends the time it take to restart operation. This prevents the power supply from overheating at the overload conditions.

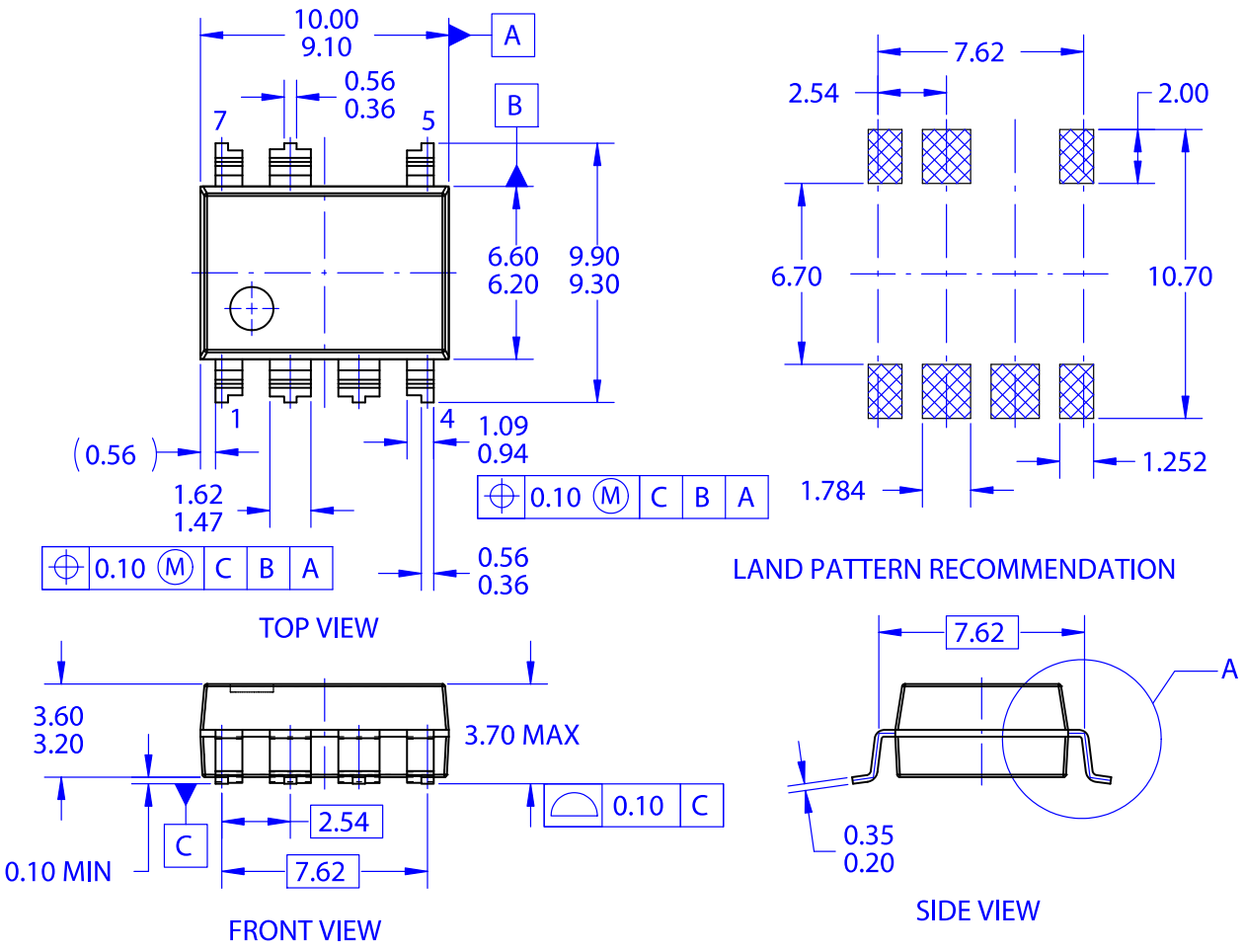
ORDERING INFORMATION

Device	$R_{DS(ON)}$ (Ω)	f_{OSC} (kHz)	Package	Shipping†
NCP11184A065PG	2.25	65	PDIP−7 (Pb−Free)	50 Units / Rail
NCP11185A065PG	1.3	65		
NCP11186A065PG	0.85	65		
NCP11187A065PG	0.65	65		
NCP11184A100PG	2.25	100		
NCP11187A100PG	0.65	100		
NCP11184A130PG	2.25	130		
NCP11185A130PG	1.3	130		
NCP11184A065LPG	2.25	65	LSOP−7 (Pb−Free)	50 Units / Rail
NCP11185A065LPG	1.3	65		
NCP11187A065LPG	0.65	65		
NCP11184A100LPG	2.25	100		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PDIP7 MINUS PIN 6 GW
CASE 707AA
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED
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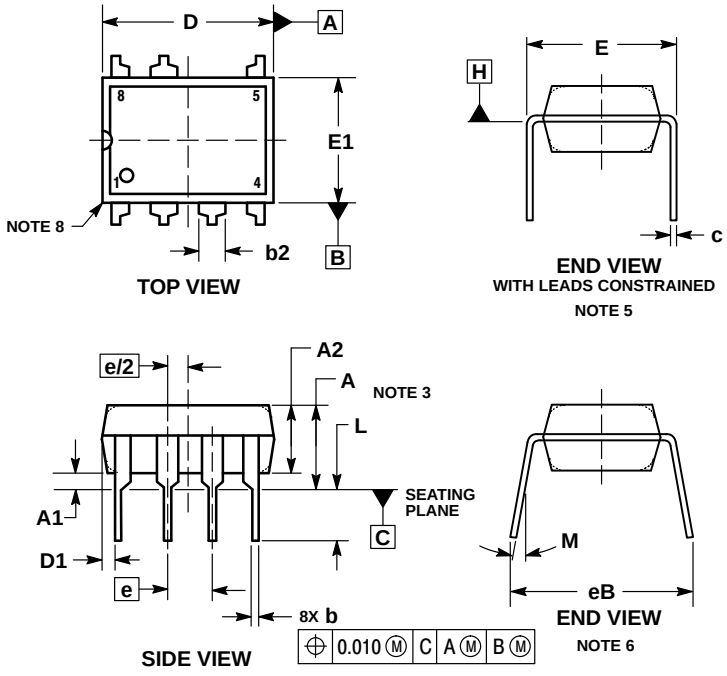
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009

PACKAGE DIMENSIONS

PDIP−7 (PDIP−8 LESS PIN 6)
CASE 626A
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	−−−−	0.210	−−−	5.33
A1	0.015	−−−−	0.38	−−−
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	−−−−	0.13	−−−
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	−−−−	0.430	−−−	10.92
L	0.115	0.150	2.92	3.81
M	−−−−	10°	−−−	10°

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