NCP136

LDO Regulator - Very Low Dropout, CMOS, Bias Rail

700 mA

ON Semiconductor®

www.onsemi.com

The NCP136 is a 700 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP136 features low I_Q consumption. The WLCSP6 1.4 mm x 0.8 mm Chip Scale package is optimized for use in space constrained applications.

Features

- Input Voltage Range: V_{OUT} to 5.5 V
- Bias Voltage Range: 2.5 V to 5.5 V
- Fixed Voltage Version Available
- Output Voltage Range: 0.5 V to 1.8 V (Fixed)
- ±1% Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra−Low Dropout: Typ. 40 mV at 700 mA
- Very Low Bias Input Current of Typ. 80 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 10 μF Ceramic Capacitor
- Available in WLCSP6 − 1.4 mm x 0.8 mm, 0.4 mm pitch Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

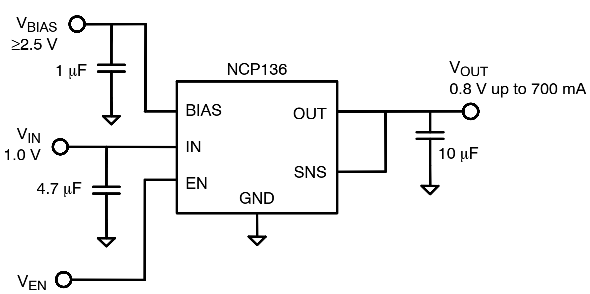
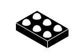
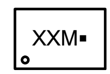


Figure 1. Typical Application Schematic



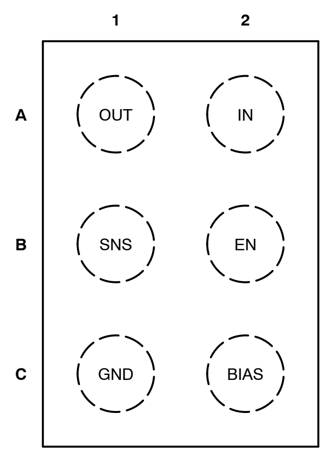
WLCSP6, 1.4x0.8x0.33
CASE 567XK

MARKING DIAGRAM



XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

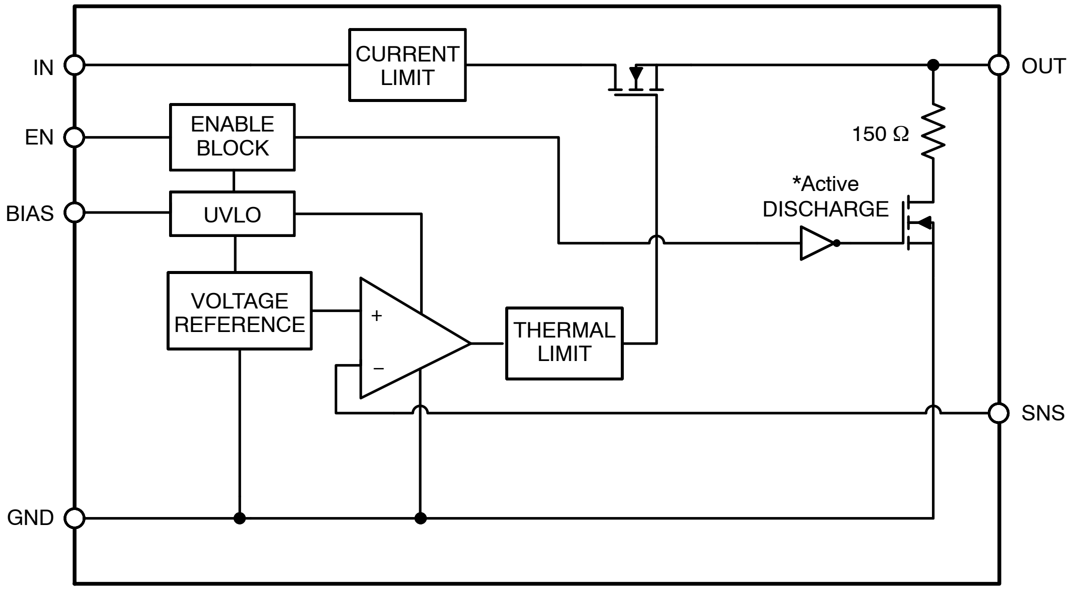
PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering information, marking and shipping information on page 11 of this data sheet.



*Active output discharge function is present only in NCP136A and NCP136C option devices.

Figure 2. Simplified Schematic Block Diagram − Fixed Version

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin Name	Description
A1	OUT	Regulated Output Voltage pin
A2	IN	Input Voltage Supply pin
B1	SNS	Output voltage Sensing Input. Connect to Output on the PCB to output the voltage corresponding to the part version.
B2	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
C1	GND	Ground pin
C2	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to (V_{IN}+0.3) ≤ 6	V
Chip Enable, Bias and SNS Input	V_{EN}, V_{BIAS}, V_{SNS}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 1.4 mm x 0.8 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	69	°C/W

3. This junction−to−ambient thermal resistance under natural convection was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high_K (2s2p) 80 mm x 80 mm multilayer board with 1−ounce internal planes and 2−ounce copper on top and bottom. Top copper layer has a dedicated 1.6 sqmm copper area.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; V_{BIAS} = 2.7 V or (V_{OUT} + 1.6 V), whichever is greater, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 μF, C_{OUT} = 10 μF, C_{BIAS} = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		V_{IN}	V_{OUT} + V_{DO}		5.5	V
Operating Bias Voltage Range		V_{BIAS}	(V_{OUT} + 1.50) ≥ 2.5		5.5	V
Undervoltage Lock−out	V_{BIAS} Rising Hysteresis	UVLO		1.6 0.2		V
Output Voltage Accuracy		V_{OUT}		±0.5		%
Output Voltage Accuracy	$-40°C \le T_J \le 85°C$, $V_{OUT(NOM)} + 0.1\ V \le V_{IN} \le V_{OUT(NOM)}$ + 1.0 V, 2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V, 1 mA < I_{OUT} < 700 mA	V_{OUT}	−1.0		+1.0	%
V_{IN} Line Regulation	$V_{OUT(NOM)} + 0.1\ V \le V_{IN} \le 5.0$ V	$Line_{Reg}$		0.01		%/V
V_{BIAS} Line Regulation	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{BIAS} < 5.5 V	$Line_{Reg}$		0.01		%/V
Load Regulation	I_{OUT} = 1 mA to 700 mA	$Load_{Reg}$		1.5		mV
V_{IN} Dropout Voltage	I_{OUT} = 700 mA (Note 5)	V_{DO}		40	60	mV
V_{BIAS} Dropout Voltage	I_{OUT} = 700 mA, $V_{IN} = V_{BIAS}$ (Notes 5, 6)	V_{DO}		1.1	1.5	V
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$	I_{CL}	800	1450	2000	mA
SNS Pin Operating Current		I_{SNS}		0.1	0.5	μA
Bias Pin Quiescent Current	V_{BIAS} = 2.7 V, I_{OUT} = 0 mA	I_{BIASQ}		70	110	μA
Bias Pin Disable Current	$V_{EN} \le 0.4$ V	$I_{BIAS(DIS)}$		0.5	1	μA
Input Pin Disable Current	$V_{EN} \le 0.4$ V	$I_{VIN(DIS)}$		0.5	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”	$V_{EN(H)}$	0.9			V
	EN Input Voltage “L”	$V_{EN(L)}$			0.4	
EN Pull Down Current	V_{EN} = 5.5 V	I_{EN}		0.3	1	μA
Power Supply Rejection Ratio	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.2 V, V_{BIAS} = 3.0 V	PSRR(V_{IN})		75		dB
	V_{BIAS} to V_{OUT}, f = 1 kHz, I_{OUT} = 10 mA, $V_{IN} \ge V_{OUT}$ +0.5 V, $V_{OUT(NOM)}$ = 1.2 V, V_{BIAS} = 3.0 V	PSRR(V_{BIAS})		80		dB
Output Noise Voltage	$V_{IN} = V_{OUT}$ +0.5 V, f = 10 Hz to 100 kHz, $V_{OUT(NOM)}$ = 1.2 V	V_N		40		μV_{RMS}
Thermal Shutdown Threshold	Temperature increasing			160		°C
	Temperature decreasing			140		
Output Discharge Pull−Down	$V_{EN} \le 0.4$ V, V_{OUT} = 0.5 V, NCP136A and NCP136C option	R_{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
6. For fixed output voltages below 1.5 V, V_{BIAS} dropout does not apply due to a minimum Bias operating voltage of 2.5 V.

ELECTRICAL CHARACTERISTICS $-40°C \le TJ \le 85°C$; I_{OUT} = 1 mA, V_{EN} = 1 V, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, C_{BIAS} = 1 µF. Typical values are at T_J = +25°C. Min/Max values are for $-40°C \le T_J \le 85°C$ unless otherwise noted. (Note 7)

Parameter	Test conditions		Symbol	Min	Typ	Max	Unit
NCP136xFCT080TBG V_{BIAS} = 3 V, V_{IN} = 1.0 V							
Delay time	From assertion of V_{EN} to output voltage increase	'A' and 'B' option	t_{DELAY}		55		µs
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' and 'B' option	t_{RISE}		17		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' and 'B' option	t_{ON}		80		
NCP136xFCT088TBG V_{BIAS} = 3 V, V_{IN} = 1.1 V							
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{DELAY}		71		µs
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		16		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		97		
NCP136xFCT105TBG V_{BIAS} = 3 V, V_{IN} = 1.25 V							
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{DELAY}		71		µs
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		18		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		102		
NCP136xFCT110TBG V_{BIAS} = 3 V, V_{IN} = 1.3 V							
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{DELAY}		71		µs
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		19		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		105		
NCP136xFCT120TBG V_{BIAS} = 3 V, V_{IN} = 1.4 V							
Delay time	From assertion of V_{EN} to output voltage increase	'A' option	t_{ON}		70		µs
		'C' option			80		
Rise time	V_{OUT} rise from 10% to 90% $V_{OUT(NOM)}$	'A' option	t_{RISE}		21		
		'C' option			80		
Turn−On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$	'A' option	t_{ON}		108		
		'C' option			210		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

TYPICAL CHARACTERISTICS

At $T_J = +25°C$, $V_{IN} = V_{OUT(NOM)} + 0.3$ V, $V_{BIAS} = 2.8$ V, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)} = 1.2$ V, $I_{OUT} = 700$ mA, $C_{IN} = 4.7$ µF, $C_{BIAS} = 1$ µF, and $C_{OUT} = 10$ µF (effective capacitance), unless otherwise noted.

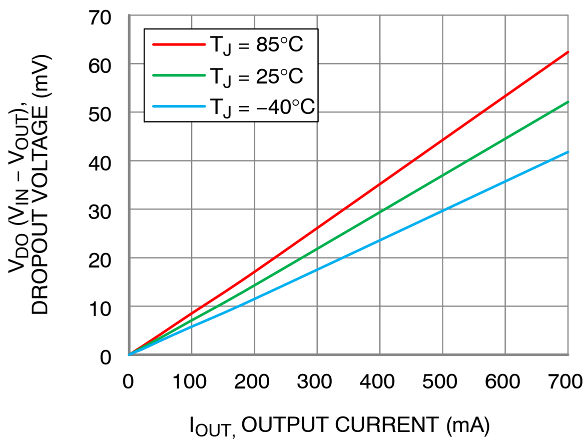


Figure 3. V_{IN} Dropout Voltage vs. I_{OUT} and T_J

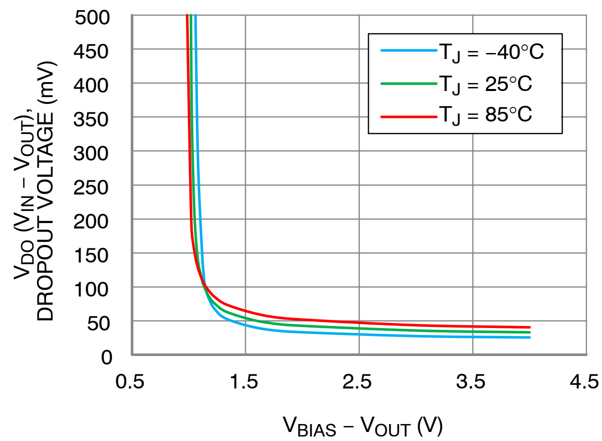


Figure 4. V_{IN} Dropout Voltage vs. $V_{BIAS} - V_{OUT}$ and T_J

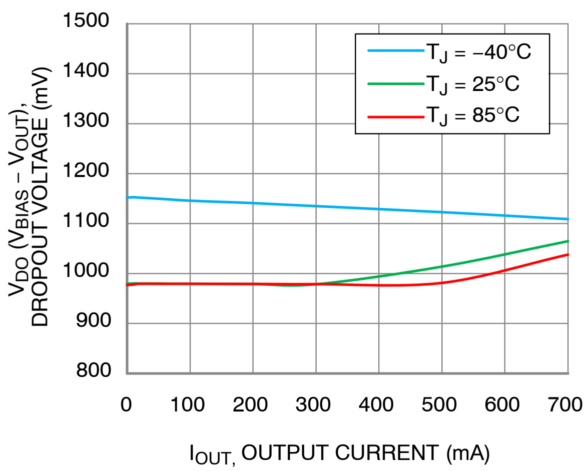


Figure 5. V_{BIAS} Dropout Voltage vs. I_{OUT} and T_J

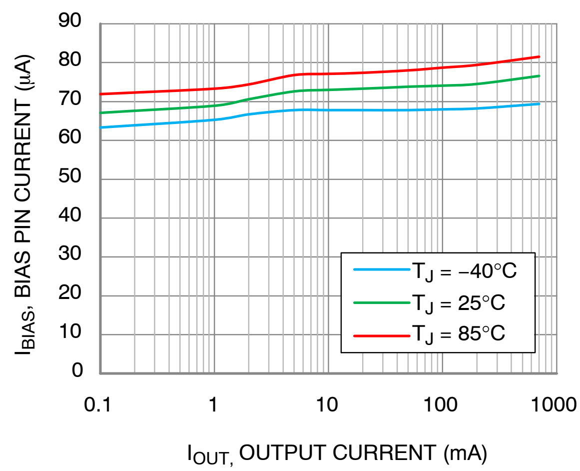


Figure 6. BIAS Pin Current vs. I_{OUT} and T_J

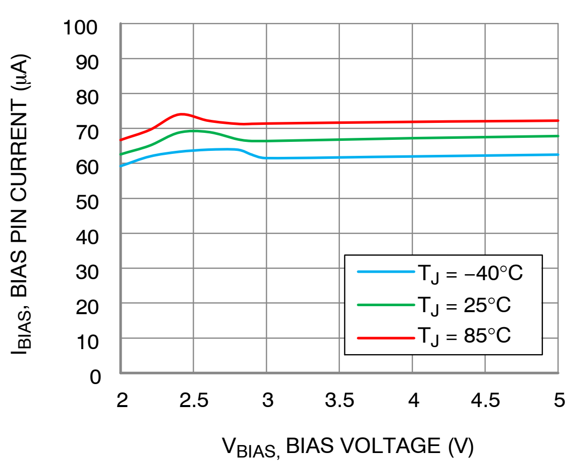


Figure 7. BIAS Pin Current vs. V_{BIAS} and T_J

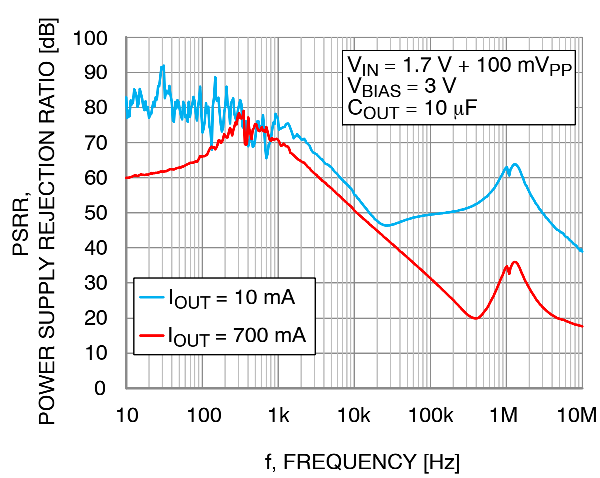


Figure 8. V_{IN} PSRR vs. Frequency

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, $V_{IN} = V_{OUT(NOM)}$ + 0.3 V, V_{BIAS} = 2.8 V, $V_{EN} = V_{BIAS}$, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 700 mA, C_{IN} = 4.7 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance), unless otherwise noted.

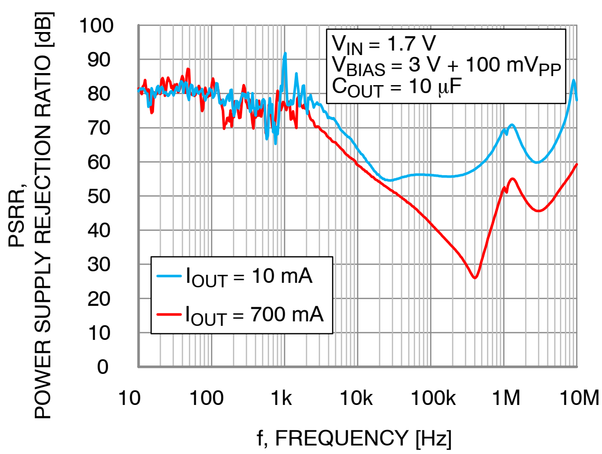


Figure 9. V_{BIAS} PSRR vs. Frequency

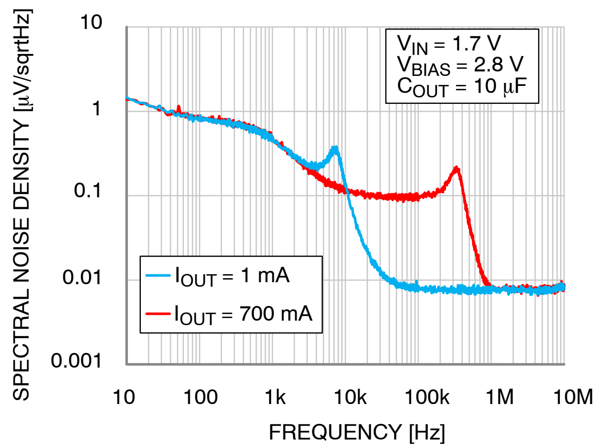


Figure 10. Output Voltage Spectral Noise Density vs. Frequency

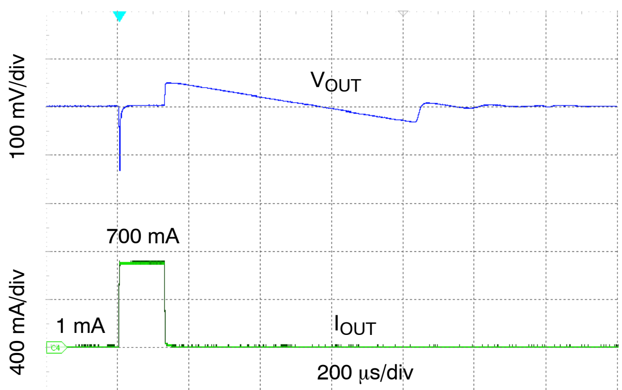


Figure 11. Load Transient Response, I_{OUT} = 1 mA to 700 mA in 1 μs, C_{OUT} = 10 μF

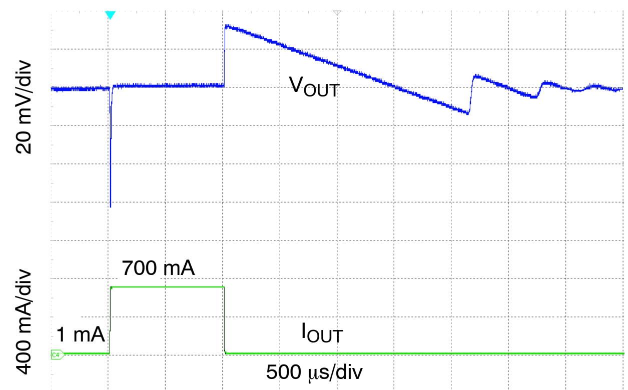


Figure 12. Load Transient Response, I_{OUT} = 1 mA to 700 mA in 1 μs, C_{OUT} = 47 μF

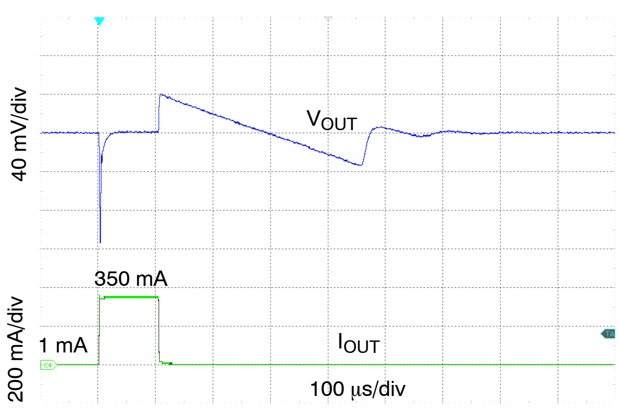


Figure 13. Load Transient Response, I_{OUT} = 1 mA to 350 mA in 1 μs, C_{OUT} = 4.7 μF

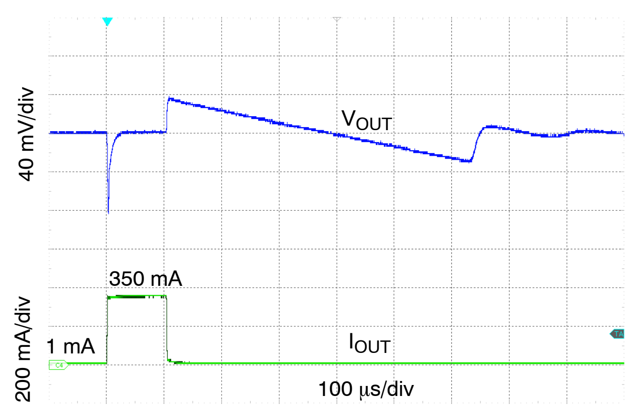


Figure 14. Load Transient Response, I_{OUT} = 1 mA to 350 mA in 1 μs, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, V_{BIAS} = 2.8 V, V_{EN} = V_{BIAS}, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 700 mA, C_{IN} = 4.7 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance), unless otherwise noted.

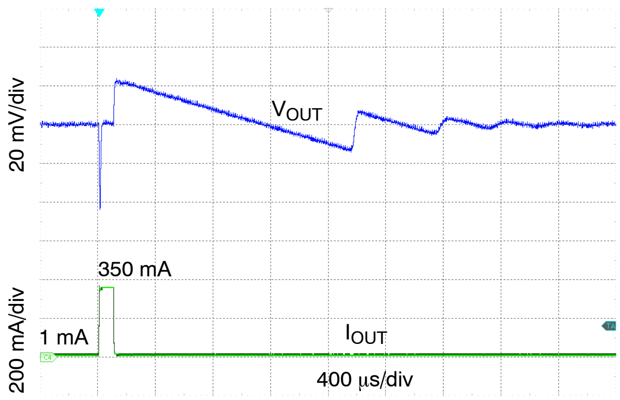


Figure 15. Load Transient Response, I_{OUT} = 1 mA to 350 mA in 1 μs, C_{OUT} = 47 μF

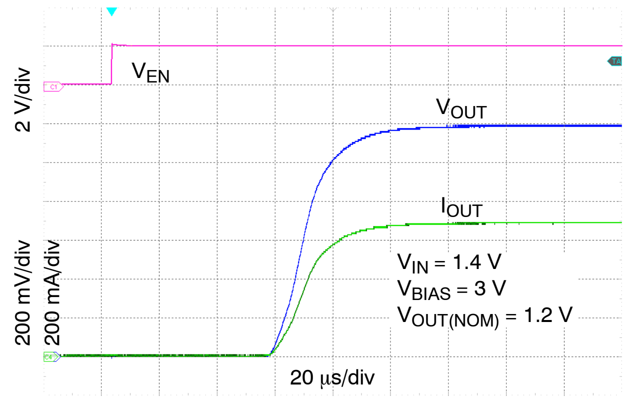


Figure 16. Enable Transient Response, C_{OUT} = 10 μF, I_{OUT} = 700 mA – A Option (Normal)

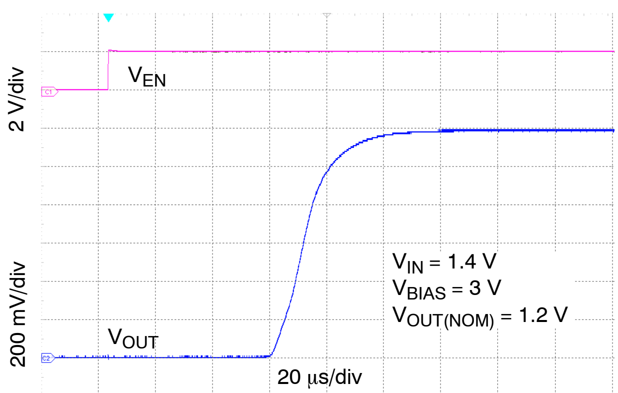


Figure 17. Enable Transient Response, C_{OUT} = 10 μF, I_{OUT} = 0 mA – A Option (Normal)

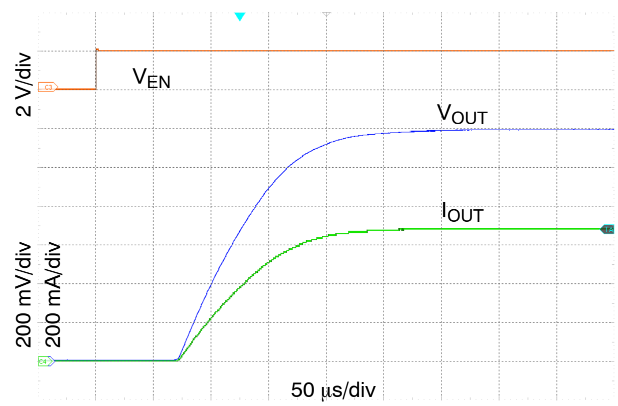


Figure 18. Enable Transient Response, C_{OUT} = 10 μF, I_{OUT} = 700 mA – C Option (Slow)

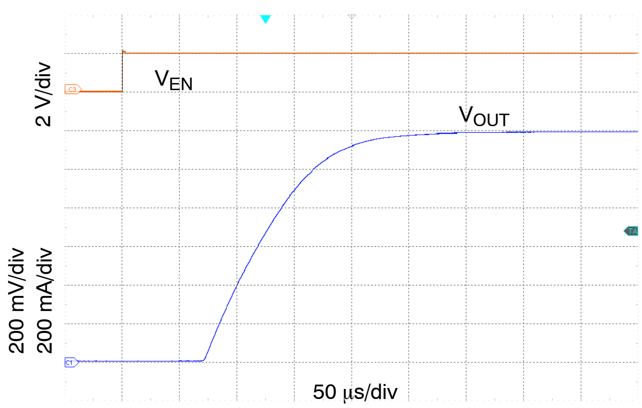


Figure 19. Enable Transient Response, C_{OUT} = 10 μF, I_{OUT} = 0 mA – C Option (Slow)

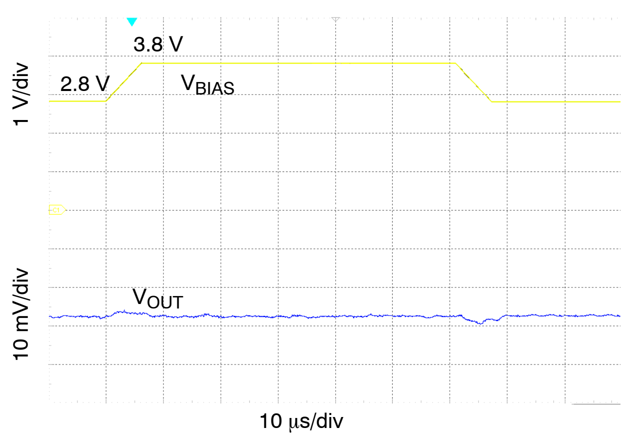


Figure 20. BIAS Line Transient Response, V_{BIAS} = 2.8 V to 3.8 V in 5 μs

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.3 V, V_{BIAS} = 2.8 V, V_{EN} = V_{BIAS}, $V_{OUT(NOM)}$ = 1.2 V, I_{OUT} = 700 mA, C_{IN} = 4.7 μF, C_{BIAS} = 1 μF, and C_{OUT} = 10 μF (effective capacitance), unless otherwise noted.

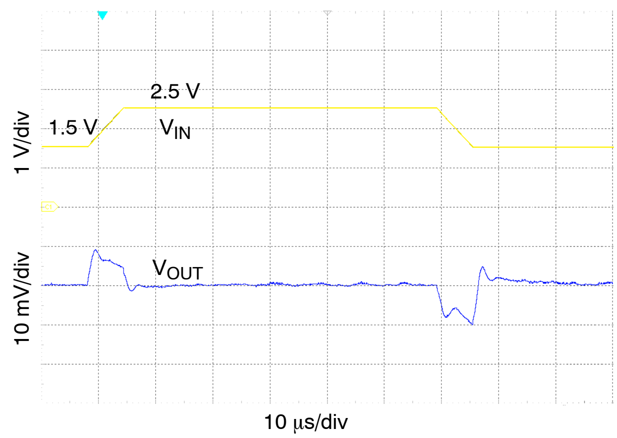


Figure 21. IN Line Transient Response, V_{IN} = 1.5 V to 2.5 V in 5 μs

APPLICATIONS INFORMATION

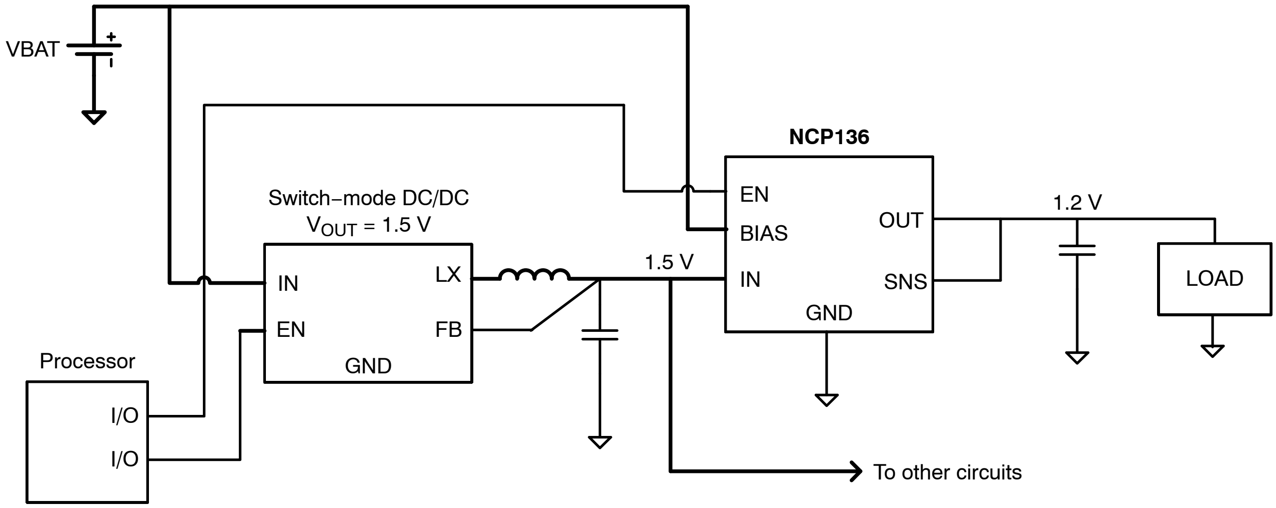


Figure 22. Typical Application: Low−Voltage DC/DC Post−Regulator with ON/OFF Functionality

The NCP136 dual−rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from V_{IN} voltage. All the low current internal control circuitry is powered from the V_{BIAS} voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. Vin to Vout operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

The NCP136 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP136 Voltage linear regulator Fixed version is available.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN} – V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough; specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} – V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The NCP136 device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 4.7 μF to 47 μF. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} = 1 μF and C_{BIAS} = 0.1 μF or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP136 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. To get the full functionality of Soft Start, it is recommended to turn on the V_{IN} and V_{BIAS} supply voltages first and activate the Enable pin no sooner than V_{IN} and V_{BIAS} are on their nominal levels. If the enable function is not to be used then the pin should be connected to V_{IN} or V_{BIAS}.

If the EN pin voltage is < 0.4 V the device is guaranteed to be disabled. The pass transistor is turned off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active (devices with Output Active Discharge feature only) so that the output voltage V_{OUT} is pulled down to GND through a 150 Ω resistor. In the disable state the device consumes as low as typ. 0.5 µA from the V_{IN} and 0.5 µA from V_{BIAS}. If the EN pin voltage > 0.9 V the device is guaranteed to be enabled. The NCP136 regulates the output voltage and the active discharge transistor is turned off. The EN pin has internal pull−down current source with typ. value of 0.3 µA which assures that the device is turned off when the EN pin is not connected.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +105°C maximum.

ORDERING INFORMATION

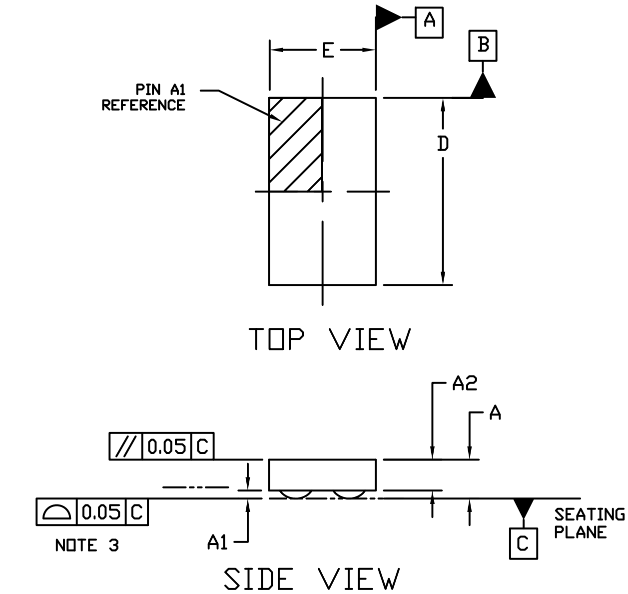
Device	Nominal Output Voltage	Marking	Option	Package	Shipping†
NCP136AFCT080T2G	0.80 V	7A	Output Active Discharge, Normal Turn−On Slew Rate	WLCSP6 Case 567XK (Pb−Free)	5000 / Tape & Reel
NCP136BFCT080T2G	0.80 V	7H	Non – Active Discharge, Normal Turn−On Slew Rate		
NCP136AFCT088T2G	0.88 V	7J	Output Active Discharge, Normal Turn−On Slew Rate		
NCP136AFCT105T2G	1.05 V	7K	Output Active Discharge, Normal Turn−On Slew Rate		
NCP136AFCT110T2G	1.10 V	7L	Output Active Discharge, Normal Turn−On Slew Rate		
NCP136AFCT120T2G	1.20 V	7E	Output Active Discharge, Normal Turn−On Slew Rate		
NCP136CFCT120T2G	1.20 V	7C	Output Active Discharge, Slow Turn−On Slew Rate		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

PACKAGE DIMENSIONS

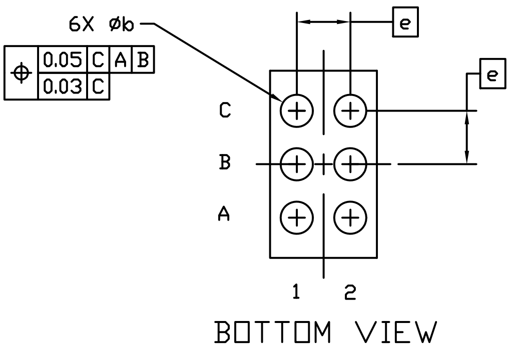
WLCSP6 1.4x0.8x0.33
CASE 567XK
ISSUE O

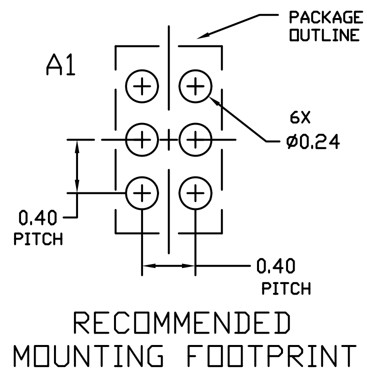


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	0.33
A1	0.040	0.060	0.080
A2	0.23 REF		
b	0.220	0.240	0.260
D	1.370	1.400	1.430
E	0.770	0.800	0.830
e	0.40 BSC		





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