

NCP185

Product Preview

LDO Regulator, 500 mA, Ultra-Low Noise, High PSRR

The NCP185 is designed to offer class leading noise performance only $1.8 \mu\text{V}_{\text{RMS}}$ and excellent dynamic performance. In combination with very low quiescent current typ. $95 \mu\text{A}$ the NCP185 is the best choice for latest generation of images sensors, wifi modules and battery powered devices. Minimum input voltage only 1.3 V allows to use the NCP185 in very wide range of applications in combination with very low dropout device improves efficiency and power dissipation.

Features

- Operating Input Voltage Range: 1.3 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.3 V
- $\pm 2\%$ Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. $95 \mu\text{A}$
- Standby Current: Typ. $0.1 \mu\text{A}$
- Very Low Dropout: 260 mV for 1.2 V at 500 mA
- Ultra High PSRR: Typ. 80 dB at 50 mA , $f = 1 \text{ kHz}$
- Ultra Low Noise: $1.8 \mu\text{V}_{\text{RMS}}$
- Stable with a $2.2 \mu\text{F}$ Small Case Size Ceramic Capacitors
- Available in – WLCSP6 $1.2 \text{ mm} \times 0.8 \text{ mm}$
– WDFNW8 $2 \text{ mm} \times 2 \text{ mm}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

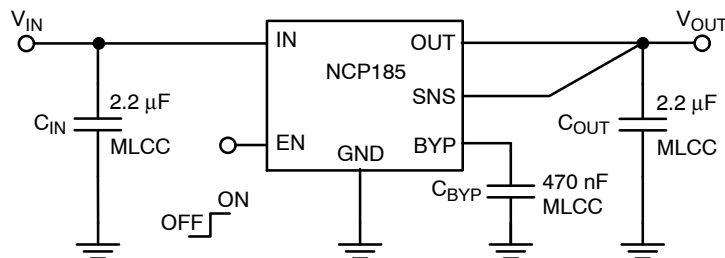


Figure 1. Typical Application Schematics

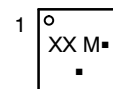
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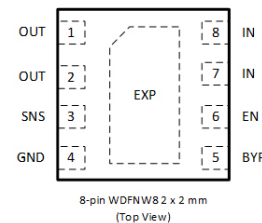
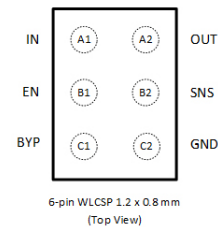
MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

NCP185

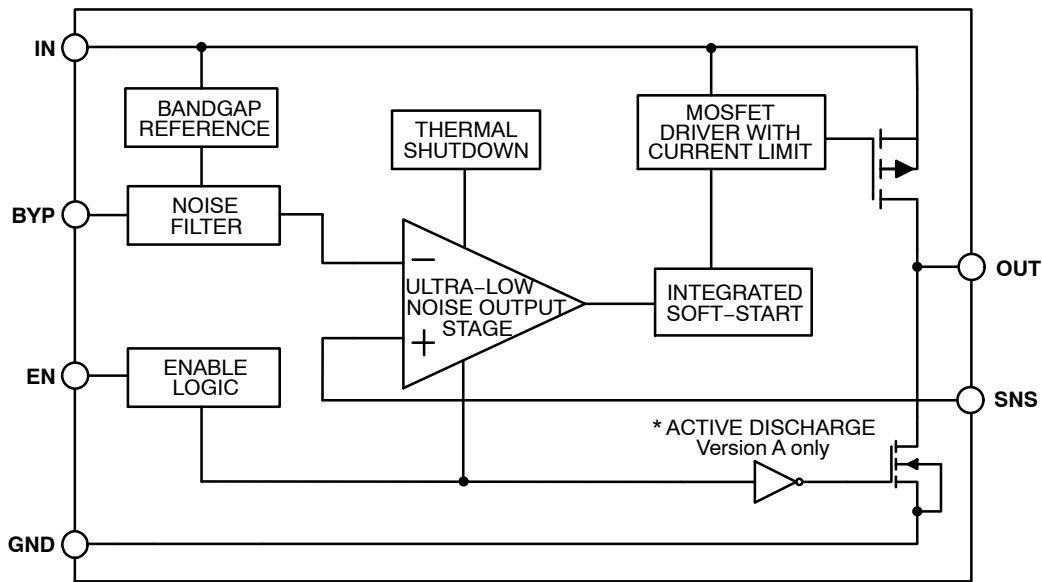


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. WLCSP6	Pin No. WDFNW8	Pin Name	Description
A1	7, 8	IN	Input voltage supply pin.
A2	1, 2	OUT	Regulated output voltage. The output should be bypassed with small 2.2 μ F ceramic capacitor.
B1	6	EN	Chip enable: Applying $V_{EN} < 0.2$ V disables the regulator, Pulling $V_{EN} > 0.7$ V enables the LDO.
B2	3	SNS	Sense pin should be connected directly to VOUT on load side to compensate PCB trace resistance and reduce voltage drop.
C1	5	BYP	The 470 nF bypass capacitor should be connected to this pin to ensure excellent noise parameter
C2	4	GND	Common ground connection
-	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	-0.3 V to 6	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} + 0.3$, max. 6 V	V
Chip Enable Input	V_{CE}	-0.3 V to 6	V
Bypass Pin	V_{BYP}	-0.3 V to 6	V
Sense Pin	V_{SNS}	-0.3 V to 6	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	$^{\circ}$ C
Storage Temperature	T_{STG}	-55 to 150	$^{\circ}$ C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

2. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per EIA/JESD22-A114

ESD Machine Model tested per EIA/JESD22-A115

ESD Charged Device Model tested per EIA/JESD22-C101, Field Induced Charge Model

Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

NCP185

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WLCSP6 (Note 3), Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	TBD	°C/W
Thermal Characteristics, WDFNW8 (Note 3), Thermal Resistance, Junction-to-Air		TBD	

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51-7

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 0.5\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 2.2\text{ }\mu\text{F}$, $C_{BYP} = 470\text{ nF}$, unless otherwise noted. $V_{EN} = 1.2\text{ V}$. Typical values are at $T_J = +25^{\circ}\text{C}$ (Note 4).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	1.3		5.5	V
Output Voltage Accuracy	$V_{IN} = (V_{OUT(NOM)} + 0.5\text{ V})$ to 5.5 V $0\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$	V_{OUT}	-2		+2	%
Line Regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	$Line_{Reg}$		0.02		%/V
Load Regulation	$I_{OUT} = 1\text{ mA}$ to 500 mA	$Load_{Reg}$		1		mV
Dropout Voltage (Note 5)	$I_{OUT} = 500\text{ mA}$ $V_{OUT(NOM)} = 1.2\text{ V}$	V_{DO}		260	TBD	mV
Output Current Limit	$V_{OUT} = 90\% V_{OUT(NOM)}$	I_{CL}	600	800		mA
Short Circuit Current	$V_{OUT} = 0\text{ V}$	I_{SC}		850		
Quiescent Current	$I_{OUT} = 0\text{ mA}$	I_Q		95	TBD	μA
Shutdown Current	$V_{EN} \leq 0.4\text{ V}$, $V_{IN} = 5.5\text{ V}$	I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage "H"	V_{ENH}	0.7			V
	EN Input Voltage "L"	V_{ENL}			0.2	
EN Pull Down Current	$V_{EN} = 5.5\text{ V}$	I_{EN}		0.2	0.5	μA
Turn-On Time	$C_{OUT} = 1\text{ }\mu\text{F}$, From assertion of V_{EN} to $V_{OUT} = 95\% V_{OUT(NOM)}$			TBD		μs
Power Supply Rejection Ratio	$I_{OUT} = 50\text{ mA}$ $f = 100\text{ Hz}$ $f = 1\text{ kHz}$ $f = 10\text{ kHz}$ $f = 100\text{ kHz}$	PSRR		91 92 85 60		dB
Output Voltage Noise	$f = 10\text{ Hz}$ to 100 kHz $I_{OUT} = 50\text{ mA}$	V_N		1.8		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising	T_{SDH}		160		°C
	Temperature falling	T_{SDL}		140		°C
Active Output Discharge Resistance	$V_{EN} < 0.4\text{ V}$, Version A only	R_{DIS}		280		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25^{\circ}\text{C}$.

Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

5. Dropout voltage is characterized when V_{OUT} falls 20 mV below $V_{OUT(NOM)}$.

DEVICE ORDERING INFORMATION

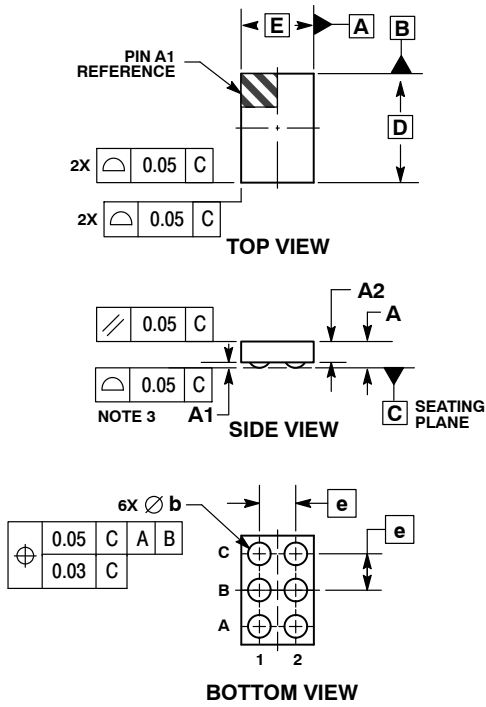
Device	Marking	Package	Shipping†
NCP185	TBD	WLCSP6 (Pb-Free)	TBD / Tape & Reel
NCP185	TBD	WDFNW8 (Pb-Free)	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP185

PACKAGE DIMENSIONS

WLCSP6, 1.20x0.80
CASE 567MV
ISSUE B

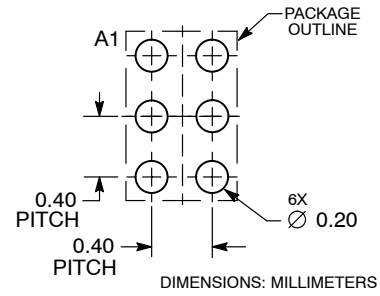


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.33
A1	0.04	0.08
A2	0.23 REF	
b	0.24	0.30
D	1.20 BSC	
E	0.80 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

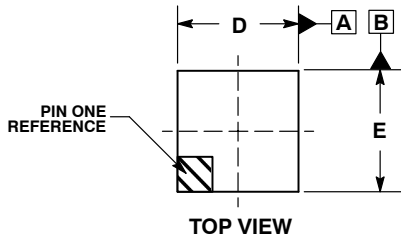


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

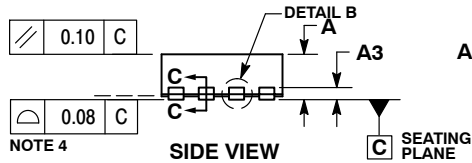
NCP185

PACKAGE DIMENSIONS

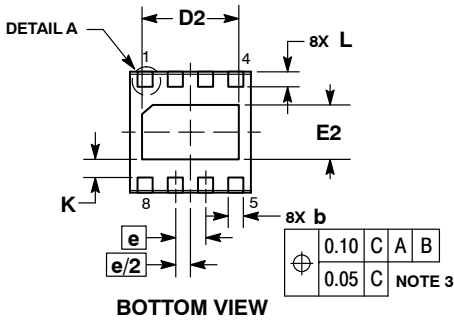
WDFNW8 2x2, 0.5P CASE 511CL ISSUE O



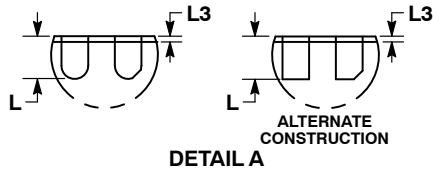
TOP VIEW



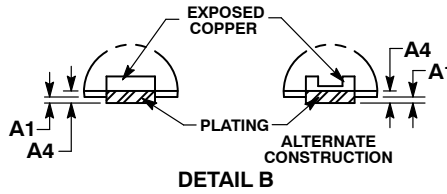
SIDE VIEW



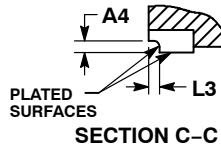
BOTTOM VIEW



DETAIL A



DETAIL B



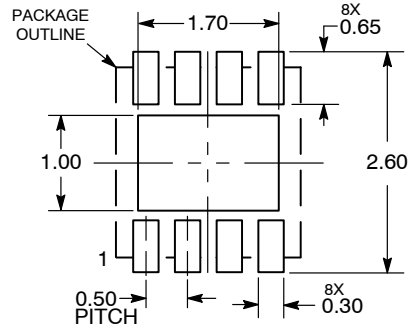
SECTION C-C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20 REF		
A4	0.05	0.10	0.15
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.50 BSC		
K	0.25	---	---
L	0.20	0.30	0.40
L3	0.00	0.05	0.10

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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