NCP3285, NCP3285A

Product Preview

Single-Phase Voltage Regulator with SVID

High Efficiency, Integrated Power MOSFETs

The NCP3285/A, a single−phase synchronous buck regulator with SVID, integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution. The NCP3285/A is able to deliver up to 20 A / 30 A TDC output current on a wide output voltage range. Operating in high switching frequency up to 1 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. It provides differential voltage sense and comprehensive protections.

Features

- Vin = 4.5 V ~ 18 V
- Vout = 0.5 V ~ 2.0 V to Support Intel VR13 and VR13.HC SVID
- Integrated Power MOSFETs
- Up to 20 A (NCP3285) / 30 A (NCP3285A) Continuous Output Current and 30 A (NCP3285) / 45 A (NCP3285A) Pulse Current
- Integrated 5 V LDO or External 5 V Supply
- Enable with Programmable Vin UVLO
- 600 k / 800 k / 1000 kHz Switching Frequency
- Selectable Forced CCM and Auto DCM/CCM
- 16 Selectable Boot Voltages
- 16 Selectable SVID Addresses
- Output Discharge in Shutdown
- Programmable Current Limit
- Latch−Off Over−Voltage and Under−Voltage Protection
- Recoverable Thermal Shutdown Protection
- PQFN37, 5 x 6 mm, 0.5 mm Pitch Package
- This is a Pb−Free Device

Typical Applications

- Point of Load
- Computing Applications
- Telecom and Networking
- Server and Storage System

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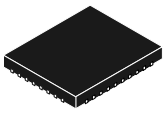
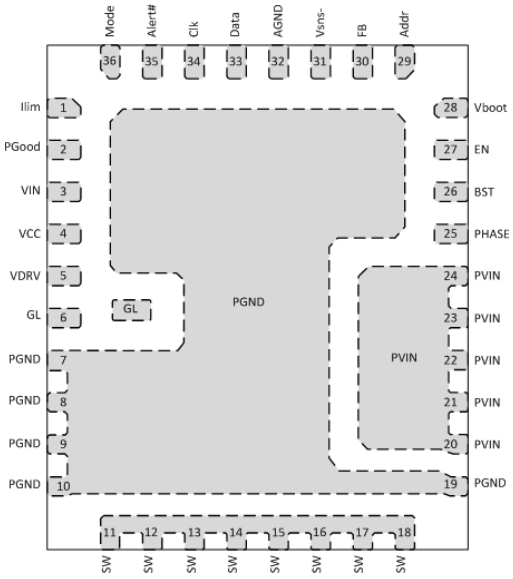


PQFN37 5x6, 0.5P
CASE 483BZ

MARKING DIAGRAM

A = Assembly Site
WL = Wafer Lot Number
Y = Year of Production
WW = Work Week Number
G = Pb−Free Designator

PINOUT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3285MNTXG	PQFN37 (Pb−Free)	2500 / Tape & Reel
NCP3285AMNTXG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

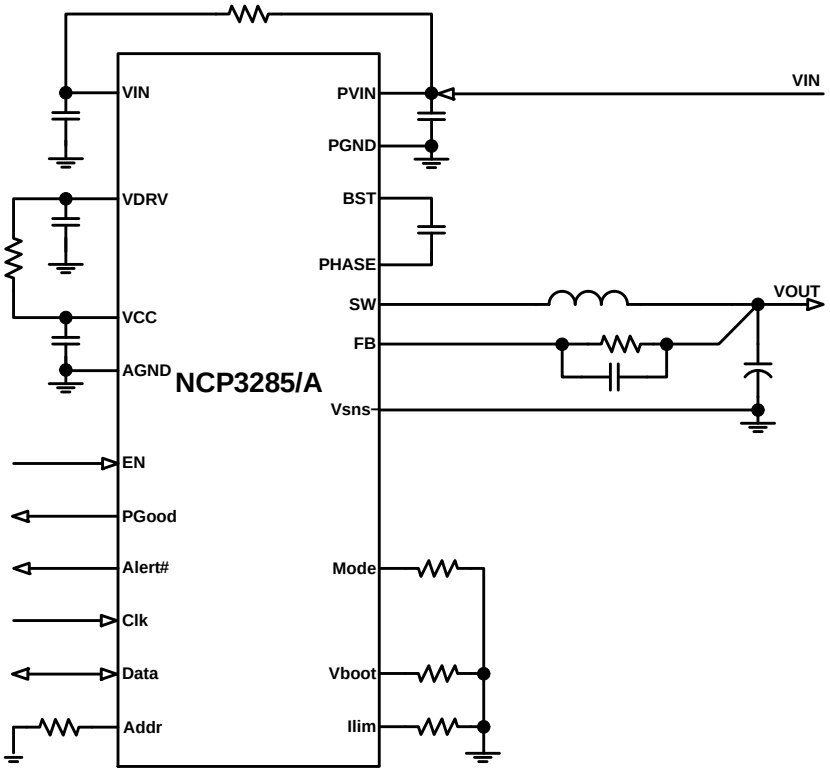


Figure 1. Typical Application Circuit with Single Input Power Supply (LDO Enabled)

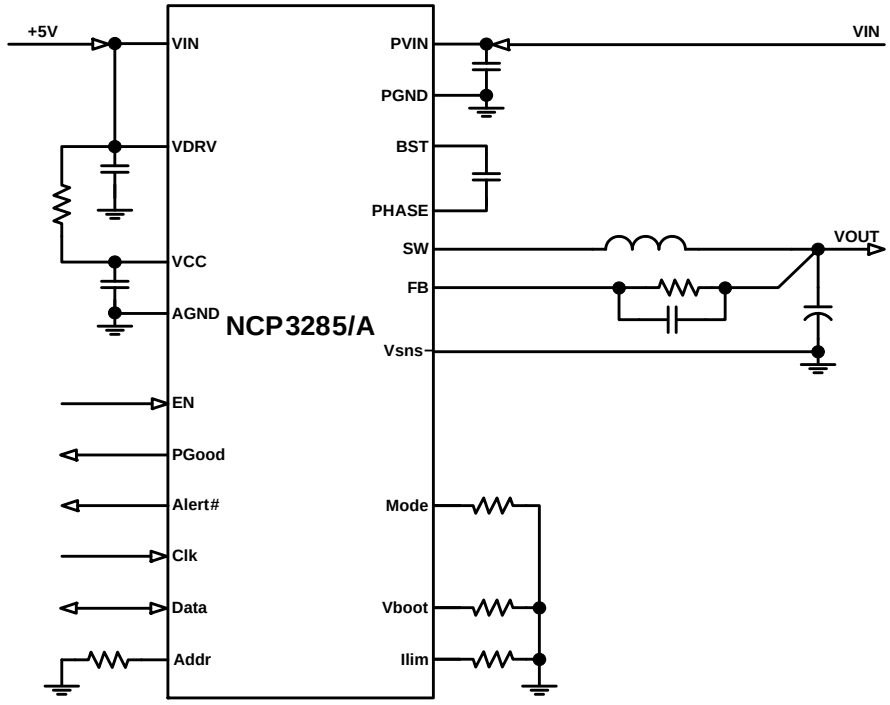


Figure 2. Typical Application Circuit with External 5 V Supply for VCC (LDO Disabled)

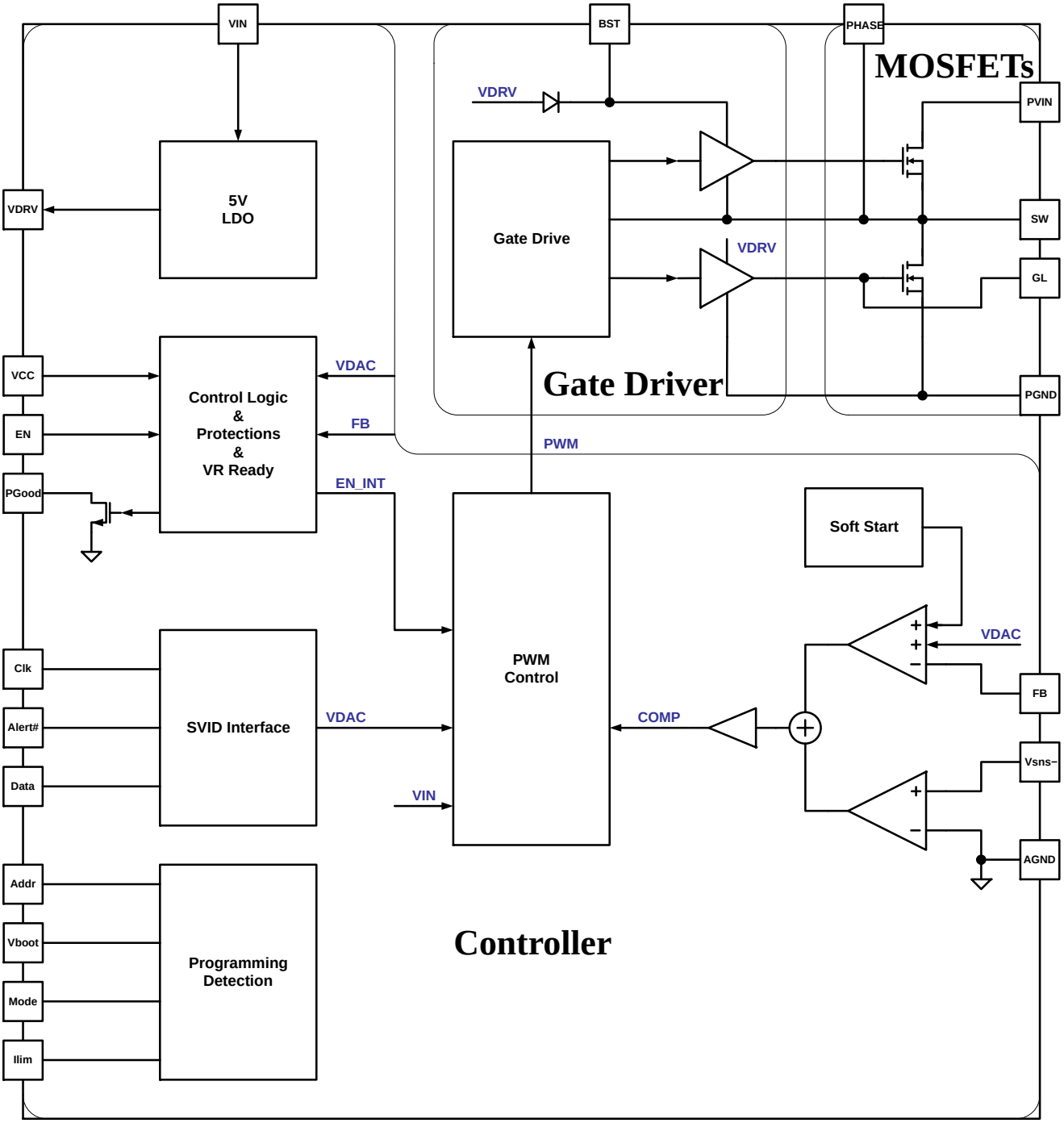


Figure 3. Functional Block Diagram

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	Ilim	Analog Output	**Current Limit.** A resistor between this pin and AGND to program current limit.
2	PGood	Logic Output	**Power GOOD.** Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
3	VIN	Power Input	**Power Supply Input of LDO.** Power supply input pin of internal 5 V LDO. A 1.0 μF or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to this pin. A direct short from this pin to VDRV (pin 5) disables the internal LDO for applications with an external 5 V supply as power of VDRV and VCC.
4	VCC	Analog Power	**Supply Voltage Input of Controller.** A 2.2 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
5	VDRV	Analog Power	**Output of LDO and Supply Voltage Input of Gate Drivers.** Output of integrated 5.0 V LDO and power supply input pin of gate drivers. A 4.7 μF / 25 V or larger ceramic capacitor bypasses this input to PGND. This capacitor should be placed as close as possible to this pin.
6	GL	Analog Output	**Gate of Low−Side MOSFET.** Directly connected with the gate of the low−side power MOSFET.
7~10,19	PGND	Power Ground	**Power Ground.** These pins are the power supply ground pins of the device, which are connected to source of internal low−side power MOSFET. Must be connected to the system ground.
11~18	SW	Power Bidirectional	**Switch Node.** Pins to be connected to an external inductor. These pins are interconnection between internal high−side MOSFET and low−side MOSFET.
20~24	PVIN	Power Input	**Power Supply Input.** These pins are the power supply input pins of the device, which are connected to drain of internal high−side power MOSFET. A 22 μF or more ceramic capacitors must bypass this input to PGND. The capacitors should be placed as close as possible to these pins.
25	PHASE	Power Return	**Phase Node.** Provides a return path for integrated high−side gate driver. It is internally connected to source of high−side MOSFET.
26	BST	Power Bidirectional	**Bootstrap.** Provides bootstrap voltage for high−side gate driver. A 0.22 μF / 25 V ceramic capacitor is required from this pin to PHASE (pin 25).
27	EN	Logic Input	**Enable.** Logic high enables controller while logic low disables controller. Input supply UVLO can be programmed at this pin.
28	Vboot	Analog Input	**Boot−Up Voltage.** A resistor from this pin to ground programs boot−up voltage.
29	Addr	Analog Input	**SVID Address.** A resistor from this pin to ground programs SVID address.
30	FB	Analog Input	**Feedback.** Inverting input to error amplifier.
31	Vsns−	Analog Input	**Voltage Sense Negative Input.** Connect this pin to remote voltage negative sense point.
32	AGND	Analog Ground	**Analog Ground.** Ground of controller. Must be connected to the system ground.
33	Data	Logic Bidirectional	**Serial Data IO Port.** Data port of SVID interface.
34	Clk	Logic Input	**Serial Clock.** Clock input of SVID interface.
35	Alert#	Logic Output	**ALERT#.** Open−drain output. Provides a logic low valid alert signal of SVID interface.
36	Mode	Analog Input	**Mode.** A resistor between this pin and AGND to program operation mode, nominal switching frequency, and options.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage to PGND	V_{PVIN}, V_{VIN}		23	V
PHASE/SW to PGND	V_{PHASE}, V_{SW}	−0.6 −5 (<50 ns)	23 25 (<10 ns)	V
Driver Supply Voltage to PGND	VDRV	−0.3	5.5	V
Analog Supply Voltage to AGND	VCC	−0.3	6.5	V
BST to PGND	BST_PGND	−0.3	30 33 (<50 ns)	V
BST to PHASE/SW	BST_PHASE/SW	−0.3	6.5	V
GL to PGND	GL	−0.3 −2 (<200 ns)	VDRV+0.3	V
Vsns- to AGND	Vsns−	−0.2	0.2	V
PGND to AGND	PGND	−0.3	0.3	V
Other Pins		−0.3	VCC+0.3	V
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM		2000	V
Charge Device Model (CDM) ESD Rating are (Note 1)	ESD CDM		2000	V
Latch up Current: (Note 2)	I_{LU}	−100	100	mA
Operating Junction Temperature Range	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction to Top Case(Note 3)	$R_{\Psi JC}$	1.0 (NCP3285) 0.8 (NCP3285A)		°C/W
Thermal Resistance Junction to Board (Note 3)	$R_{\Psi JB}$	1.2 (NCP3285) 0.9 (NCP3285A)		°C/W
Thermal Resistance Junction to Ambient (Note 3)	$R_{\theta JA}$	27.0 (NCP3285) 26.7 (NCP3285A)		°C/W
Maximum Power Dissipation (Note 4)	P_D	3.70 (NCP3285) 3.75 (NCP3285A)		W
Moisture Sensitivity Level (Note 5)	MSL	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4−layer FR−4 PCB board, which has two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)
4. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on T_{JMAX} = 125°C and T_A = 25°C.
5. Moisture Sensitivity Level (MSL): IPC/JEDEC standard: J−STD−020A.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 125°C. unless other noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Units
SUPPLY VOLTAGE MONITOR						
VCC Under−Voltage (UVLO) Threshold	VCC falling	V_{DDUV-}	4.0			V
VCC OK Threshold	VCC rising	V_{DDOK}			4.4	V
VCC UVLO Hysteresis		V_{DDHYS}		200		mV
SUPPLY CURRENT						
PVIN Shutdown Current	EN low	I_{SDPVIN}	−	0.062	6	μA
VIN Quiescent Supply Current (VCC Current Included)	EN high, no switching, LDO enabled, VIN=18V, VCC=VDRV	I_{QVIN}	−	11	18	mA
	EN high, no switching, LDO disabled, VIN=VDRV=VCC=4.5V		−	11	18	
VIN Shutdown Current (VCC Current Included)	EN low, LDO enabled, VIN=18V, VCC=VDRV	I_{SDVIN}	−	27	45	μA
	EN low, LDO disabled, VIN=VDRV=VCC=4.5V		−	60	100	
5 V LINEAR REGULATOR						
Output Voltage	6V < VIN < 18V, IDRV = 0 to 30mA (External) EN high, no Switching	V_{DRV}	4.8	5.0	5.3	V
Dropout Voltage	VIN = 5V, IDRV = 50mA (External), EN high, no Switching	V_{DO}			250	mV
PWM MODULATION						
Minimum On Time	(Note 6)	T_{on_min}		50		ns
Minimum Off Time	(Note 6)	T_{off_min}		200		ns
REGULATION ACCURACY						
System Voltage Accuracy	5 mV VID Step Mode	1.0V ≤ DAC ≤ 1.52V		−0.5%• DAC	0.5%• DAC	V
		0.8V ≤ DAC ≤ 0.995V		−5m	+5m	
		0.25V ≤ DAC ≤ 0.795V		−8m	+8m	
	10 mV VID Step Mode	1.5V ≤ DAC ≤ 2.0V		−0.5%• DAC	0.5%• DAC	
		1.0V ≤ DAC ≤ 1.49V		−8m	+8m	
		0.5V ≤ DAC ≤ 0.99V		−10m	+10m	
DVID						
Fast Slew Rate	Programmed at Mode Pin	FSR		10		mV/μs
				20		
Slow Slew Rate		SSR	FSR/2 FSR/4 (default) FSR/8 FSR/16			mV/μs
VOLTAGE ERROR AMPLIFIER						
FB Bias Current	V_{FB} = 1.0 V	I_{FB}	−50		50	nA
CURRENT−SENSE AMPLIFIER						
Closed−Loop DC Gain		$GAIN_{CA}$		−12.2		V/V
−3 dB Gain Bandwidth	(Note 6)	BW_{CA}		10		MHz
Input Offset Voltage	$V_{osCS} = V_{SW} - V_{PGND}$ (Note 6)	V_{osCS}	−500	−	500	μV

6. Guaranteed by design, not tested in production.

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Units
ENABLE						
EN ON Threshold		V_{EN_TH}	0.69	0.79	0.88	V
Hysteresis Resistance		R_{HYS}		40		kΩ
Hysteresis Current		I_{EN_HYS}		5		μA
EN Input Leakage Current	EN = 0V	I_{EN_LK}			1.0	μA
SWITCHING FREQUENCY						
Switching Frequency in CCM	Programmed at Mode Pin (Note 6)	F_{SW}		1000		kHz
				800		
				600		
Source Current from Mode Pin		I_{FSET}	48.5	50	51.5	μA
SOFT START						
System Reset Time	Measured from EN to start of soft start	T_{RST}	0.8	0.93	1.1	ms
Soft Start Slew Rate		SSSR		FSR/4		mV/μs
PGOOD						
PGOOD Startup Delay	Measured from end of Soft Start to PGOOD assertion	T_{d_PGOOD}			6	μs
PGOOD Shutdown Delay	Measured from EN to PGOOD de−assertion			5		μs
PGOOD Low Voltage	I_{PGOOD}= −4 mA	V_{IPGOOD}			0.3	V
PGOOD Leakage Current	PGOOD = 5 V	$I_{lkgPGOOD}$			1.0	μA
PROTECTIONS						
Valley Current Limit Threshold	$T_A = T_J$ = 25°C, R_{LIM} = 47.5 kΩ	I_{LMT_Valley}		45		A
	R_{LIM} = 42.2 kΩ			40		
	R_{LIM} = 36.5 kΩ			35		
	R_{LIM} = 31.6 kΩ			30		
	R_{LIM} = 26.1 kΩ			25		
	R_{LIM} = 21.0 kΩ			20		
	R_{LIM} = 15.4 kΩ			15		
	R_{LIM} = 10.2 kΩ			10		
	R_{LIM} = 5.23 kΩ			5		
Fast Under Voltage Protection (FUVP) Threshold	FB to AGND		0.15	0.2	0.25	V
Fast Under Voltage Protection (FUVP) Delay	(Note 6)			1.0		us
Slow Under Voltage Protection (SUVP) Threshold	COMP to AGND (Note 6)			3.0		V
Slow Under Voltage Protection (SUVP) Delay	(Note 6)			50		us
Absolute Over Voltage Threshold During Soft−Start	FB to AGND		1.92	2.0	2.08	V
Absolute Over Voltage Threshold Hysteresis	(Note 6)			−25		mV
Over Voltage Threshold Above DAC	FB rising	V_{OVTH}	165	200	225	mV

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Units
PROTECTIONS						
Over Voltage Protection Hysteresis	FB falling (Note 6)	V_{OVHYS}		−25		mV
Over Voltage Debounce Time	FB rising to GL high (Note 6)			1.0		us
Thermal Shutdown (TSD) Threshold	(Note 6)	T_{sd}	140	150		°C
Recovery Temperature Threshold	(Note 6)	T_{rec}		125		°C
Thermal Shutdown (TSD) Debounce Time	(Note 6)			125		ns
TEMPERATURE TELEMETRY						
Temperature Telemetry Tolerance	$T_A = T_J$ = 90~120°C (Note 6)		−4.0		+4.0	°C
VBOOT						
Sensing Current			9.7	10	10.3	μA
ADDRESS						
Sensing Current			9.7	10	10.3	μA
IMAX						
Sensing Current			12.125	12.5	12.875	μA
CLK, DATA						
Input High Voltage		V_{IH}	0.65			V
Input Low Voltage		V_{IL}			0.45	V
Input Threshold Hysteresis		V_{HYS}		85		mV
Buffer On Resistance (Data)		R_{ON}	4		13	Ω
Input Leakage Current	Pin voltage between 0 and 1.05 V		−1		1	μA
Input Capacitance	(Note 6)				4.0	pF
VR Clock to Data Delay	Time between Clk rising edge and valid Data level (Note 6)	Tco	4		12	ns
Setup Time	Time before Clk falling (sampling) edge that Data level must be valid (Note 6)	Tsu	7			ns
Hold Time	Time after Clk falling edge that the Data level remains valid (Note 6)	Thld	14			ns
ALERT#						
Output On Resistance		R_{ON}	4		13	Ω
Output Leakage Current	High Impedance State, ALERT # = 3.3 V		−1.0	−	1.0	μA
ADC						
Voltage Range	(Note 6)		0		2.0	V
Total Unadjusted Error (TUE)	(Note 6)		−1		1	%
Differential Nonlinearity (DNL)	8−bit (Note 6)				1	LSB
Power Supply Sensitivity	(Note 6)			±1		%
Conversion Time	(Note 6)			30		μs
Round Robin	(Note 6)			90		μs

6. Guaranteed by design, not tested in production.

Table 4. VR13 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V) 5 mV Mode	Voltage(V) 10 mV Mode	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V) 5 mV Mode	Voltage(V) 10 mV Mode	HEX
0	0	0	0	0	0	0	0	0.000	0.000	00	0	0	1	1	0	0	0	0	0.485	0.970	30
0	0	0	0	0	0	0	1	0.250	0.500	01	0	0	1	1	0	0	0	1	0.490	0.980	31
0	0	0	0	0	0	1	0	0.255	0.510	02	0	0	1	1	0	0	1	0	0.495	0.990	32
0	0	0	0	0	0	1	1	0.260	0.520	03	0	0	1	1	0	0	1	1	0.500	1.000	33
0	0	0	0	0	1	0	0	0.265	0.530	04	0	0	1	1	0	1	0	0	0.505	1.010	34
0	0	0	0	0	1	0	1	0.270	0.540	05	0	0	1	1	0	1	0	1	0.510	1.020	35
0	0	0	0	0	1	1	0	0.275	0.550	06	0	0	1	1	0	1	1	0	0.515	1.030	36
0	0	0	0	0	1	1	1	0.280	0.560	07	0	0	1	1	0	1	1	1	0.520	1.040	37
0	0	0	0	1	0	0	0	0.285	0.570	08	0	0	1	1	1	0	0	0	0.525	1.050	38
0	0	0	0	1	0	0	1	0.290	0.580	09	0	0	1	1	1	0	0	1	0.530	1.060	39
0	0	0	0	1	0	1	0	0.295	0.590	0A	0	0	1	1	1	0	1	0	0.535	1.070	3A
0	0	0	0	1	0	1	1	0.300	0.600	0B	0	0	1	1	1	0	1	1	0.540	1.080	3B
0	0	0	0	1	1	0	0	0.305	0.610	0C	0	0	1	1	1	1	0	0	0.545	1.090	3C
0	0	0	0	1	1	0	1	0.310	0.620	0D	0	0	1	1	1	1	0	1	0.550	1.100	3D
0	0	0	0	1	1	1	0	0.315	0.630	0E	0	0	1	1	1	1	1	0	0.555	1.110	3E
0	0	0	0	1	1	1	1	0.320	0.640	0F	0	0	1	1	1	1	1	1	0.560	1.120	3F
0	0	0	1	0	0	0	0	0.325	0.650	10	0	1	0	0	0	0	0	0	0.565	1.130	40
0	0	0	1	0	0	0	1	0.330	0.660	11	0	1	0	0	0	0	0	1	0.570	1.140	41
0	0	0	1	0	0	1	0	0.335	0.670	12	0	1	0	0	0	0	1	0	0.575	1.150	42
0	0	0	1	0	0	1	1	0.340	0.680	13	0	1	0	0	0	0	1	1	0.580	1.160	43
0	0	0	1	0	1	0	0	0.345	0.690	14	0	1	0	0	0	1	0	0	0.585	1.170	44
0	0	0	1	0	1	0	1	0.350	0.700	15	0	1	0	0	0	1	0	1	0.590	1.180	45
0	0	0	1	0	1	1	0	0.355	0.710	16	0	1	0	0	0	1	1	0	0.595	1.190	46
0	0	0	1	0	1	1	1	0.360	0.720	17	0	1	0	0	0	1	1	1	0.600	1.200	47
0	0	0	1	1	0	0	0	0.365	0.730	18	0	1	0	0	1	0	0	0	0.605	1.210	48
0	0	0	1	1	0	0	1	0.370	0.740	19	0	1	0	0	1	0	0	1	0.610	1.220	49
0	0	0	1	1	0	1	0	0.375	0.750	1A	0	1	0	0	1	0	1	0	0.615	1.230	4A
0	0	0	1	1	0	1	1	0.380	0.760	1B	0	1	0	0	1	0	1	1	0.620	1.240	4B
0	0	0	1	1	1	0	0	0.385	0.770	1C	0	1	0	0	1	1	0	0	0.625	1.250	4C
0	0	0	1	1	1	0	1	0.390	0.780	1D	0	1	0	0	1	1	0	1	0.630	1.260	4D
0	0	0	1	1	1	1	0	0.395	0.790	1E	0	1	0	0	1	1	1	0	0.635	1.270	4E
0	0	0	1	1	1	1	1	0.400	0.800	1F	0	1	0	0	1	1	1	1	0.640	1.280	4F
0	0	1	0	0	0	0	0	0.405	0.810	20	0	1	0	1	0	0	0	0	0.645	1.290	50
0	0	1	0	0	0	0	1	0.410	0.820	21	0	1	0	1	0	0	0	1	0.650	1.300	51
0	0	1	0	0	0	1	0	0.415	0.830	22	0	1	0	1	0	0	1	0	0.655	1.310	52
0	0	1	0	0	0	1	1	0.420	0.840	23	0	1	0	1	0	0	1	1	0.660	1.320	53
0	0	1	0	0	1	0	0	0.425	0.850	24	0	1	0	1	0	1	0	0	0.665	1.330	54
0	0	1	0	0	1	0	1	0.430	0.860	25	0	1	0	1	0	1	0	1	0.670	1.340	55
0	0	1	0	0	1	1	0	0.435	0.870	26	0	1	0	1	0	1	1	0	0.675	1.350	56
0	0	1	0	0	1	1	1	0.440	0.880	27	0	1	0	1	0	1	1	1	0.680	1.360	57
0	0	1	0	1	0	0	0	0.445	0.890	28	0	1	0	1	1	0	0	0	0.685	1.370	58
0	0	1	0	1	0	0	1	0.450	0.900	29	0	1	0	1	1	0	0	1	0.690	1.380	59
0	0	1	0	1	0	1	0	0.455	0.910	2A	0	1	0	1	1	0	1	0	0.695	1.390	5A
0	0	1	0	1	0	1	1	0.460	0.920	2B	0	1	0	1	1	0	1	1	0.700	1.400	5B
0	0	1	0	1	1	0	0	0.465	0.930	2C	0	1	0	1	1	1	0	0	0.705	1.410	5C
0	0	1	0	1	1	0	1	0.470	0.940	2D	0	1	0	1	1	1	0	1	0.710	1.420	5D
0	0	1	0	1	1	1	0	0.475	0.950	2E	0	1	0	1	1	1	1	0	0.715	1.430	5E
0	0	1	0	1	1	1	1	0.480	0.960	2F	0	1	0	1	1	1	1	1	0.720	1.440	5F

Table 4. VR13 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V) 5 mV Mode	Voltage(V) 10 mV Mode	HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V) 5 mV Mode	Voltage(V) 10 mV Mode	HEX
0	1	1	0	0	0	0	0	0.725	1.450	60	1	0	0	1	0	0	0	0	0.965	1.930	90
0	1	1	0	0	0	0	1	0.730	1.460	61	1	0	0	1	0	0	0	1	0.970	1.940	91
0	1	1	0	0	0	1	0	0.735	1.470	62	1	0	0	1	0	0	1	0	0.975	1.950	92
0	1	1	0	0	0	1	1	0.740	1.480	63	1	0	0	1	0	0	1	1	0.980	1.960	93
0	1	1	0	0	1	0	0	0.745	1.490	64	1	0	0	1	0	1	0	0	0.985	1.970	94
0	1	1	0	0	1	0	1	0.750	1.500	65	1	0	0	1	0	1	0	1	0.990	1.980	95
0	1	1	0	0	1	1	0	0.755	1.510	66	1	0	0	1	0	1	1	0	0.995	1.990	96
0	1	1	0	0	1	1	1	0.760	1.520	67	1	0	0	1	0	1	1	1	1.000	2.000	97
0	1	1	0	1	0	0	0	0.765	1.530	68	1	0	0	1	1	0	0	0	1.005	2.010	98
0	1	1	0	1	0	0	1	0.770	1.540	69	1	0	0	1	1	0	0	1	1.010	2.020	99
0	1	1	0	1	0	1	0	0.775	1.550	6A	1	0	0	1	1	0	1	0	1.015	2.030	9A
0	1	1	0	1	0	1	1	0.780	1.560	6B	1	0	0	1	1	0	1	1	1.020	2.040	9B
0	1	1	0	1	1	0	0	0.785	1.570	6C	1	0	0	1	1	1	0	0	1.025	2.050	9C
0	1	1	0	1	1	0	1	0.790	1.580	6D	1	0	0	1	1	1	0	1	1.030	2.060	9D
0	1	1	0	1	1	1	0	0.795	1.590	6E	1	0	0	1	1	1	1	0	1.035	2.070	9E
0	1	1	0	1	1	1	1	0.800	1.600	6F	1	0	0	1	1	1	1	1	1.040	2.080	9F
0	1	1	1	0	0	0	0	0.805	1.610	70	1	0	1	0	0	0	0	0	1.045	2.090	A0
0	1	1	1	0	0	0	1	0.810	1.620	71	1	0	1	0	0	0	0	1	1.050	2.100	A1
0	1	1	1	0	0	1	0	0.815	1.630	72	1	0	1	0	0	0	1	0	1.055	2.110	A2
0	1	1	1	0	0	1	1	0.820	1.640	73	1	0	1	0	0	0	1	1	1.060	2.120	A3
0	1	1	1	0	1	0	0	0.825	1.650	74	1	0	1	0	0	1	0	0	1.065	2.130	A4
0	1	1	1	0	1	0	1	0.830	1.660	75	1	0	1	0	0	1	0	1	1.070	2.140	A5
0	1	1	1	0	1	1	0	0.835	1.670	76	1	0	1	0	0	1	1	0	1.075	2.150	A6
0	1	1	1	0	1	1	1	0.840	1.680	77	1	0	1	0	0	1	1	1	1.080	2.160	A7
0	1	1	1	1	0	0	0	0.845	1.690	78	1	0	1	0	1	0	0	0	1.085	2.170	A8
0	1	1	1	1	0	0	1	0.850	1.700	79	1	0	1	0	1	0	0	1	1.090	2.180	A9
0	1	1	1	1	0	1	0	0.855	1.710	7A	1	0	1	0	1	0	1	0	1.095	2.190	AA
0	1	1	1	1	0	1	1	0.860	1.720	7B	1	0	1	0	1	0	1	1	1.100	2.200	AB
0	1	1	1	1	1	0	0	0.865	1.730	7C	1	0	1	0	1	1	0	0	1.105	2.210	AC
0	1	1	1	1	1	0	1	0.870	1.740	7D	1	0	1	0	1	1	0	1	1.110	2.220	AD
0	1	1	1	1	1	1	0	0.875	1.750	7E	1	0	1	0	1	1	1	0	1.115	2.230	AE
0	1	1	1	1	1	1	1	0.880	1.760	7F	1	0	1	0	1	1	1	1	1.120	2.240	AF
1	0	0	0	0	0	0	0	0.885	1.770	80	1	0	1	1	0	0	0	0	1.125	2.250	B0
1	0	0	0	0	0	0	1	0.890	1.780	81	1	0	1	1	0	0	0	1	1.130	2.260	B1
1	0	0	0	0	0	1	0	0.895	1.790	82	1	0	1	1	0	0	1	0	1.135	2.270	B2
1	0	0	0	0	0	1	1	0.900	1.800	83	1	0	1	1	0	0	1	1	1.140	2.280	B3
1	0	0	0	0	1	0	0	0.905	1.810	84	1	0	1	1	0	1	0	0	1.145	2.290	B4
1	0	0	0	0	1	0	1	0.910	1.820	85	1	0	1	1	0	1	0	1	1.150	2.300	B5
1	0	0	0	0	1	1	0	0.915	1.830	86	1	0	1	1	0	1	1	0	1.155	2.310	B6
1	0	0	0	0	1	1	1	0.920	1.840	87	1	0	1	1	0	1	1	1	1.160	2.320	B7
1	0	0	0	1	0	0	0	0.925	1.850	88	1	0	1	1	1	0	0	0	1.165	2.330	B8
1	0	0	0	1	0	0	1	0.930	1.860	89	1	0	1	1	1	0	0	1	1.170	2.340	B9
1	0	0	0	1	0	1	0	0.935	1.870	8A	1	0	1	1	1	0	1	0	1.175	2.350	BA
1	0	0	0	1	0	1	1	0.940	1.880	8B	1	0	1	1	1	0	1	1	1.180	2.360	BB
1	0	0	0	1	1	0	0	0.945	1.890	8C	1	0	1	1	1	1	0	0	1.185	2.370	BC
1	0	0	0	1	1	0	1	0.950	1.900	8D	1	0	1	1	1	1	0	1	1.190	2.380	BD
1	0	0	0	1	1	1	0	0.955	1.910	8E	1	0	1	1	1	1	1	0	1.195	2.390	BE
1	0	0	0	1	1	1	1	0.960	1.920	8F	1	0	1	1	1	1	1	1	1.200	2.400	BF

Table 4. VR13 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V)		HEX	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage(V)		HEX
								5 mV Mode	10 mV Mode										5 mV Mode	10 mV Mode	
1	1	0	0	0	0	0	0	1.205	2.410	C0	1	1	1	1	0	0	0	0	1.445	2.890	F0
1	1	0	0	0	0	0	1	1.210	2.420	C1	1	1	1	1	0	0	0	1	1.450	2.900	F1
1	1	0	0	0	0	1	0	1.215	2.430	C2	1	1	1	1	0	0	1	0	1.455	2.910	F2
1	1	0	0	0	0	1	1	1.220	2.440	C3	1	1	1	1	0	0	1	1	1.460	2.920	F3
1	1	0	0	0	1	0	0	1.225	2.450	C4	1	1	1	1	0	1	0	0	1.465	2.930	F4
1	1	0	0	0	1	0	1	1.230	2.460	C5	1	1	1	1	0	1	0	1	1.470	2.940	F5
1	1	0	0	0	1	1	0	1.235	2.470	C6	1	1	1	1	0	1	1	0	1.475	2.950	F6
1	1	0	0	0	1	1	1	1.240	2.480	C7	1	1	1	1	0	1	1	1	1.480	2.960	F7
1	1	0	0	1	0	0	0	1.245	2.490	C8	1	1	1	1	1	0	0	0	1.485	2.970	F8
1	1	0	0	1	0	0	1	1.250	2.500	C9	1	1	1	1	1	0	0	1	1.490	2.980	F9
1	1	0	0	1	0	1	0	1.255	2.510	CA	1	1	1	1	1	0	1	0	1.495	2.990	FA
1	1	0	0	1	0	1	1	1.260	2.520	CB	1	1	1	1	1	0	1	1	1.500	3.000	FB
1	1	0	0	1	1	0	0	1.265	2.530	CC	1	1	1	1	1	1	0	0	1.505	3.010	FC
1	1	0	0	1	1	0	1	1.270	2.540	CD	1	1	1	1	1	1	0	1	1.510	3.020	FD
1	1	0	0	1	1	1	0	1.275	2.550	CE	1	1	1	1	1	1	1	0	1.515	3.030	FE
1	1	0	0	1	1	1	1	1.280	2.560	CF	1	1	1	1	1	1	1	1	1.520	3.040	FF
1	1	0	1	0	0	0	0	1.285	2.570	D0											
1	1	0	1	0	0	0	1	1.290	2.580	D1											
1	1	0	1	0	0	1	0	1.295	2.590	D2											
1	1	0	1	0	0	1	1	1.300	2.600	D3											
1	1	0	1	0	1	0	0	1.305	2.610	D4											
1	1	0	1	0	1	0	1	1.310	2.620	D5											
1	1	0	1	0	1	1	0	1.315	2.630	D6											
1	1	0	1	0	1	1	1	1.320	2.640	D7											
1	1	0	1	1	0	0	0	1.325	2.650	D8											
1	1	0	1	1	0	0	1	1.330	2.660	D9											
1	1	0	1	1	0	1	0	1.335	2.670	DA											
1	1	0	1	1	0	1	1	1.340	2.680	DB											
1	1	0	1	1	1	0	0	1.345	2.690	DC											
1	1	0	1	1	1	0	1	1.350	2.700	DD											
1	1	0	1	1	1	1	0	1.355	2.710	DE											
1	1	0	1	1	1	1	1	1.360	2.720	DF											
1	1	1	0	0	0	0	0	1.365	2.730	E0											
1	1	1	0	0	0	0	1	1.370	2.740	E1											
1	1	1	0	0	0	1	0	1.375	2.750	E2											
1	1	1	0	0	0	1	1	1.380	2.760	E3											
1	1	1	0	0	1	0	0	1.385	2.770	E4											
1	1	1	0	0	1	0	1	1.390	2.780	E5											
1	1	1	0	0	1	1	0	1.395	2.790	E6											
1	1	1	0	0	1	1	1	1.400	2.800	E7											
1	1	1	0	1	0	0	0	1.405	2.810	E8											
1	1	1	0	1	0	0	1	1.410	2.820	E9											
1	1	1	0	1	0	1	0	1.415	2.830	EA											
1	1	1	0	1	0	1	1	1.420	2.840	EB											
1	1	1	0	1	1	0	0	1.425	2.850	EC											
1	1	1	0	1	1	0	1	1.430	2.860	ED											
1	1	1	0	1	1	1	0	1.435	2.870	EE											
1	1	1	0	1	1	1	1	1.440	2.880	EF											

Table 5. SUPPORTED SVID COMMANDS

#	Command	Master Payload	Slave Payload	Description
01h	SetVID_Fast	VID Code	N/A	Set the new VID target, VR Jumps to new VID target with controlled (up or down) slew rate programmed by the VR.
02h	SetVID_Slow	VID Code	N/A	Set the VID target, VR jumps to new VID target with controlled slew rate (up or down) programmed by the VR.
03h	SetVID_Decay	VID Code	N/A	Sets the VID target, VR jumps to new VID target, but **does not** control the slew rate, the output voltage decays at a rate proportional to the load current. SetVID_Decay is only used in VID down direction.
04h	SetPS	Byte indicating power state for slave	N/A	Sends information to VR controller so it can configure VR to improve efficiency, especially at light load.
05h	SetRegAddr	Address of the index in the data table	N/A	Sets the address pointer in the data register table. Typically the next command SetRegData is the payload that gets loaded into this address.
06h	SetRegData	New data register contents	N/A	Writes the contents to the data register that was previously identified by the address pointer with SetRegAddr.
07h	GetReg	Register Address	Specified register contents	Slave returns the contents of the specified register as the payload; The majority of the VR monitoring data is accessed through the GetReg command.
08h	Test Mode			For evaluation purpose only.
09h	SetWP	Byte indicating the working point, slew rate, and alert to select.	N/A	SetWP payload is a bit mapped word that identifies the WP registers which hold the new target VID code, transition slew rate, and alert# behavior when the voltage rails transition to the new voltage targets.

Table 6. SUPPORTED SVID REGISTERS

Index	Name	Description	Master Access	Default
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	85h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC.	R	00h
03h	Date code ID		R	00h
05h	Protocol ID	Identifies the SVID protocol the controller supports. 07h = VR13.0 and 5 mV VID; 04h = VR13.0 and 10 mV VID.	R	07h
06h	Capability	Informs the Master of the controller's Capabilities, 1 = supported, 0 = not supported Bit 7 = Iout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1 Bit 6 = ADC Measurement of Temp Supported = 1 Bit 5 = ADC Measurement of Pin Supported = 0 Bit 4 = ADC Measurement of Vin Supported = 0 Bit 3 = ADC Measurement of Iin Supported = 0 Bit 2 = ADC Measurement of Pout Supported = 0 Bit 1 = ADC Measurement of Vout Supported = 0 Bit 0 = ADC Measurement of Iout Supported = 1	R	C1h
10h	Status_1	Data register read after ALERT# signal is asserted. Conveying the status of the VR. (pp.94, Intel #456098)	R	00h
11h	Status_2	Data register showing optional status_2 data. (pp.94, Intel #456098)	R	00h
12h	Temp Zone	Data register showing temperature zones the system is operating in. (pp.106, Intel #456098) 1 tick is 3 ^{o}C.	R	00h
15h	I_out	8 bit binary word ADC of current. The ADC should be scaled such that FFh= IMAX for the VR for maximum resolution of the ADC data.	R	00h

Table 6. SUPPORTED SVID REGISTERS

Index	Name	Description	Master Access	Default
16h	V_out	Not supported.	R	00h
17h	VR_Temp	8 bit binary word ADC of temperature. Binary format in °C, i.e. 64h = 100°C. 00h indicates this function is not supported. Default value of 19h means 25°C.	R	19h
18h	P_out	Not supported.	R	
1Bh	PIN_H	Not supported.	R	
1Ch	Status 2 Last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h
21h	Icc_Max	Data register containing the Icc_Max. 1 LSB means 1 A. Default value 19h = 25 A.	R	19h
22h	Temp_Max	Data register containing the max temperature and the level VR_hot asserts. This value defaults to 100°C.	R	64h
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us.	R	0Ah
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 4X slower than the SR_fast rate. Binary format in mV/us	R	02h
26h	Vboot	The NCP3285/A ramps to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage. Default value = 0 V.	R	00h
2Ah	SR_Slow Selector	01h = Fast_SR/2 02h = Fast_SR/4 (Default) 04h = Fast_SR/8 08h = Fast_SR/16	R/W	02h
2Eh	Pin_Max	Not supported.	R	
2Fh	Pin_Alert_TH	Not supported.	R	
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. VR 13 VID format. Default values are FFh (1.52 V) in 5 mV mode and 97h (2.0 V) in 10 mV mode.	R/W	FFh
31h	VID setting	Data register containing currently programmed VID voltage. VID data format.	R	00h
32h	Pwr State	Register containing the current programmed power state.	R/W	00h

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h = no offset
		01h = +1 VID step
		02h = +2 VID steps
		FFh = −1 VID step
		FEh = −2 VID steps.
			R/W	00h

34h	MultiVR Config	VR_Ready_0V=1; The VR_Ready line does not de−assert when issued a SetVID(0.0V) orSetPS(4) command.	R	01h
3Ah	Work Point 0	VID target for WP0 command	R/W	00h
3Bh	Work Point 1	VID target for WP1 command	R/W	00h
3Ch	Work Point 2	VID target for WP2 command	R/W	00h
3Dh	Work Point 3	VID target for WP3 command	R/W	00h
3Eh	Work Point 4	VID target for WP4 command	R/W	00h

DETAILED DESCRIPTION

General

The NCP3285/A, a single−phase synchronous buck regulator with SVID, integrates power MOSFETs to provide a high−efficiency and compact−footprint power management solution. The NCP3285/A is able to deliver up to 20 A / 30 A TDC output current on a wide output voltage range. Operating in high switching frequency up to 1 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. It provides differential voltage sense and comprehensive protections.

Operation Modes

Operation mode, switching frequency, VID mode, and fast DVID slew rate are programmed at Mode pin with a ±1% tolerance resistor as shown in Table 7.

Table 7. MODE CONFIGURATION

Resistance @ Mode Pin (Ω, ±1%)	Frequency (kHz)	Operation Mode (PS0 and PS1)	VID Mode		SR_fast
			VBOOT = 0 V to 1.5 V	VBOOT = 1.6 V to 1.8 V	
0	600	FCCM	5 mV	10 mV	10 mV/μs
499	800				
825	1000				20 mV/μs
1.15k	800				
1.62k	600				
2.00k	800				10 mV/μs
2.49k	1000				
3.16k	800				
3.83k	600	Auto DCM/CCM	10 mV		
4.64k	800				
5.62k	1000				
6.65k	1000		5 mV		20 mV/μs
7.87k	800				
9.09k	600				
10.5k	600				10 mV/μs
12.1k	800				
14.0k	1000				
16.2k	1000		10 mV		20 mV/μs
18.7k	800				
21.5k	600				
24.9k	600	FCCM			10 mV/μs
28.7k	800				
33.2k	1000				
Float	800		5 mV		

The NCP3285/A may operate in one of three power states, named PS0 (default), PS1, and PS2 as shown in Table 8, which is programmed by SVID SetPS command. The NCP3285/A can acknowledge commands of SetPS3 and SetPS4 but actually goes into PS2 mode after receiving those commands. The operation mode in PS0 and PS1 is selected at Mode pin. For VR13 applications, FCCM mode needs to be selected for PS0 and PS1.

Table 8. POWER STATUS AND OPERATION MODES

Power Status	Operation Mode
PS0	Forced CCM or Auto CCM/DCM (by Mode Pin) – normal mode (Default)
PS1	Forced CCM or Auto CCM/DCM (by Mode Pin) – low power mode
PS2	Auto CCM/DCM –very low power mode

To have a consistent mode−change behavior and eliminate possible gate driver failures in response to SVID SetPS command, an internal mode−change synchronization circuit is employed. After receival of SetPS command, the internal mode−change signal is triggered at either a rising edge of PWM signal or a time−out signal on a first−come first−served basis. The time−out signal is asserted when both high−side and low−side MOSFETs are off for more than 200 ns in DCM operation.

Current−Mode RPM Operation

The NCP3285/A operates with the current−mode Ramp−Pulse−Modulation (RPM) scheme in PS0/1/2/3 operation states. In Forced CCM mode, the inductor current is always continuous and the device operates in quasi−fixed switching frequency, which has a typical value programmed by users through a resistor at pin FREQ. In Auto CCM/DCM mode, the inductor current is continuous and the device operates in quasi−fixed switching frequency in medium and heavy load range, while the inductor current becomes discontinuous and the device automatically operates in PFM mode with an adaptive fixed on time and variable switching frequency in light load range.

Serial VID interface (SVID)

The NCP3285/A supports Intel serial VID interface. It communicates with the microprocessor through three wires (Clk, Data, ALERT#). Clk, Data and ALERT# should be pulled high to CPU I/O voltage VTT (which is typically 1.0 to 1.1 V) using external Resistors. The SVID bus will operate at a frequency up to 43 MHz. For NCP3285/A, supported SVID commands are listed in Table 5. All the supported registers are shown in Table 6.

SVID Address and Boot−Up Voltage

SVID address is programmed at Addr pin and boot−up voltage is programmed at Vboot pin as shown in Table 9 and Table 10.

ICC_MAX and I_OUT

The NCP3285/A reports output current I_{OUT} as a linear fraction of a full−scale output current named I_{MAX}. I_{MAX} has 9 discrete levels, which should be selected according to the current limit set in the application with an essential margin. The NCP3285/A detects external resistance R_{Ilim} at I_{lim} pin during system reset time before soft start and stores a corresponding IMAX value into Icc_Max register as shown in Table 11. The real output current value I_{OUT} can be obtained from the reading I_out in the register 0x15h with a converting factor of $I_{MAX}/255$.

$$I_{OUT} = \frac{I\_out_{15h}}{255} \cdot I_{MAX} \qquad \text{(eq. 1)}$$

Table 9. SVID ADDRESS SELECTION

Resistance (+/−1%) @ Addr Pin	SVID Address
Float	1111b
150k	1110b
127k	1101b
105k	1100b
88.7k	1011b
75.0k	1010b
61.9k	1001b
51.1k	1000b
43.2k	0111b
36.5k	0110b
30.1k	0101b
21.0k	0100b
14.0k	0011b
9.53k	0010b
5.62k	0001b
0	0000b

Table 10. BOOT−UP VOLTAGE SELECTION

Resistance (+/−1%) @ Vboot Pin	Boot−Up Voltage (V)
Float	1.8
150k	1.7
127k	1.6
105k	1.5
88.7k	1.35
75.0k	1.25
61.9k	1.2
51.1k	1.1
43.2k	1.05
36.5k	1.0
30.1k	0.95
21.0k	0.9
14.0k	0.85
9.53k	0.8
5.62k	0.75
0	0

Table 11. ICC_MAX PROGRAMMING

Resistance (±1%) @ Ilim Pin	I_{MAX} (A)	ICC_MAX Register (21h)	Valley Current Limit (A)
R_{LIM} = 47.5 kΩ	50	32	45
R_{LIM} = 42.2 kΩ	45	2D	40
R_{LIM} = 36.5 kΩ	40	28h	35
R_{LIM} = 31.6 kΩ	35	23h	30
R_{LIM} = 26.1 kΩ	30	1Eh	25
R_{LIM} = 21.0 kΩ	25	19h	20
R_{LIM} = 15.4 kΩ	20	14h	15
R_{LIM} = 10.2 kΩ	15	0Fh	10
R_{LIM} = 5.23 kΩ	10	0Ah	5

Enable and Input UVLO

The NCP3285/A is enabled when the voltage at EN pin is higher than an internal threshold V_{EN_TH}. A hysteresis can be programmed by an external resistor REN connected to EN pin as shown in Figure 4. The high threshold V_{EN_H} in ENABLE signal is

$$V_{EN\_H} = V_{EN\_TH} \quad \text{(eq. 2)}$$

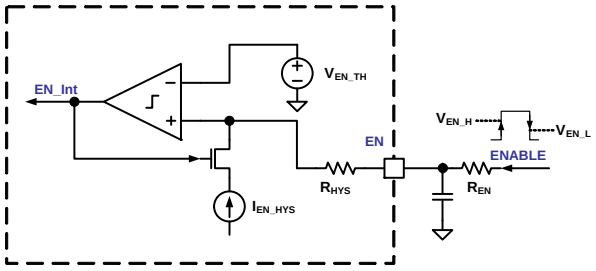


Figure 4. Enable and Hysteresis Programming

The low threshold V_{EN_L} in ENABLE signal is

$$V_{EN\_L} = V_{EN\_TH} - V_{EN\_HYS} \quad \text{(eq. 3)}$$

The hysteresis VEN_HYS is

$$V_{EN\_HYS} = I_{EN\_HYS} \cdot \left(R_{HYS} + R_{EN}\right) \quad \text{(eq. 4)}$$

A UVLO function for input power supply can be implemented at EN pin. As shown in Figure 5, the UVLO threshold can be programmed by two external resistors. The high threshold VIN_H in VIN signal is

$$V_{IN\_H} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \cdot V_{EN\_TH}, \quad \text{(eq. 5)}$$

The low threshold VIN_L in VIN signal is

$$V_{IN\_L} = V_{IN\_H} - V_{IN\_HYS} \quad \text{(eq. 6)}$$

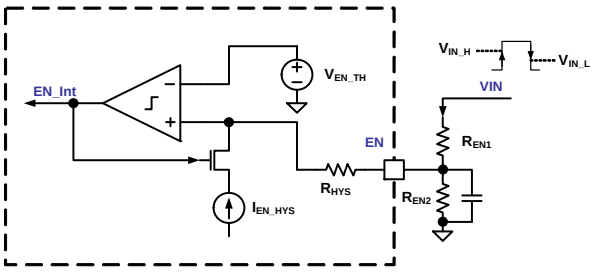


Figure 5. Enable and Input Supply UVLO Circuit

The hysteresis VIN_HYS is

$$V_{IN\_HYS} = I_{EN\_HYS} \cdot \left(R_{HYS}\left(1 + \frac{R_{EN1}}{R_{EN2}}\right) + R_{EN1}\right), \quad \text{(eq. 7)}$$

To avoid undefined operation, EN pin should not be left float in applications.

Over Current Protection (OCP)

The NCP3285/A protects converter from over current by a cycle−by−cycle current limitation. The average current limit ILMT can be calculated from the programmed valley current limit ILMT_Valley and inductor current ripple.

$$I_{LMT} = I_{LMT\_Valley} + \frac{V_O \cdot \left(V_{IN} - V_O\right)}{2 \cdot V_{IN} \cdot L \cdot F_{SW}} = 9.62 \cdot 10^{-4} \cdot R_{Ilim} + \frac{V_O \cdot \left(V_{IN} - V_O\right)}{2 \cdot V_{IN} \cdot L \cdot F_{SW}}, \quad \text{(eq. 8)}$$

where R_{Ilim} is resistance of the programming resistor at Ilim pin, V_{IN} is input voltage, V_O is output voltage, L is filter inductance, and F_{SW} is nominal switching frequency.

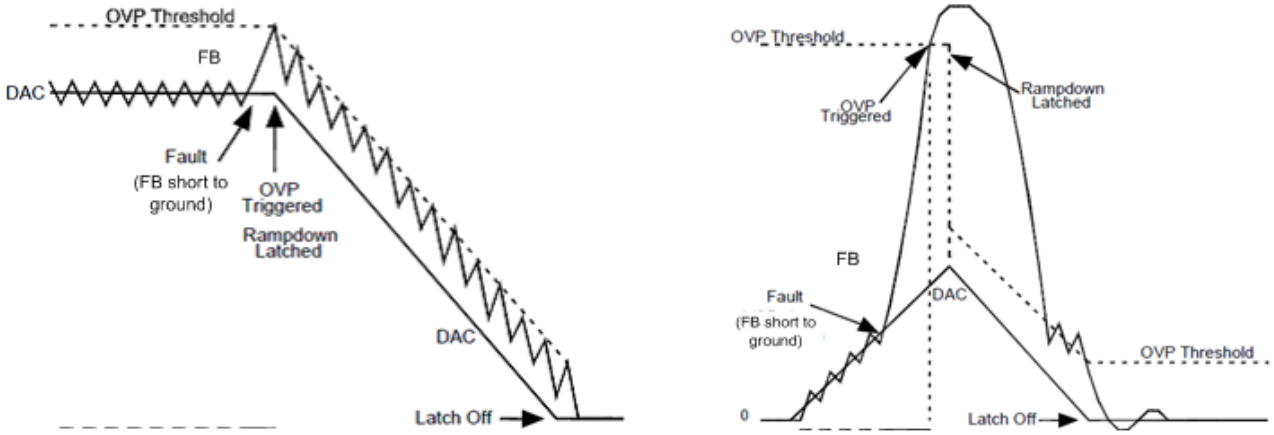
OCP detection starts from beginning of soft−start time TSS, and ends in shutdown. Inductor current is monitored by voltage sensing between SW pin and PGND pin. If over current happens and lasts for more than 50 μs, the device latches off. The device may trip under voltage protection before OCP latch−off if output voltage drops down very fast. To restart the device after OCP latch−off, the system needs to have either VCC or EN toggled state.

Under Voltage Protection (UVP)

UVP detection starts when PGOOD delay Td_PGOOD is expired right after soft start, and ends in shutdown. The NCP3285/A pulls PGOOD low and turns off both high−side and low−side MOSFETs once FB voltage drops below 0.2 V for more than 1.0 μs. To restart the device after UVP latch−off, the system needs to have either VCC or EN toggled state.

Over Voltage Protection (OVP)

OVP detection starts from the beginning of soft−start time TSS and ends in shutdown. During normal operation the output voltage is monitored at FB pin. If FB voltage exceeds the OVP threshold for more than 1 μs, OVP is triggered and PGOOD is pulled low. In the meanwhile, the high−side MOSFET is latched off and the low−side MOSFET is turned on. After the OVP trips, the DAC ramps slowly down to zero, having a negative slew rate as the same value of soft start to reduce negative output voltage spike. The low−side MOSFET toggles between on and off as the output voltage follows the OVP threshold down with a hysteresis. After the DAC gets to zero, the high−side MOSFET holds off and the low−side MOSFET keeps on. During soft−start, the OVP threshold is set to a fixed value of 2.0 V, and it changes to DAC+200 mV after DAC starts to ramp down due to OVP. To restart the device from OVP latch−off, the system needs to have either VCC or EN toggled state.



(a) Normal Operation Mode (b) During Start Up

Figure 6. Function of Over Voltage Protection

Thermal Shutdown (TSD)

The NCP3285/A has an internal thermal shutdown protection to protect the device from overheating in an extreme case that the die temperature exceeds 150°C. TSD detection is activated when VCC and EN are valid. Once the thermal protection is triggered, the whole chip shuts down. If the temperature drops below 125°C, the system automatically recovers and a normal power−up sequence follows.

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- **Power Paths:** Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling:** The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to PVIN and PGND pins.
- **VCC Decoupling:** Place decoupling caps as close as possible to the controller VCC and VDRV pins. The filter resistor at VCC pin should be not higher than 2.2 Ω to prevent large voltage drop.
- **Switching Node:** SW node should be a copper pour, but compact because it is also a noise source.
- **Bootstrap:** The bootstrap cap and an option resistor need to be very close and directly connected between pin 26 (BST) and pin 25 (PHASE). No need to externally connect pin 25 to SW node because it has been internally connected to other SW pins.
- **Ground:** It would be good to have multiple ground planes. Directly connect the exposed PGND pad to ground plane through multiple vias. Connect AGND pin to ground planes through a via close to the pin.
- **Voltage Sense:** Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense. Keep the FB trace short to minimize its capacitance to ground.
- **SVID Bus:** The Serial VID bus is a high speed data bus and the bus routing should be done to limit noise coupling from the switching node. The SVID lines must be ground referenced and each line’s width and spacing should be such that they have nominal 50 Ω impedance with the board stackup. For details, please refer to Intel SVID routing guidelines.

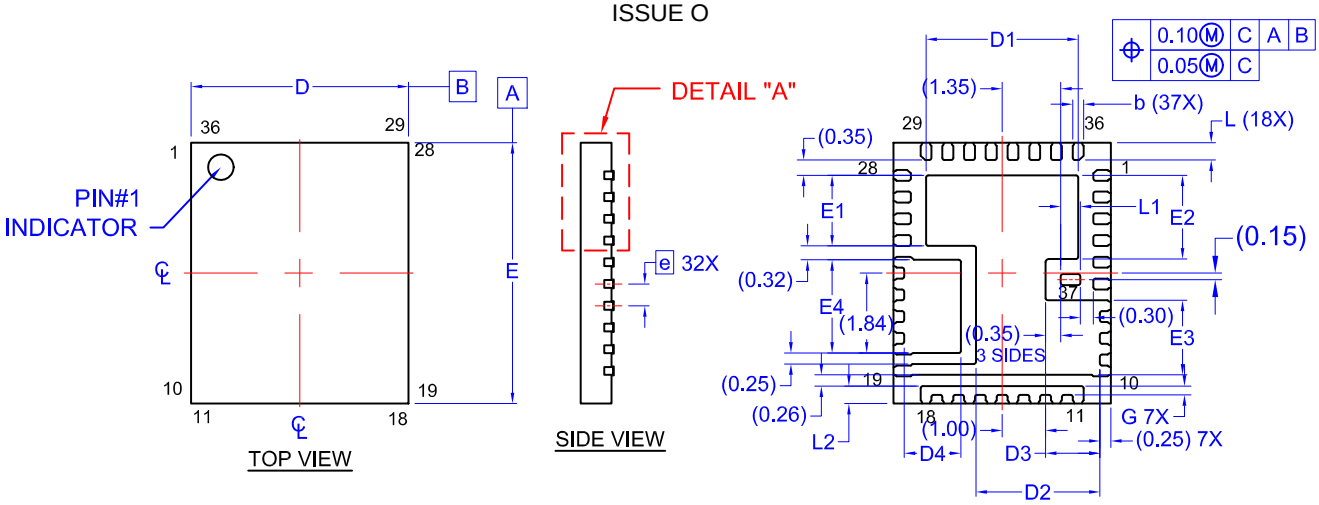
Thermal Layout Considerations

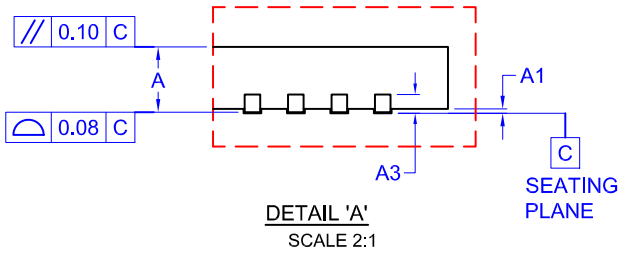
Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

PACKAGE DIMENSIONS

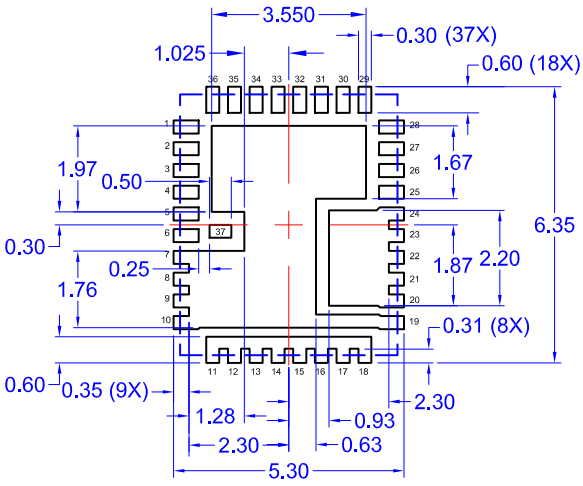
PQFN37 5x6, 0.5P
CASE 483BZ
ISSUE O





DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	3.40	3.50	3.60
D2	2.75	2.85	2.95
D3	1.15	1.25	1.35
D4	1.20	1.30	1.40
E	5.90	6.00	6.10
E1	1.52	1.62	1.72
E2	1.82	1.92	2.02
E3	1.62	1.72	1.82

DIM	MILLIMETERS		
	MIN	NOM	MAX
E4	2.04	2.14	2.24
e	0.50 BSC		
G	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.35	0.45	0.55
L2	0.30	0.40	0.50
M	0.35	0.45	0.55



LAND PATTERN RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

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