NCP45650, NCP45651

Advance Information

ecoSwitch™

Advanced Load Management

Controlled Load Switch with Low R_{ON}

The NCP4565x series of load management devices provide a component and area−reducing solution for efficient power domain switching with inrush current limit via soft start. These devices are designed to integrate control and driver functionality with a high performance low on−resistance power MOSFET in a single package. This cost effective solution is ideal for power management and disconnect functions in USB ports requiring low power consumption in a small footprint.

Features

- Advanced Controller with Charge Pump
- Integrated N-Channel MOSFET with Low R_{ON}
- Soft-Start via Controlled Slew Rate
- Adjustable Slew Rate Control
- Power Good Output
- Thermal Shutdown
- Under Voltage Lockout
- Over Current Protection
- Input Voltage Range 1 V to 13.5 V
- Extremely Low Standby Current
- Load Bleed (NCP45650) − No Load Bleed (NCP45651)
- This is a Pb−Free Device

Typical Applications

- Notebook and Tablet Computers
- Handheld & Mobile Electronics
- Portable Medical Devices
- Hard Drives
- Peripheral Ports

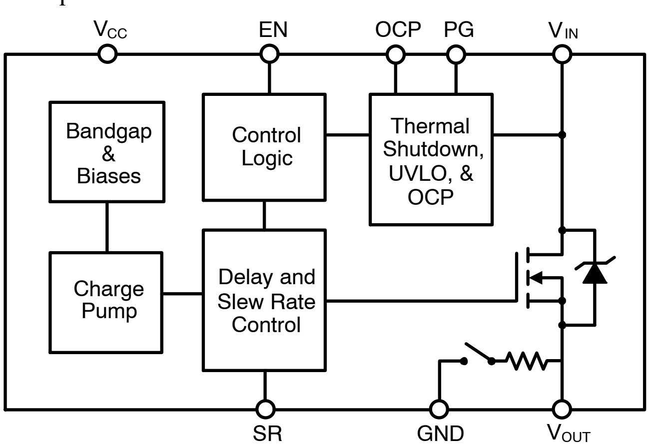


Figure 1. Block Diagram

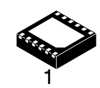
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ON Semiconductor®

www.onsemi.com

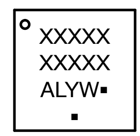
R_{ON} TYP	V_{CC}	V_{IN}	I_{MAX}*
5.1 mΩ	3.3 V	1.8 V	17.5 A
5.3 mΩ	3.3 V	5.0 V	
6.0 mΩ	3.3 V	12 V	

* Imax calculated using max R_{ON} and min short circuit trip voltage



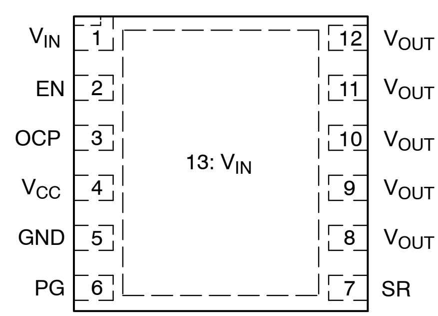
DFN12, 3x3
CASE 506DY

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP45650IMNTWG	DFN12	TBD
NCP45651IMNTWG		

Note: Bleed resistor is contained in the NCP45650

December, 2018 − Rev. P0

Publication Order Number:
NCP45650/D

Table 1. PIN DESCRIPTION

Pin	Name	Function
1, 13	V_{IN}	Input voltage (1.5 V – 13.5 V)
2	EN	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to GND
3	OCP	Over−current protection trip point adjustment made with a voltage applied (0 V – 1.0 V), pin has an internal pull up resistor (250 kΩ +/−20%) to EN; float if over−current protection is not needed
4	V_{CC}	Driver supply voltage (3.0 V – 5.5 V)
5	GND	Driver ground
6	PG	Active−high, open−drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 100 kΩ to an external voltage source required; float if not used.
7	SR	Slew rate adjustment made with an external capacitor to GND; float if not used
8 – 12	V_{OUT}	Source of MOSFET connected to load. Includes an internal bleed resistor to GND

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
Input Voltage Range	V_{IN}	−0.3 to 18	V
Output Voltage Range	V_{OUT}	−0.3 to 18	V
EN Input Voltage Range	V_{EN}	−0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 1)	V_{PG}	−0.3 to 6	V
OCP Input Voltage Range	V_{OCP}	−0.3 to 6	V
Thermal Resistance, Junction−to−Ambient, Steady State (Note 2)	$R_{\theta JA}$	28.6	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	1.7	°C/W
Continuous MOSFET Current @ T_A = 25°C (Note 2)	I_{MAX}	24	A
Total Power Dissipation @ T_A = 25°C (Note 2) Derate above T_A = 25°C	P_D	3.49 34.9	W mW/°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Notes 3 and 4)	ESD_{HBM}	2.0	kV
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1.0	kV
Latch−up Current Immunity (Notes 3 and 4)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PG is an open−drain output that requires an external pull up resistor ≥ 1 kΩ to an external voltage source.
2. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu. SC protection will engage before max current is reached.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78
4. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3	5.5	V
Input Voltage	V_{IN}	1	13.5	V
OCP Input Voltage	V_{OCP}	0	1	V
Ground	GND		0	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
MOSFET						
On−Resistance	V_{CC} = 3.3 V; V_{IN} = 1.8 V	R_{ON}		5.1	6.7	mΩ
	V_{CC} = 3.3 V; V_{IN} = 5 V			5.3	6.9	
	V_{CC} = 3.3 V; V_{IN} = 12 V			6.0	7.5	
	V_{CC} = 3.3 V; V_{IN} = 13.5V			6.7	8.5	
Leakage Current (Note 5)	V_{EN} = 0 V; V_{IN} = 13.5 V	I_{LEAK}		5	100	nA
CONTROLLER						
Supply Standby Current (Note 6)	V_{EN} = 0 V	I_{STBY}		2.7	5	μA
Supply Dynamic Current (Note 7)	V_{EN} = V_{CC} = 3 V; V_{IN} = 12 V	I_{DYN}		450	750	μA
	V_{EN} = V_{CC} = 5.5 V; V_{IN} = 1 V			740	1000	
Internal Load Bleed Resistance (Note 8)	V_{EN} = 0 V	R_{BLEED}	300	590	1000	Ω
Internal Bleed Leakage Current		I_{BLEED}		15.3	80	μA
EN Input High Voltage		V_{IH}	2			V
EN Input Low Voltage		V_{IL}			0.8	V
EN Input Leakage Current	V_{EN} = 0 V	I_{IL}		0.092	1	μA
EN Pull Down Resistance		R_{PD}	110	100	120	kΩ
PG Output Low Voltage	I_{SINK} = 5 mA	V_{OL}		0.12	0.2	V
PG Output Leakage Current	V_{TERM} = 3.3 V	I_{OH}		5	100	nA
Slew Rate Control Constant (Note 9)	Vin = 5 V; Vcc = 3 V	K_{SR}	25	33	41	μA
FAULT PROTECTIONS						
Thermal Shutdown Threshold (Note 10)		T_{SDT}		155		°C
Thermal Shutdown Hysteresis (Note 10)		T_{HYS}		40		°C
V_{IN} Under Voltage Lockout Threshold	V_{IN} rising; Vcc = 3 V	V_{UVLO}	670	710	750	mV
V_{IN} Under Voltage Lockout Hysteresis	Vcc = 3 V	V_{HYS}	40	87	120	mV
Over−Current Protection Trip Voltage Low Vin	V_{IN} < 4.5 V, V_{OCP} = 0 V	V_{TRIP_LVIN}	10	24	40	mV
	V_{IN} < 4.5 V, V_{OCP} = 0.25 V		20	48	80	
	V_{IN} < 4.5 V, V_{OCP} = 0.5 V		50	79	110	
	V_{IN} < 4.5 V, V_{OCP} = 0.75 V		80	111	140	
	V_{IN} < 4.5 V, V_{OCP} = 1 V		110	143	180	
Over−Current Protection Trip Voltage High Vin	V_{IN} > 4.5 V, V_{OCP} = 0 V	V_{TRIP_HVIN}	10	28	40	mV
	V_{IN} > 4.5 V, V_{OCP} = 0.25 V		45	59	80	
	V_{IN} > 4.5 V, V_{OCP} = 0.5 V		75	90	110	
	V_{IN} > 4.5 V, V_{OCP} = 0.75 V		105	121	140	
	V_{IN} > 4.5 V, V_{OCP} = 1 V		135	153	180	
Over−Current Protection Blanking Time	Vcc = 3 V	t_{OCP}	2	3.4	5	ms
OCP Pull Up Resistance (Note 11)		R_{OCP}	200	250	300	kΩ
Short−Circuit Protection Trip Voltage Low Vin		V_{SC_LVIN}	110	150	190	mV
Short−Circuit Protection Trip Voltage High Vin		V_{SC_HVIN}	135	160	190	mV

5. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
6. Average current from V_{CC} to GND with MOSFET turned off and Vin is 13.5 V.
7. Average current from V_{CC} to GND after MOSFET gate is charged.
8. Resistance from VOUT to GND when the MOSFET driver is disabled.
9. See Applications Information section for details on how to adjust the gate slew rate.
10. Operation above T_J = 125°C is not guaranteed.
11. Internal resistor from OCP to EN used to pull up on OCP pin if not driven.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

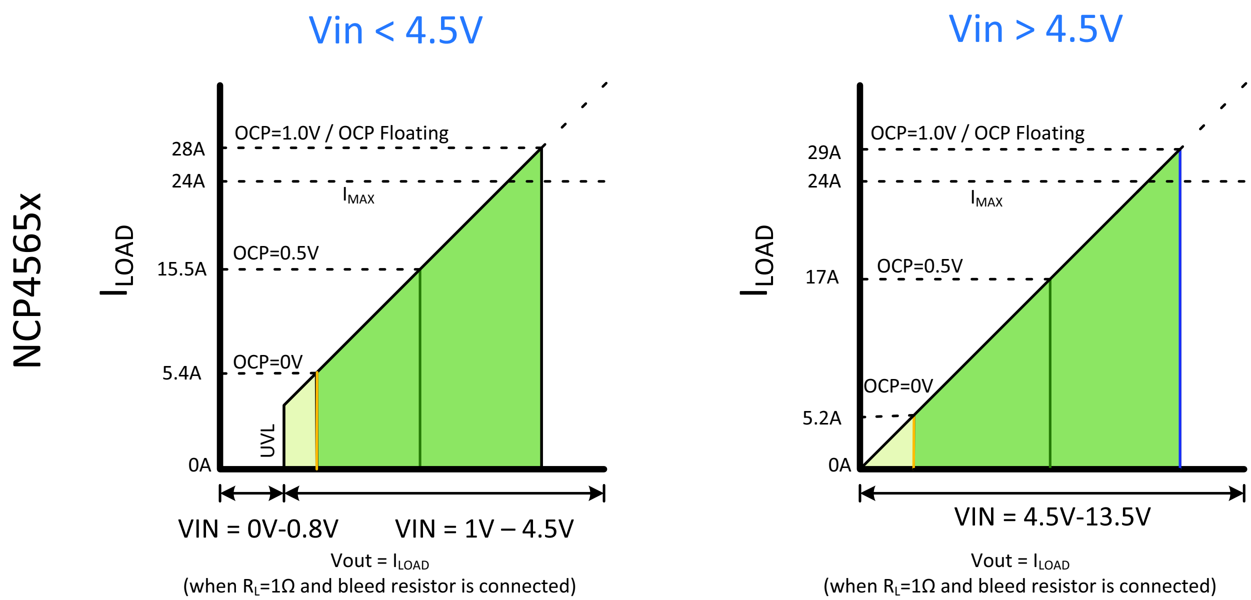


Figure 2. Safe Operating Area Plots (green represents non−fault conditions)

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Notes 12 and 13)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate − Default	V_{CC} = 3.3 V; V_{IN} = 1.8 V	SR		19		V/ms
	V_{CC} = 5.0 V; V_{IN} = 1.8 V			19		
	V_{CC} = 3.3 V; V_{IN} = 12 V			21		
	V_{CC} = 5.0 V; V_{IN} = 12 V			22		
Output Turn−on Delay	V_{CC} = 3.3 V; V_{IN} = 1.8 V	T_{ON}		138		μs
	V_{CC} = 5.0 V; V_{IN} = 1.8 V			170		
	V_{CC} = 3.3 V; V_{IN} = 12 V			260		
	V_{CC} = 5.0 V; V_{IN} = 12 V			250		
Output Turn−off Delay	V_{CC} = 3.3 V; V_{IN} = 1.8 V	T_{OFF}		2.0		μs
	V_{CC} = 5.0 V; V_{IN} = 1.8 V			1.6		
	V_{CC} = 3.3 V; V_{IN} = 12 V			0.7		
	V_{CC} = 5.0 V; V_{IN} = 12 V			0.4		
Power Good Turn−on Time	V_{CC} = 3.3 V; V_{IN} = 1.8 V	$T_{PG,ON}$		1.02		ms
	V_{CC} = 5.0 V; V_{IN} = 1.8 V			0.95		
	V_{CC} = 3.3 V; V_{IN} = 12 V			1.52		
	V_{CC} = 5.0 V; V_{IN} = 12 V			1.23		
Power Good Turn−off Time	V_{CC} = 3.3 V; V_{IN} = 1.8 V	$T_{PG,OFF}$		20		ns
	V_{CC} = 5.0 V; V_{IN} = 1.8 V			14		
	V_{CC} = 3.3 V; V_{IN} = 12 V			20		
	V_{CC} = 5.0 V; V_{IN} = 12 V			14		

12. See below figure for Test Circuit and Timing Diagram.
13. Tested with the following conditions: V_{TERM} = V_{CC}; R_{PG} = 100 kΩ; R_L = 10 Ω; C_L = 0.1 μF.

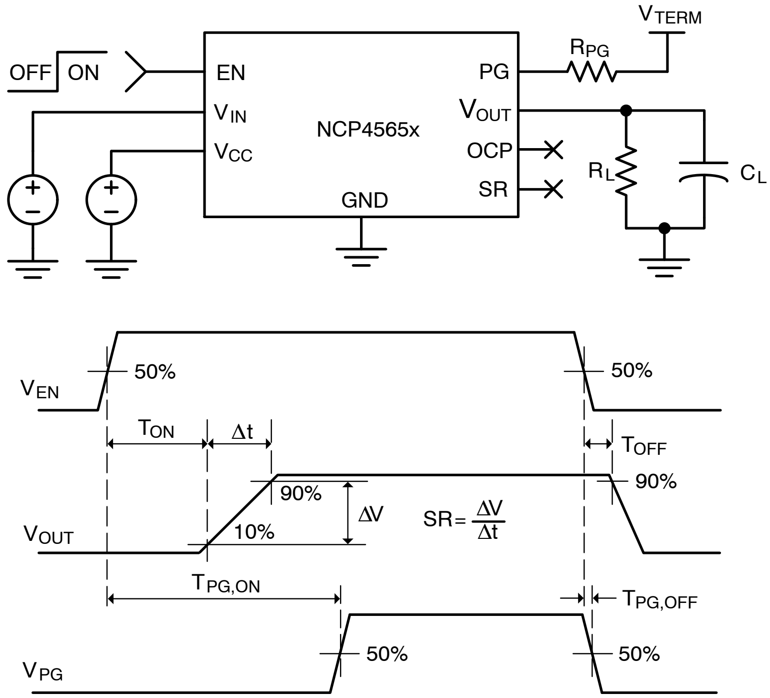


Figure 3. Switching Characteristics Test Circuit and Timing Diagrams

APPLICATIONS INFORMATION

Enable Control

The NCP4565x parts allow for enabling the MOSFET in an active−high configuration. When the EN pin is at a logic high level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

Load Bleed

The NCP45650 device has an on−chip bleed resistor that is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. Delays are added to the enable of this switch to ensure that both the MOSFET and the bleed switch are not concurrently active. The NCP45651 does not include the load bleed function.

Over−Current and Short−Circuit Protection

The NCP4565x devices are equipped with over−current and short−circuit protection that are used to help protect the part and the system from a sudden high−current event, such as the output, V_{OUT}, being shorted to ground. This circuitry is only active when the gate of the MOSFET is fully driven.

Once active, the circuitry monitors the difference in the voltage on the V_{IN} pin and the voltage on the V_{OUT} pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is immediately turned off and for the NCP45650 the load bleed is activated. The part remains latched in this off state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The over−current trip point can be controlled with the OCP pin to allow for protection before the short−circuit threshold. If no adjustment is needed, then OCP can be left floating. In the event the OCP threshold is exceeded, the MOSFET will shut down after the blanking time if the voltage difference remains greater than the threshold. Like the short−circuit protection, the part remains latched in this off state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Thermal Shutdown

The thermal shutdown of the NCP4565x devices protect the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over−temperature condition is detected, the MOSFET is immediately turned off and the load bleed is activated.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Under Voltage Lockout

The under voltage lockout of the NCP45655x devices turn the MOSFET off and activate the load bleed when the input voltage, V_{IN}, drops below the under voltage lockout threshold. This circuitry is disabled when EN is not active to reduce standby current.

If the V_{IN} voltage rises above the under voltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The NCP4565x devices have a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, RPG, greater than or equal to 1k to an external voltage source that is compatible with input levels of all devices connected to this pin.

The power good output can be used as the enable signal for other active−high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

Slew Rate Control

The NCP4565x devices are equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}}\ [V/s] \qquad \text{(eq. 1)}$$

Where K_{SR} is the specified slew rate control constant, found on page 3, and C_{SR} is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified Imax. CL (capacitive load) should be less then Cmax as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}}$$

Where Imax is the maximum load current, and SRtyp is the typical default slew rate when no external load capacitor is added to the SR pin.

ecoSWITCH LAYOUT GUIDELINES

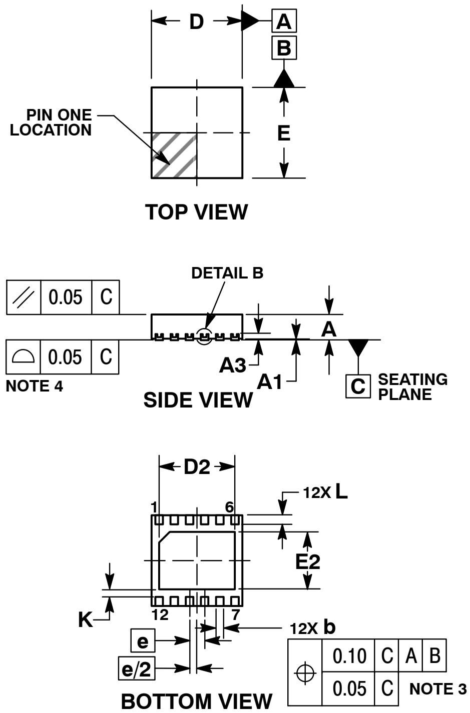
Electrical Layout Considerations

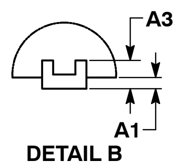
Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

Power Planes: The ecoSWITCH is optimized for extremely low Ron resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the VIN and VOUT pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of VIN to VOUT should be avoided, as this will adversely affect slew rates. The figure below shows an example of correct power plane layout. The number and location of pins for specific ecoSWITCH products may vary. This demonstrates large planes for both VIN and VOUT, while avoiding capacitive coupling between the two planes.

PACKAGE DIMENSIONS

DFN12 3x3, 0.5P
CASE 506DY
ISSUE O

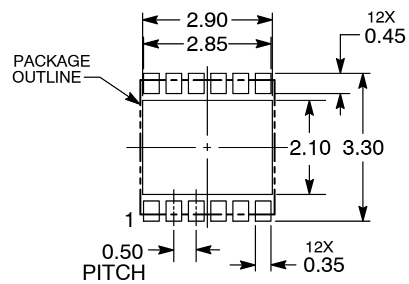




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.50 BSC		
K	0.25 REF		
L	0.20	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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