LDO Regulator, 150 mA, 38 V, 1 μA I_Q, with PG

Product Preview

NCP730

The NCP730 device is based on unique combination of features − very low quiescent current, fast transient response and high input and output voltage ranges. The NCP730 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Quiescent current of only 1 μA makes this device ideal solution for battery−powered, always−on systems. Several fixed output voltage versions are available as well as the adjustable version.

The device (version B) implements power good circuit (PG) which indicates that output voltage is in regulation. This signal could be used for power sequencing or as a microcontroller reset.

Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage: 1.2 V to 24 V
- Capable of Sourcing 200 mA Peak Output Current
- Low Shutdown Current: 100 nA typ.
- Very Low Quiescent Current: 1 μA typ.
- Low Dropout: 290 mV typ. at 150 mA, 3.3 V Version
- Output Voltage Accuracy ±1%
- Power Good Circuit (Version B)
- Stable with Small 1 μF Ceramic Capacitors
- Built−in Soft Start Circuit to Suppress Inrush Current
- Over−Current and Thermal Shutdown Protections
- Available in Small TSOP−5 and WDFN6 (2x2) Packages
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Battery Power Tools and Equipment
- Home Automation
- RF Devices
- Metering
- Remote Control Devices
- White Goods

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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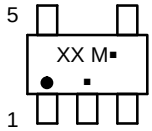
TSOP−5
CASE 483

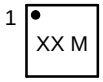
WDFN6 (2x2)
CASE 511BR

MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

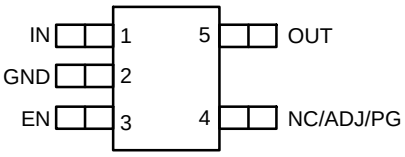
(Note: Microdot may be in either location)



XX = Specific Device Code
M = Date Code

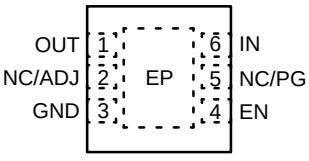
PIN ASSIGNMENTS

TSOP−5



CASE 483

WDFN6 (2x2)



CASE511BR

(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

TYPICAL APPLICATION SCHEMATICS

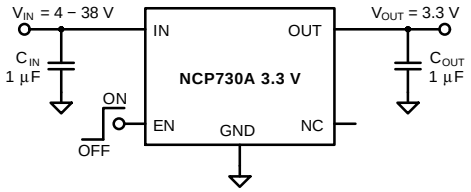


Figure 1. Fixed Output Voltage Application (No PG)

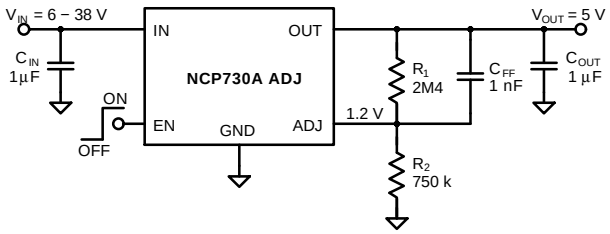


Figure 2. Adjustable Output Voltage Application (No PG)

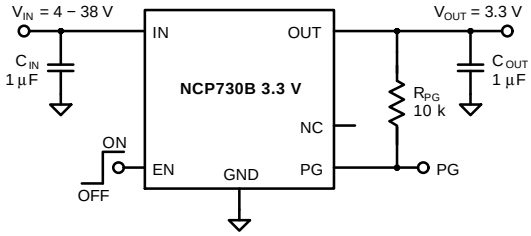


Figure 3. Fixed Output Voltage Application with PG

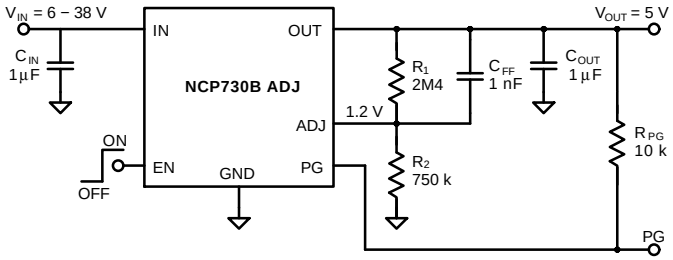


Figure 4. Adjustable Output Voltage Application with PG

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

SIMPLIFIED BLOCK DIAGRAMS

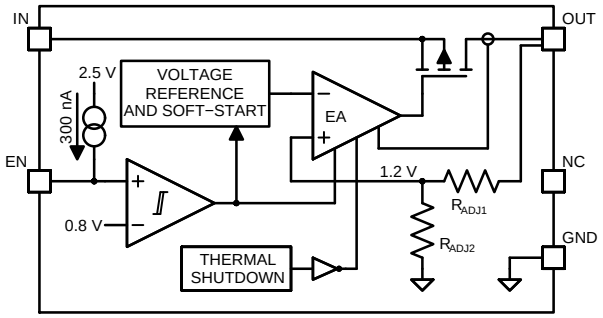


Figure 5. NCP730A FIX (A Version = No PG)
Applicable for TSOP−5 and WDFN−6 2x2

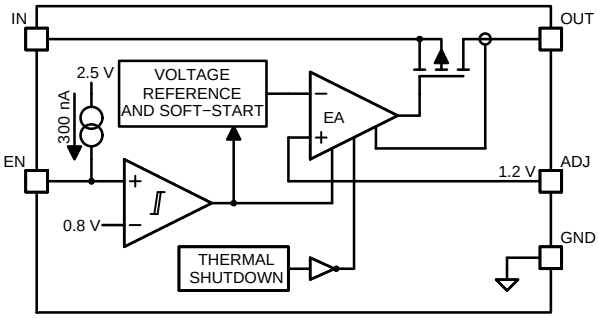


Figure 6. NCP730A ADJ (A Version = No PG)
Applicable for TSOP−5 and WDFN−6 2x2

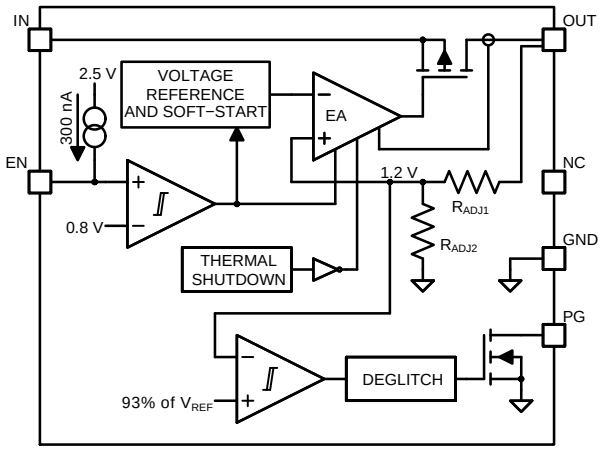


Figure 7. NCP730B FIX (B Version = with PG)
Applicable for TSOP−5 and WDFN−6 2x2

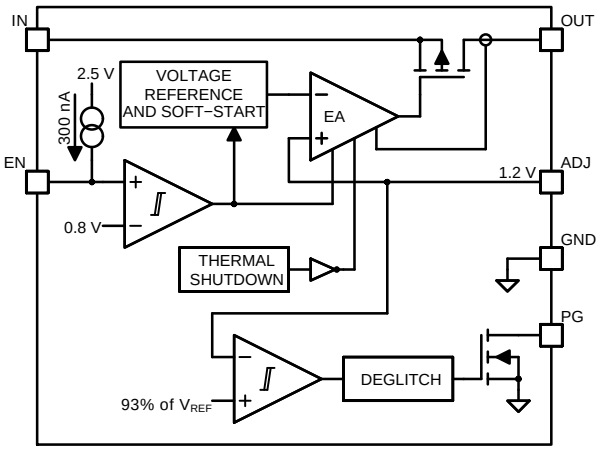


Figure 8. NCP730B ADJ (B Version = with PG)
Applicable for WDFN−6 2x2

PIN DESCRIPTION

Pin No. TSOP−5	Pin No. WDFN−6	Pin Name	Description
1	6	IN	Power supply input pin.
2	3	GND	Ground pin.
5	1	OUT	LDO output pin.
3	4	EN	Enable input pin (high − enabled, low − disabled). If this pin is connected to IN pin or if it is left unconnected (pull−up resistor is not required) the device is enabled.
4 (Note 1)	2	ADJ	Adjust input pin, could be connected to the resistor divider to the OUT pin.
4 (Note 1)	5	PG	Power good output pin. Could be left unconnected or could be connected to GND if not needed.
4 (Note 1)	2, 5	NC	Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation.
NA	EP	EPAD	Connect the exposed pad to GND.

1. Pin function depends on device version.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VIN Voltage (Note 2)	V_{IN}	−0.3 to 40	V
VOUT Voltage	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 40 V; what is lower]	V
EN Voltage	V_{EN}	−0.3 to (V_{IN} + 0.3)	V
ADJ Voltage	$V_{FB/ADJ}$	−0.3 to 5.5	V
PG Voltage	V_{PG}	−0.3 to (V_{IN} + 0.3)	V
Output Current	I_{OUT}	Internally limited	mA
PG Current	I_{PG}	3	mA
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114 (AEC−Q100−002)
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101 (AEC Q100−011D)

THERMAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	WDFN6 2x2	TSOP−5	Unit
Thermal Resistance, Junction−to−Air	R_{thJA}	61	142	°C/W
Thermal Resistance, Junction−to−Case (top)	R_{thJCt}	TBD	80	°C/W
Thermal Resistance, Junction−to−Case (bottom)	R_{thJCb}	14	N/A	°C/W
Thermal Resistance, Junction−to−Board (top)	R_{thJBt}	TBD	76	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Psi_{JCt}	3	21	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Psi_{JB}	TBD	61	°C/W

4. Measured according to JEDEC board specification (board 1S2P, Cu layer thickness 1 oz, Cu area 650 mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT−NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective capacitance – Note 5), T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified) (Note 6)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Recommended Input Voltage		V_{IN}	2.7	−	38	V
Output Voltage Accuracy	T_J = −40°C to +85°C	V_{OUT}	−1	−	1	%
	T_J = −40°C to +125°C		−1	−	2	
ADJ Reference Voltage	ADJ version only	V_{ADJ}	−	1.2	−	V
ADJ Input Current	V_{ADJ} = 1.2 V	I_{ADJ}	−0.1	0.01	0.1	μA
Line Regulation	V_{IN} = $V_{OUT−NOM}$ + 1 V to 38 V and V_{IN} ≥ 2.7 V	$\Delta V_{O(\Delta VI)}$	−	−	0.2	$\%V_{OUT}$
Load Regulation	I_{OUT} = 0.1 mA to 150 mA	$\Delta V_{O(\Delta IO)}$	−	−	0.4	$\%V_{OUT}$
Quiescent Current (version A)	V_{IN} = $V_{OUT−NOM}$ + 1 V to 38 V, I_{OUT} = 0 mA	I_Q	−	1.3	2.5	μA
Quiescent Current (version B)	V_{IN} = $V_{OUT−NOM}$ + 1 V to 38 V, I_{OUT} = 0 mA		−	1.8	3.0	
Ground Current	I_{OUT} = 150 mA	I_{GND}	−	325	450	μA
Shutdown Current	V_{EN} = 0 V, I_{OUT} = 0 mA	I_{SHDN}	−	0.35	1.5	μA
Output Current Limit	V_{OUT} = $V_{OUT−NOM}$ − 100 mV	I_{OLIM}	200	280	450	mA
Short Circuit Current	V_{OUT} = 0 V	I_{OSC}	200	280	450	mA

ELECTRICAL CHARACTERISTICS (V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF (effective capacitance – Note 5), T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified) (Note 6) (continued)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Dropout Voltage (Note 7)	I_{OUT} = 150 mA		V_{DO}	−	290	480	mV
Power Supply Ripple Rejection	V_{IN} = $V_{OUT-NOM}$ + 2 V I_{OUT} = 10 mA	10 Hz	PSRR	−	80	−	dB
		10 kHz		−	70	−	
		100 kHz		−	42	−	
		1 MHz		−	48	−	
Output Noise	f = 10 Hz to 100 kHz		V_N	−	100* V_{OUT}	−	μV_{RMS}
EN Threshold	V_{EN} rising		V_{EN-TH}	0.7	0.9	1.05	V
EN Hysteresis	V_{EN} falling		V_{EN-HY}	0.01	0.1	0.2	V
EN Internal Pull−up Current	V_{EN} = 1 V, V_{IN} = 5.5 V		I_{EN}	−	0.3	1	μA
Start−up time (Note 8)	$V_{OUT-NOM}$ ≤ 3.3 V		t_{START}	100	250	500	μs
	$V_{OUT-NOM}$ > 3.3 V			300	600	1000	
Internal UVLO Threshold	Ramp V_{IN} up until output is turned on		V_{IUL-TH}	1.6	1.95	2.6	V
Internal UVLO Hysteresis	Ramp V_{IN} down until output is turned off		V_{IUL-HY}	0.05	0.2	0.3	V
PG Threshold (Note 9)	V_{OUT} rising		V_{PG-TH}	90	93	96	%
PG Hysteresis (Note 9)	V_{OUT} falling		V_{PG-HY}	0.1	2	3.5	%
PG Deglitch Time (Note 9)			t_{PG-DG}	75	160	270	μs
PG Delay Time (Note 9)			t_{PG-DL}	120	320	600	μs
PG Output Low Level Voltage (Note 9)	I_{PG} = 1 mA		V_{PG-OL}	−	0.2	0.4	V
PG Output Leakage Current (Note 9)	V_{PG} = 30 V		I_{PG-LK}	−	0.1	1	μA
Thermal Shutdown Temperature	Temperature rising from T_J = +25°C		T_{SD}	−	165	−	°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	−	20	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
7. Dropout measured when the output voltage falls 100 mV below the nominal output voltage. Limits are valid for all voltage versions.
8. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.
9. Applicable only to version B (device option with power good output).

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT−NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

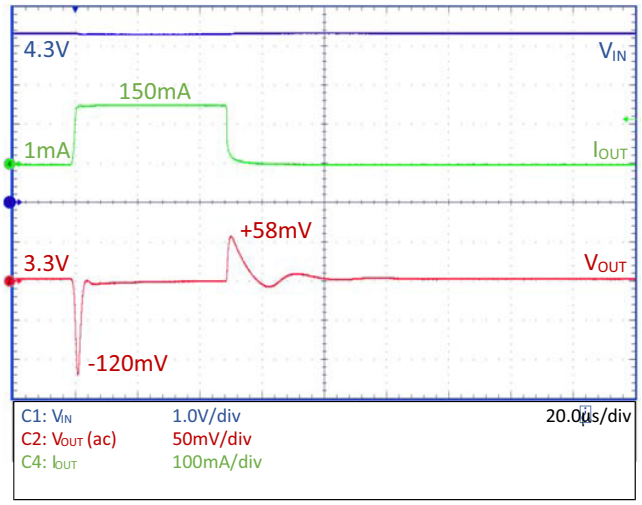


Figure 9. NCP730−3.3 V, C_{OUT} = 1 μF

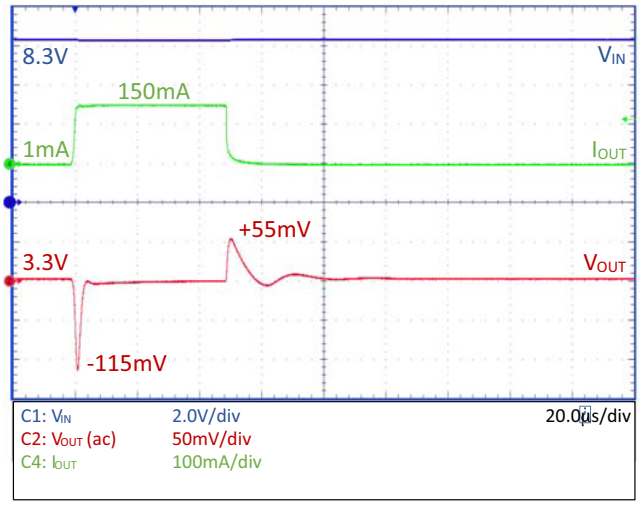


Figure 10. NCP730−3.3 V, C_{OUT} = 1 μF

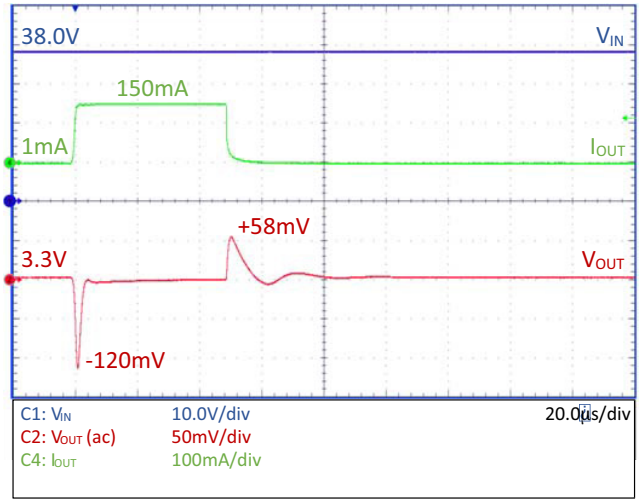


Figure 11. NCP730−3.3 V, C_{OUT} = 1 μF

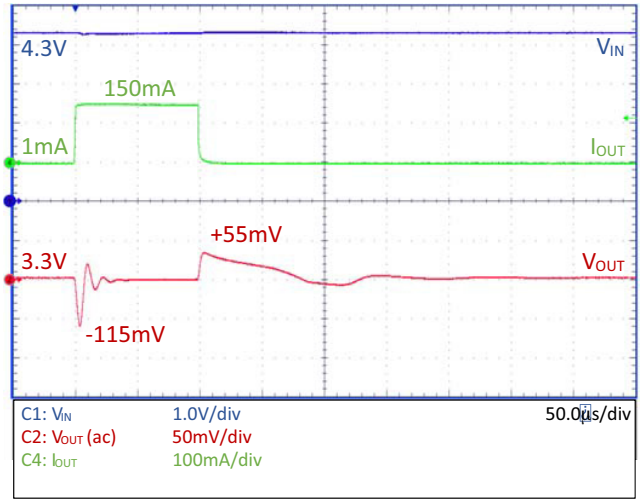


Figure 12. NCP730−3.3 V, C_{OUT} = 10 μF

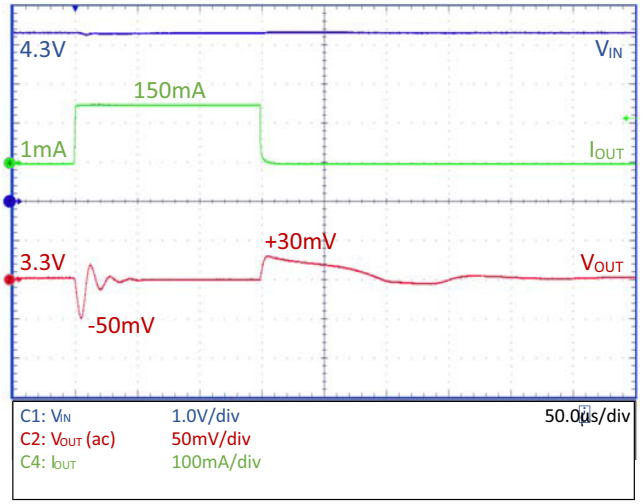


Figure 13. NCP730−3.3 V, C_{OUT} = 22 μF

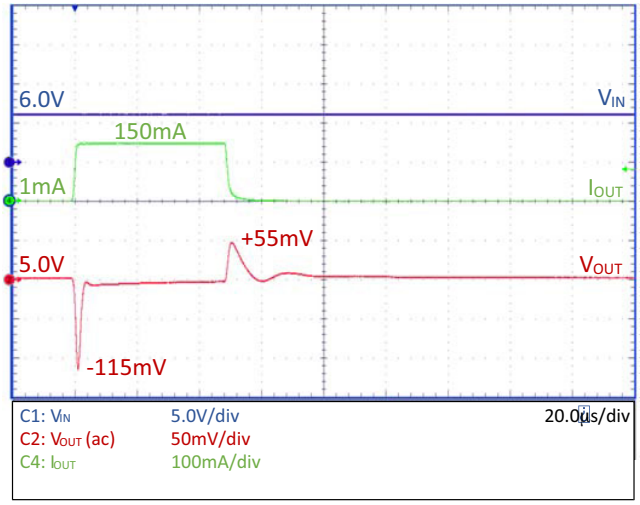


Figure 14. NCP730−5.0 V, C_{OUT} = 1 μF

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

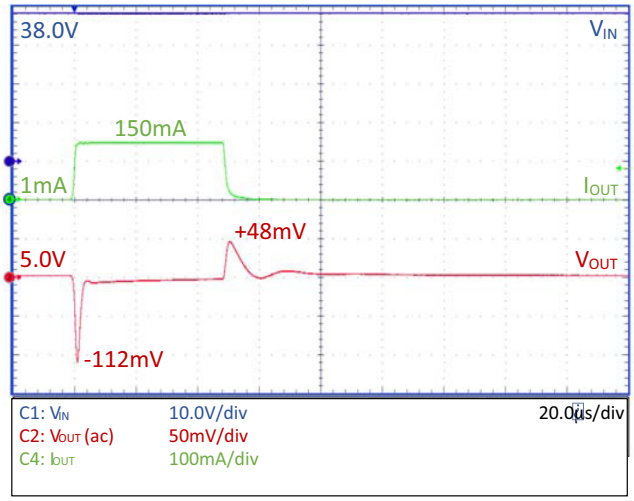


Figure 15. NCP730−5.0 V, C_{OUT} = 1 μF

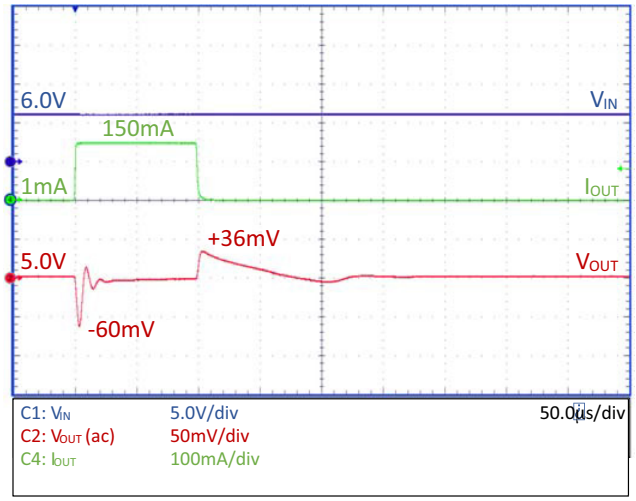


Figure 16. NCP730−5.0 V, C_{OUT} = 10 μF

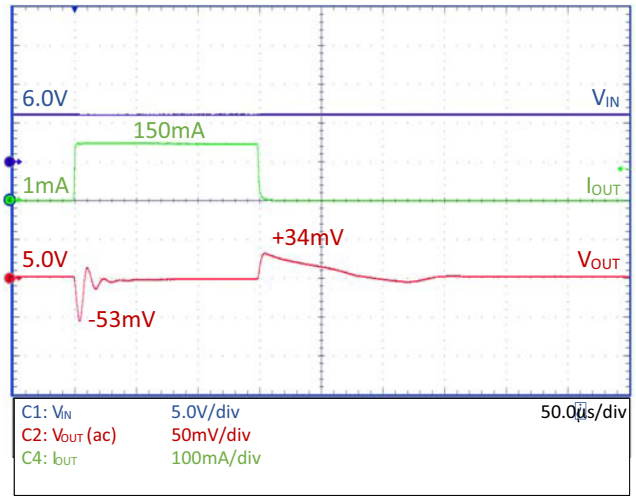


Figure 17. NCP730−5.0 V, C_{OUT} = 22 μF

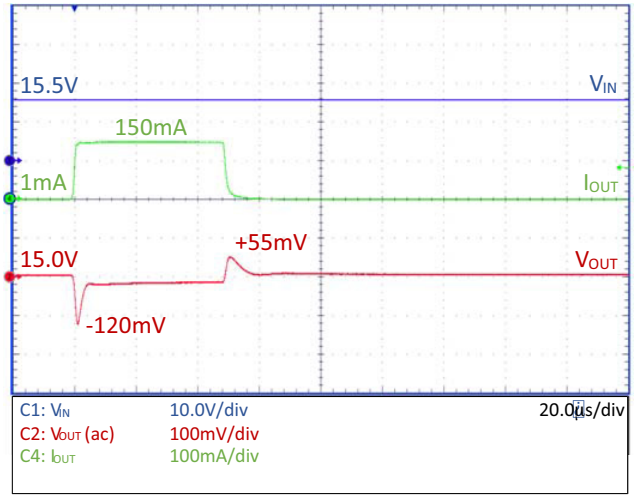


Figure 18. NCP730−15.0 V, C_{OUT} = 1 μF

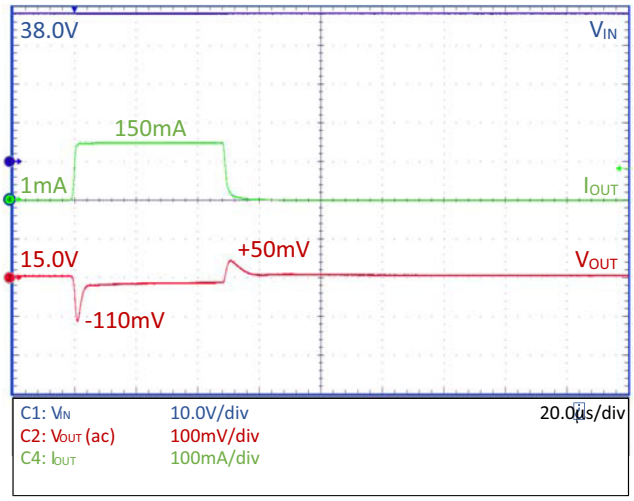


Figure 19. NCP730−15.0 V, C_{OUT} = 1 μF

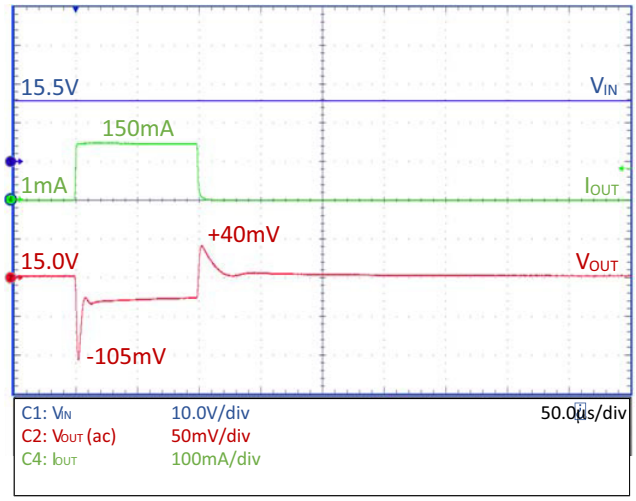


Figure 20. NCP730−15.0 V, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT−NOM}$ + 1 V and V_{IN} ≥ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{OUT} = 1.0 μF, ADJ tied to OUT, T_J = 25°C, unless otherwise specified

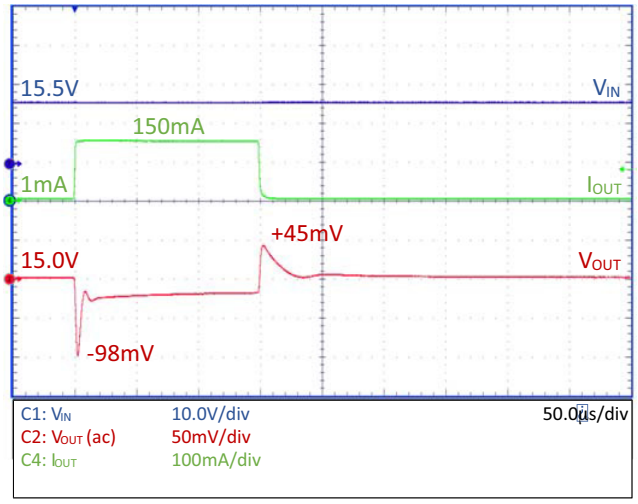


Figure 21. NCP730−15.0 V, C_{OUT} = 22 μF

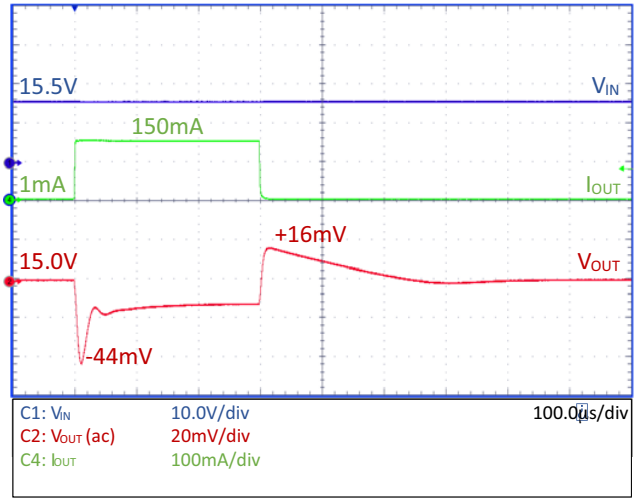


Figure 22. NCP730−15.0 V, C_{OUT} = 50 μF

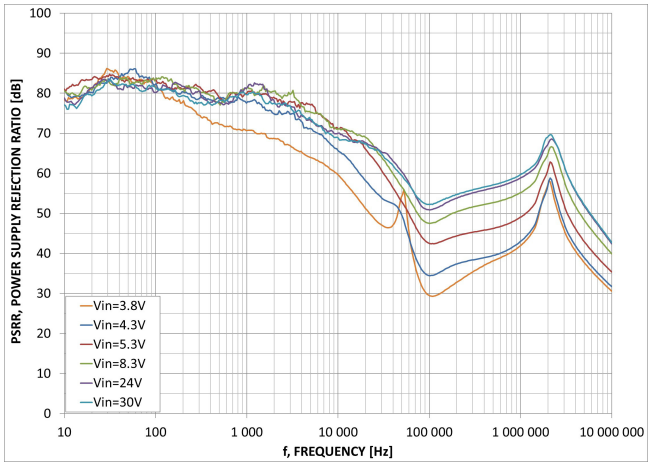


Figure 23. PSRR − NCP730−3.3 V, C_{OUT} = 1 μF, I_{OUT} = 10 mA

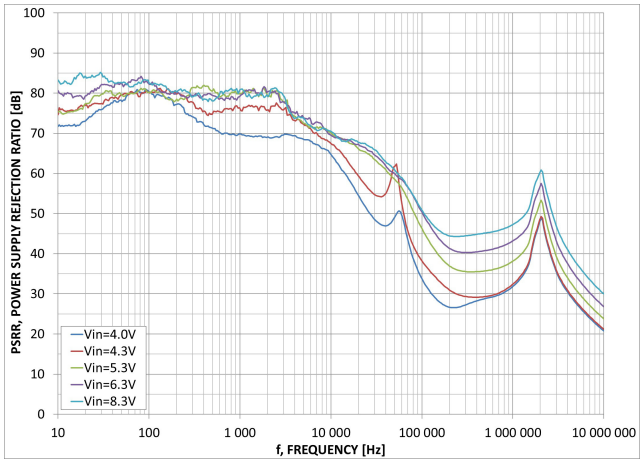


Figure 24. PSRR − NCP730−3.3 V, C_{OUT} = 1 μF, I_{OUT} = 100 mA

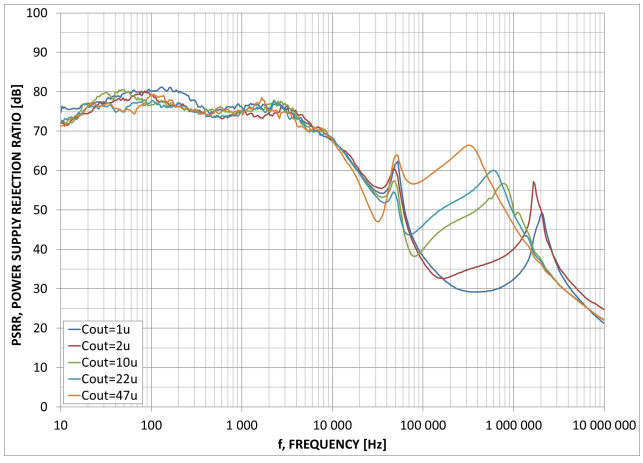


Figure 25. PSRR − NCP730−3.3 V, V_{IN} = 4.3 V, I_{OUT} = 100 mA

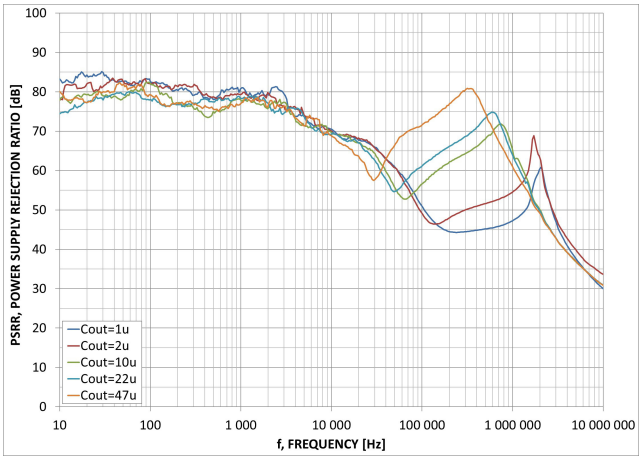


Figure 26. PSRR − NCP730−3.3 V, V_{IN} = 8.3 V, I_{OUT} = 100 mA

APPLICATIONS INFORMATION

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater (max. value is not limited). This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes. When a large load transients (like 1 mA to 150 mA) happens in the application the input power source of the LDO needs to provide enough power and the input voltage must not go below the level defined by this equation: $V_{IN} = V_{OUT-NOM} + V_{DO}$ otherwise the output voltage drop will be significantly higher (because LDO will enter the dropout state). In some cases when power supply powering the LDO has a poor load transient response or when there is a long connection between LDO and its power source then capacitance of input capacitor needs to be high enough to cover the LDO's input voltage drop caused by load transient and maintains its value above the $V_{IN} = V_{OUT-NOM} + V_{DO}$ level (then C_{IN} could be in range of hundreds of μF).

Output Capacitor Selection (C_{OUT})

The LDO requires the output capacitor connected as close as possible to the output and ground pins. The LDO is designed to remain stable with output capacitor's effective capacitance in range from 1 μF to 100 μF and ESR from 1 mΩ to 200 mΩ. The ceramic X7R or X5R type is recommended due to its low capacitance variations over the specified temperature range and low ESR. When selecting the output capacitor the changes with temperature and DC bias voltage needs to be taken into account. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details). Larger capacitance and lower ESR improves the load transient response and PSRR.

Output Voltage

NCP730 is available in two version from output voltage point of view. One is fixed output voltage version (FIX version) and the other one is adjustable output voltage version (ADJ version).

The ADJ version has ADJ pin, which could be connected to the OUT pin directly, just to compensate voltage drop across the internal bond wiring and PCB traces or could be connected to the middle point of the output voltage resistor divider for adjustment. When it is connected to the OUT pin the output voltage of the circuit is simply the same as the nominal output voltage of the LDO. When connected to the resistor divider the output voltage could be computed as the ADJ reference voltage (1.2 V) multiplied by the resistors divider ratio, see following equation.

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1 \quad \text{(eq. 1)}$$

Where:

V_{OUT} is output voltage of the circuit with resistor divider.
V_{ADJ} is the LDO's ADJ reference voltage.
I_{ADJ} is the LDO's ADJ pin input current.
R_1 and R_2 are resistors of output resistor divider.

At the classical "old style" regulators like LM317 etc. the resistors where small (100 Ω − 10 kΩ) to make regulator stable at light loads (divider was also a pre−load function). On NCP730, which is very low quiescent current LDO regulator (1 μA), we need to care about current consumption of surrounding circuitry so we need to set the current through resistor divider flowing from V_{OUT} through R_1 and R_2 to GND, as low as possible.

On the other hand, the parasitic leakage current flowing into ADJ pin (I_{ADJ}) causes V_{OUT} voltage error (given by). The I_{ADJ} is temperature dependent so it is changing and we cannot compensate it in application, we just can minimize the influence by setting of R_1 value low, what is in opposite to maximizing its value because of current consumption.

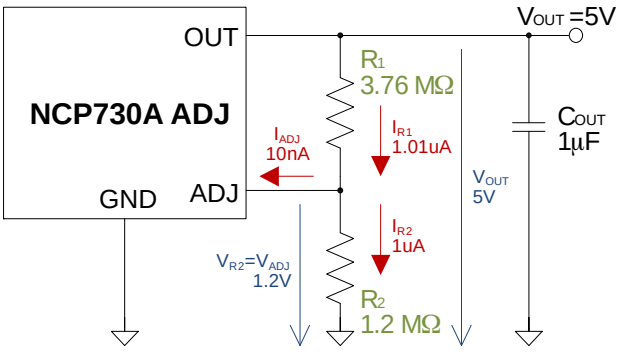
So when selecting the R_1 and R_2 values we need to find a compromise between desired V_{OUT} error (temperature dependent) and total circuit quiescent current.

If we want to simplify this task, we can say the I_{R2} should be 100−times higher than I_{ADJ} at expected T_J temperature range. If we chose the ratio "I_{R2} to I_{ADJ85}" higher (for example more than 100 as stated before), the ΔV_{OUT} error caused by I_{ADJ} change over temperature would be lower and opposite.

In limited T_J temperature range 40°C to +85°C the I_{ADJ} is about 10−times smaller than in the full temperature range 40°C to +125°C (see typical characteristics graph of I_{ADJ} over temperatures).

Example 1:

Desired V_{OUT} voltage is 5.0 V. Computed maximal T_J in application (based on max. power dissipation and cooling) is 85°C. Than maximal I_{ADJ} is at 85°C and is about: I_{ADJ85} = 10 nA.



We chose:

$$I_{R2} = 100 \cdot I_{ADJ85} = 100 \cdot 10E{-}9 = 1\ \mu A$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{1E{-}6} = 1.2\ M\Omega$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ85} + I_{R2}} = \frac{5 - 1.2}{10E{-}9 + 1E{-}6} = \frac{3.8}{1.01E{-}6} = 3.762\ M\Omega$$

Verification:

For low temperature (T_J = 25°C) the I_{ADJ25} = 1 nA:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ADJ} \cdot R_1$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 1E{-}9 \cdot 3.762E6 = 4.966\ V$$

For maximal temperature (T_J = 85°C) the I_{ADJ85} = 10 nA:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{3.762E6}{1.2E6}\right) + 10E{-}9 \cdot 3.762E6 = 5.000\ V$$

Output voltage error for temperatures 85°C to 25°C is:

$$\Delta V_{OUT} = \frac{V_{OUT85} - V_{OUT25}}{V_{OUT85}} \cdot 100 = \frac{5.000 - 4.966}{5.000} \cdot 100 = 0.68\%$$

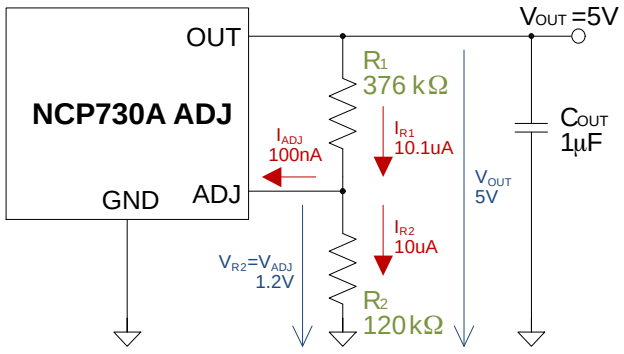
Total circuit quiescent current at T_J = 25°C is:

$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E{-}6 + 1.01E{-}6 = 2.31\ \mu A$$

We can see that current consumption of external resistor divider is almost the same as quiescent current of LDO.

Example 2:

Desired V_{OUT} voltage is 5.0 V. Computed maximal T_J in application (based on max. power dissipation and cooling) is in this case higher, 125°C, to show the difference. Than maximal I_{ADJ} is at 125°C: I_{ADJ125} = 100 nA (based on Electrical characteristics table).



We chose:

$$I_{R2} = 100 \cdot I_{ADJ125} = 100 \cdot 100E{-}9 = 10\ \mu A$$

Then:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{1.2}{10E{-}6} = 120\ k\Omega$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{V_{OUT} - V_{R2}}{I_{ADJ125} + I_{R2}} = \frac{5 - 1.2}{100E{-}9 + 10E{-}6} = \frac{3.8}{10.1E{-}6} = 376.2\ k\Omega$$

Verification:

For low temperature (T_J = 25°C) the I_{ADJ25} = 1 nA:

$$V_{OUT} = V_{ADJ} \cdot \left(1 + \frac{R_{ADJ1}}{R_{ADJ2}}\right) + I_{ADJ} \cdot R_{ADJ1}$$

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 1E{-}9 \cdot 376.2E3 = 4.962\ V$$

For maximal temperature (T_J = 125°C) the I_{ADJ125} = 100 nA:

$$V_{OUT} = 1.2 \cdot \left(1 + \frac{376.2E3}{120E3}\right) + 100E{-}9 \cdot 376.2E3 = 5.000\ V$$

Output voltage error for temperatures 125°C to 25°C is:

$$\Delta V_{OUT} = \frac{V_{OUT125} - V_{OUT25}}{V_{OUT125}} \cdot 100 = \frac{5.000 - 4.962}{5.000} \cdot 100 = 0.76\%$$

Total circuit quiescent current at T_J = 25°C is:

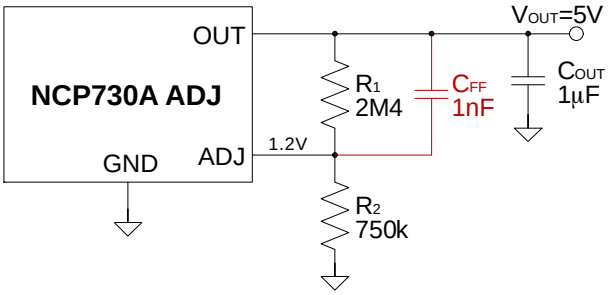
$$I_{Q(TOT)} = I_{Q(LDO)} + I_{R1} = 1.3E{-}6 + 10.1E{-}6 = 11.4\ \mu A!!!$$

We can see that error of V_{OUT} voltage is not too much higher than in example 1 but the current consumption of external resistor divider is almost 10−times the quiescent current of LDO so the total quiescent current of the circuit changed a lot.

C_{FF} Capacitor

Even the NCP730 is very low quiescent current device, both the load transients over/under shoots and settling times are excellent. See the Typical characteristics graphs.

At adjustable application, the external resistor divider with input ADJ pin capacity and ADJ pin PCB trace capacity to GND makes a low pass filter what affects the dynamic behavior of the LDO. On the next picture is shown how this unwanted side effect could be compensated by adding of feed−forward capacitor C_{FF} across R_1 resistor.



The value of the C_{FF} depends on R_1 and R_2 resistor values. When R_1, R_2 values are in hundreds of kiloohms, we propose the C_{FF} value to be about 1 nF, as shown on picture above, for the best dynamic performance. Generally, the value could be in range from 0 to 10 nF. At Typical characteristics section you can find load transient, PSRR and start−up pictures for different C_{FF} values.

Output Current Limit

Output current is internally limited to 280 mA typ. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is 90% of $V_{OUT-NOM}$). If the output voltage is shorted to ground, the device continues with current limitation at the same current level. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Minimal output current limit value is 200 mA what could be used to cover current demand peaks.

Thermal Shutdown

When the LDO's die temperature exceeds the thermal shutdown threshold value the device is internally disabled. The IC will remain in this state until the die temperature decreases by value called thermal shutdown hysteresis. Once the IC temperature falls this way, the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} = \frac{125 - T_A}{\theta_{JA}} \text{ [W]} \qquad \text{(eq. 2)}$$

Where: $(T_J - T_A)$ is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

For reliable operation junction temperature should be limited do +125°C.

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \text{ [W]} \qquad \text{(eq. 3)}$$

Where: I_{GND} is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and N/C pin to a large ground planes helps to dissipate the heat from the chip.

The relation of θ_{JA} and $P_{D(MAX)}$ to PCB copper area and Cu layer thickness could be seen on the Figures 27 and 28.

Power Supply Rejection Ratio

The LDO features high power supply rejection ratio even it is very low quiescent current device. See the Typical characteristics section for the graphs over different conditions.

The PSRR at higher frequencies (from about 100 kHz) can be tuned by the selection of C_{OUT} capacitor, applied input voltage and proper PCB layout (minimizing impedance from load to C_{OUT}).

PCB Layout Recommendations

To obtain good LDO's stability, transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors as close as possible to the device pins and make the PCB traces wide, short and place these components to the same layer as the LDO is (to avoid connection through vias). The same rules should be applied to the connections between C_{OUT} and the load – the less parasitic impedance the better transients and regulation.

To minimize the solution size, use 0402 or 0201 capacitor sizes with appropriate effective capacitance in mind.

Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Power Dissipation section). Both, exposed pad and N/C pins should be tied to the ground plane to improve power dissipation.

Regarding high impedance ADJ pin, prevent capacitive coupling of the trace to any switching signals in the circuitry.

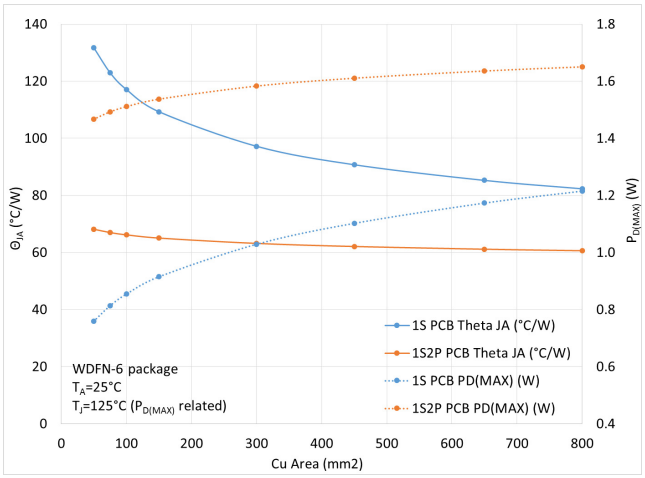


Figure 27. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

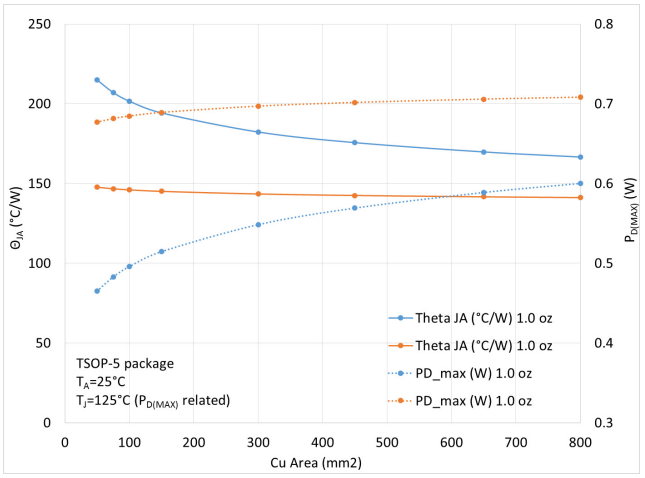


Figure 28. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

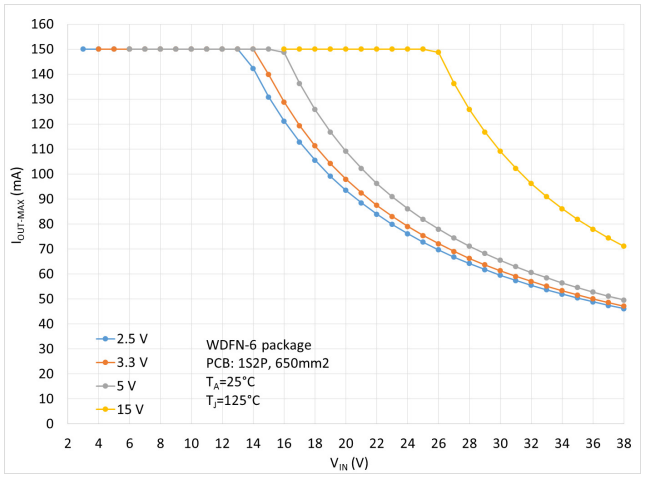


Figure 29. Maximum Output Current vs. Input Voltage

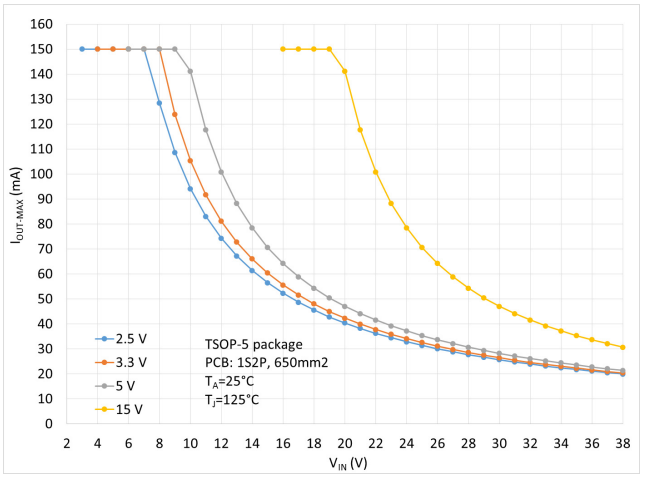


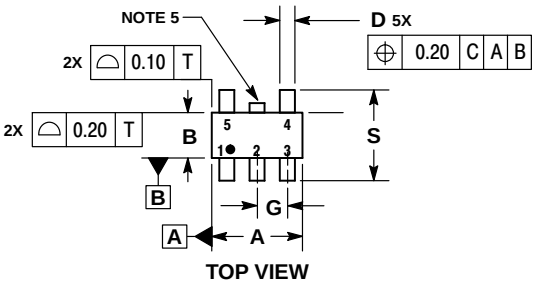
Figure 30. Maximum Output Current vs. Input Voltage

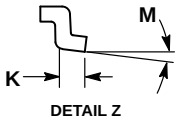
ORDERING INFORMATION

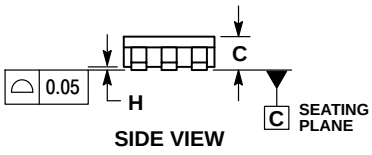
Part Number	Marking	Voltage Option ($V_{OUT-NOM}$)	Version	Package	Shipping
NCP730ASNADJT1G	HAA	ADJ	Without PG	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP730ASN250T1G	HAC	2.5 V			
NCP730ASN280T1G	HAD	2.8 V			
NCP730ASN300T1G	HAF	3.0 V			
NCP730ASN330T1G	HAE	3.3 V			
NCP730ASN500T1G	HAG	5.0 V			
NCP730BMTADJTBG	MA	ADJ	With PG	WDFN6 2x2 (Pb−Free)	3000 / Tape & Reel
NCP730BMT250TBG	MC	2.5 V			
NCP730BMT280TBG	MD	2.8 V			
NCP730BMT300TBG	ME	3.0 V			
NCP730BMT330TBG	MF	3.3 V			
NCP730BMT500TBG	MG	5.0 V			
NCP730BMT1500TBG	MH	15.0 V			

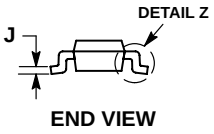
PACKAGE DIMENSIONS

TSOP−5
CASE 483
ISSUE M





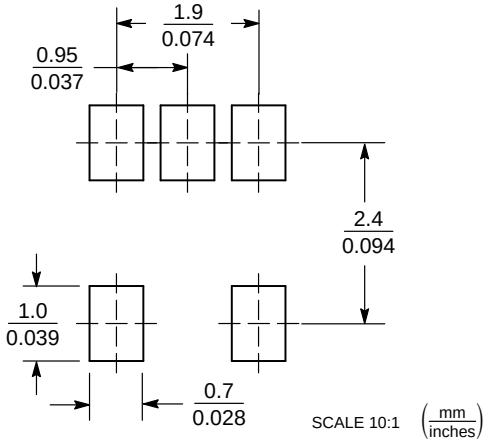




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

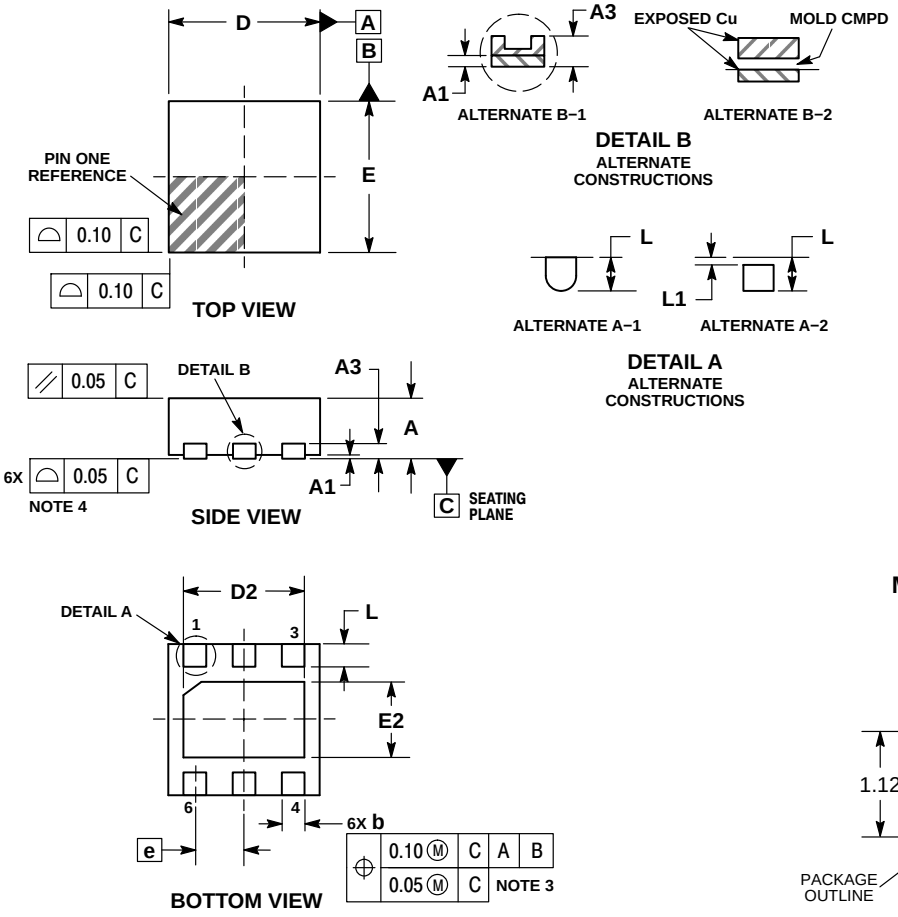
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

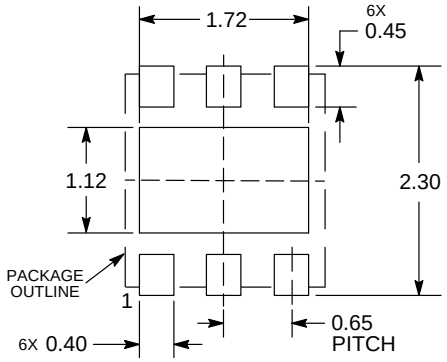
WDFN6 2x2, 0.65P
CASE 511BR
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICES CONTAINING WETTABLE FLANK OPTION, DETAIL A ALTERNATE CONSTRUCTION A−2 AND DETAIL B ALTERNATE CONSTRUCTION B−2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
L	0.20	0.40
L1	---	0.15

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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