NCP800

Lithium Battery Protection Circuit for One Cell Battery Packs

The NCP800 resides in a lithium battery pack where the battery cell continuously powers it. In order to maintain cell operation within specified limits, this protection circuit senses cell voltage and discharge current, and correspondingly controls the state of two, N−channel, MOSFET switches. These switches reside in series with the negative terminal of the cell and the negative terminal of the battery pack. During a fault condition, the NCP800 open circuits the pack by turning off one of these MOSFET switches, which disconnects the current path.

- Internally Trimmed Precision Charge and Discharge Voltage Limits
- Discharge Current Limit Detection
- Automatic Reset from Discharge Current Faults
- Low Current Standby State when Cells are Discharged
- Available in a Low Profile Surface Mount Package

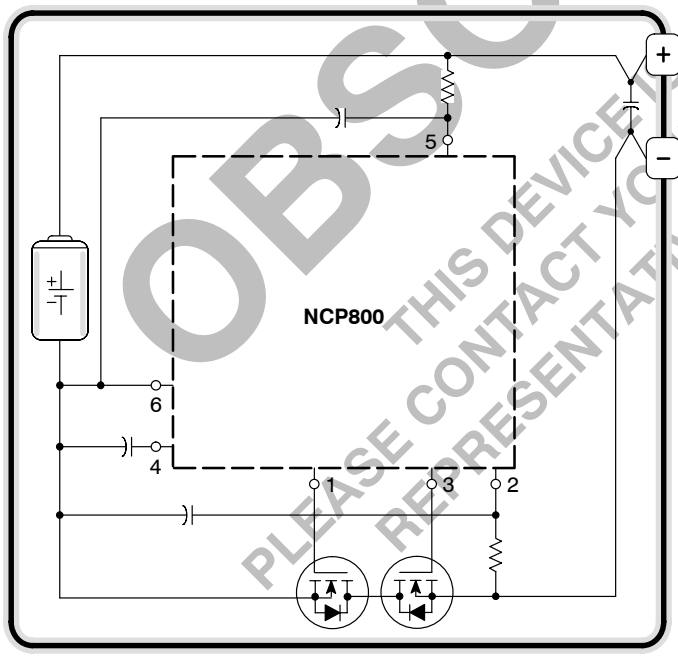
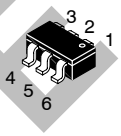


Figure 1. Typical One Cell Smart Battery Pack
This device contains 169 transistors.

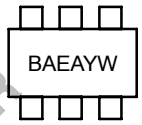
ON Semiconductor®

http://onsemi.com



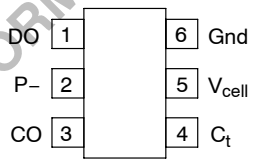
TSOP−6
SN SUFFIX
CASE 318G

MARKING DIAGRAM



BAE = Device Code
A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP800SN1T1	TSOP−6	3000 Units/Rail

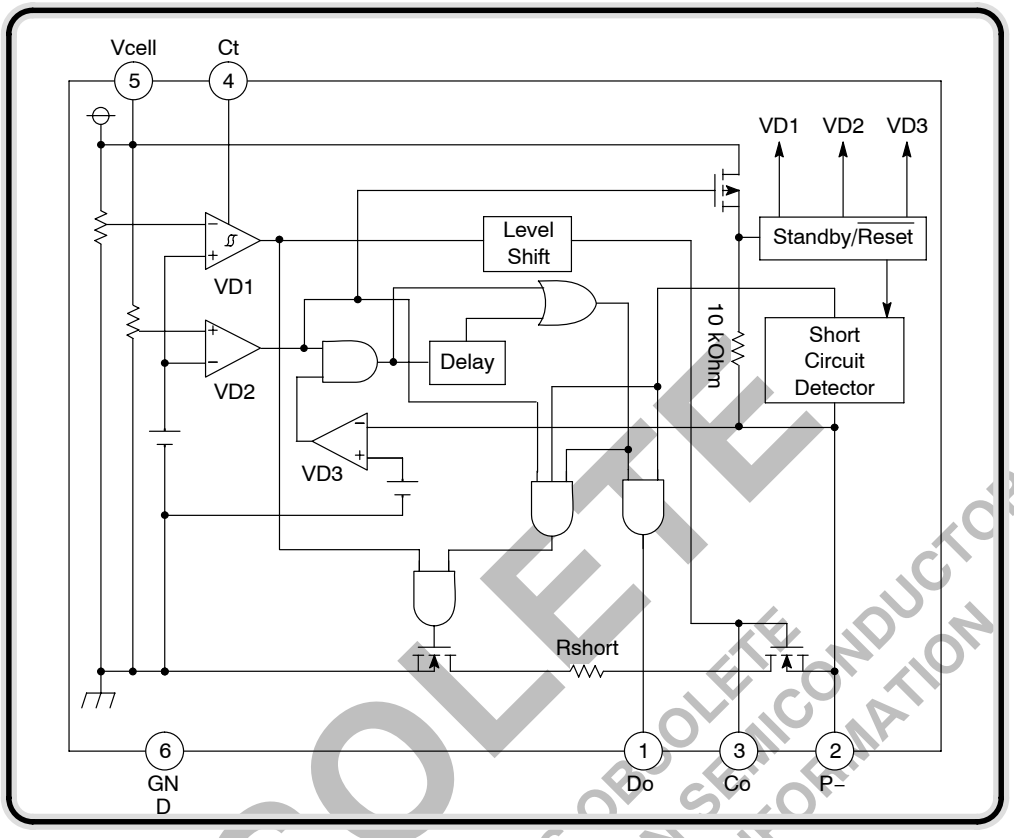


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	DO	This output connects to the gate of the discharge MOSFET allowing it to enable or disable battery pack discharging.
2	P−	This pin monitors cell discharge current. The excess current detector sets when the combined voltage drop of the charge MOSFET and the discharge MOSFET exceeds the discharge current limit threshold voltage, V(DET3). The short circuit detector activates when V(P−) is pulled within typically 0.85 V of the V_{cell} voltage. The CO driver is level shifted to the voltage at this pin.
3	CO	This output connects to the gate of the charge MOSFET switch Q1 allowing it to enable or disable battery pack charging.
4	C_t	This pin connects to the external capacitor for setting the output delay of the overvoltage detector (VD1).
5	V_{cell}	This input connects to the positive terminal of the cell for voltage monitoring and provides operating bias for the integrated circuit.
6	Gnd	This is the ground pin of the IC.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (Pin 5 to Pin 6)	V_{DD}	−0.3 to 12	V
Input Voltage Charge Gate Drive Common/Current Limit (Pin 5 to Pin 2) Overvoltage Delay Capacitor (Pin 4 to Pin 6)	 V_{P-} V_{Ct}	 V(pin5) + 0.3 to V(pin 5) − 8 0.3 to 12	V
Output Voltage CO Pin Voltage (Pin 3 to Pin 2) DO Pin Voltage (Pin 1 to Pin 6)	 V_{CO} V_{DO}	 V(pin5) + 0.3 to V(pin 5) − 8 −0.3 to 12	V
Thermal Resistance, Junction−to−Air SN Suffix, TSOP−6 Plastic Package, Case 318G	$R_{\theta JA}$	 250	°C/W
Operating Junction Temperature	T_J	−40 to 85	°C
Storage Temperature	T_{stg}	−55 to 125	°C

1. This device contains ESD protection:
   Human Body Model 2000 V.
   Machine Model Method 200 V.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Overvoltage Threshold, V_{DD} Increasing (Note 2) Overvoltage Hysteresis V_{DD} Decreasing	V_{DET1} V_{HYS1}	4.30 150	4.35 200	4.40 250	V mV
Overvoltage Delay Time C_t = 560 pF C_t = 0.01 μF	t_{DET1}	 2 –	 4 75	 6 –	ms
Undervoltage Threshold, V_{DD} Decreasing	V_{DET2}	2.437	2.5	2.563	V
Undervoltage Delay Time (V_{DD} = 3.6 V to 2.4 V)	t_{DET2}	7.0	11	13	ms
CURRENT SENSING					
Excess Current Threshold (Detect rising edge of P− pin voltage) (Note 3)	V_{DET3}	170	200	230	mV
Short Protection Voltage (V_{DD} = 3.0 V)	V_{SHORT}	V_{DD} − 1.1	V_{DD} − 0.85	V_{DD} − 0.5	V
Current Limit Delay Time (V_{DD} = 3.0 V)	t_{DET3} t_{SHORT}	9.0 –	14 10	17 –	ms μs
Reset Resistance	R_{SHORT}	50	100	150	kΩ
OUTPUTS					
Charge Gate Drive Output Low (Pin 3 to Pin 2) (V_{DD} = 4.4 V, Io = 50 μA)	V_{ol1}	–	0.16	0.5	V
Charge Gate Drive Output High (Pin 5 to Pin 3) (V_{DD} = 3.9 V, Io = −50 μA)	V_{oh1}	3.4	3.8	–	V
Discharge Gate Drive Output Low (Pin 1 to Pin 6) (V_{DD} = 2.4 V, Io = 50 μA)	V_{ol2}	–	0.1	0.5	V
Discharge Gate Drive Output High (Pin 5 to Pin 1) (V_{DD} = 3.9 V, Io = −50 μA)	V_{oh2}	3.4	3.8	–	V
TOTAL DEVICE					
Supply Current Operating (V_{DD} = 3.9 V, VP− = 0 V) Standby (V_{DD} = 2.0 V)	I_{cell}	 2.0 –	 4.0 0.3	 6.0 0.6	 μA μA
Operating Voltage	V_{DD}	1.5	–	10	V

2. Consult factory about other Overvoltage Threshold Options.
3. Consult factory about other Excess Current Threshold Options.

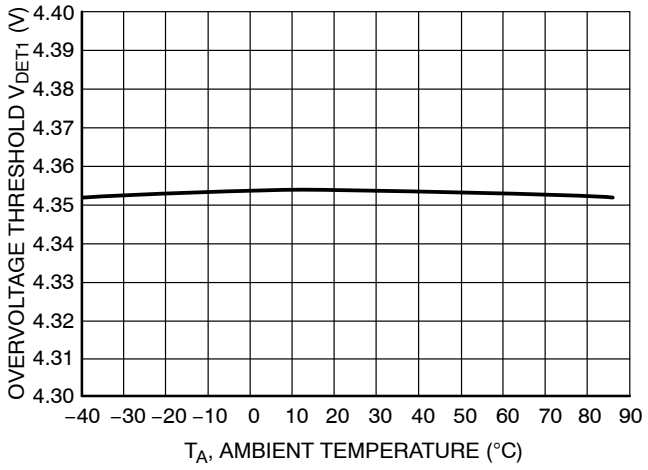


Figure 3. Overvoltage Threshold vs. Temperature

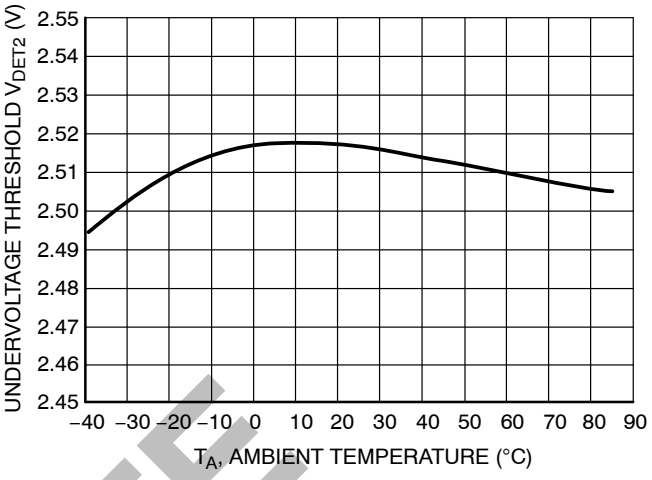


Figure 4. Undervoltage Threshold vs. Temperature

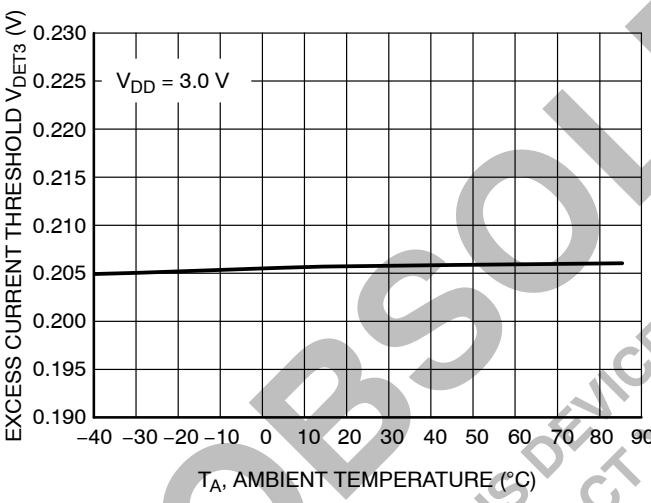


Figure 5. Excess Current Threshold vs. Temperature

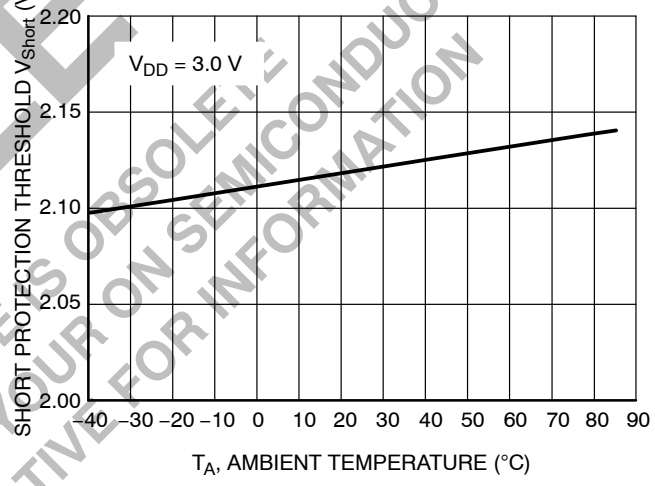


Figure 6. Short Protection Threshold vs. Temperature

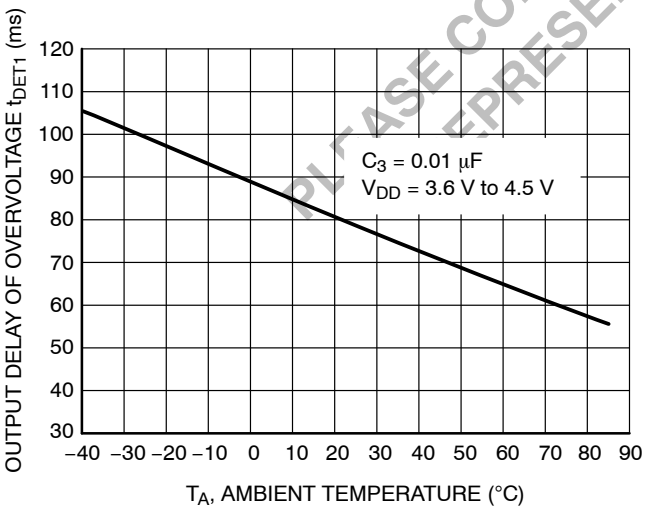


Figure 7. Output Delay of Overvoltage vs. Temperature

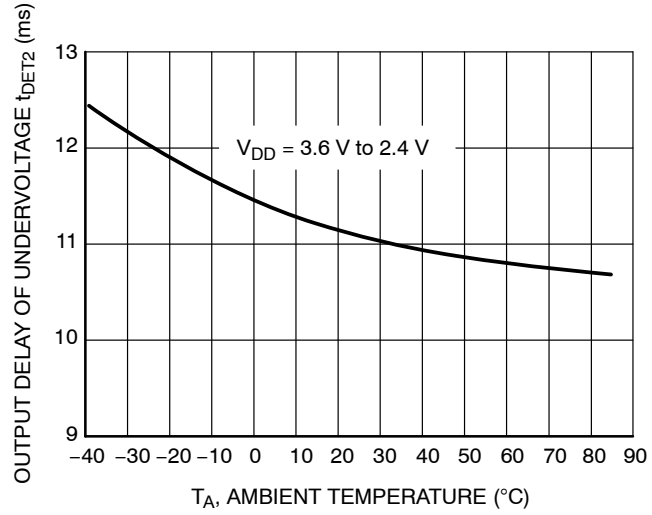


Figure 8. Output Delay of Undervoltage vs. Temperature

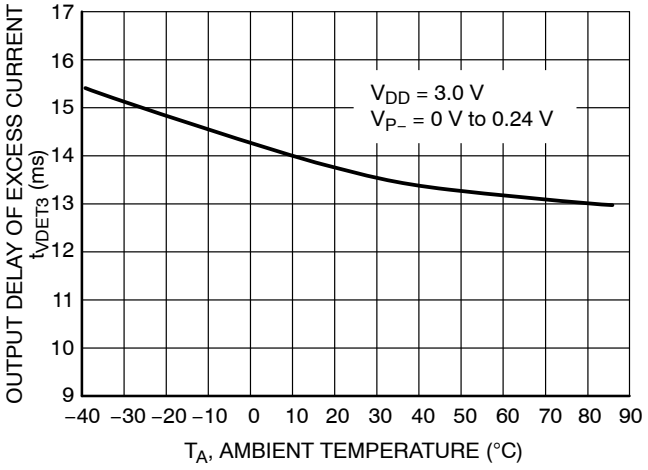


Figure 9. Output Delay of Excess Current vs. Temperature

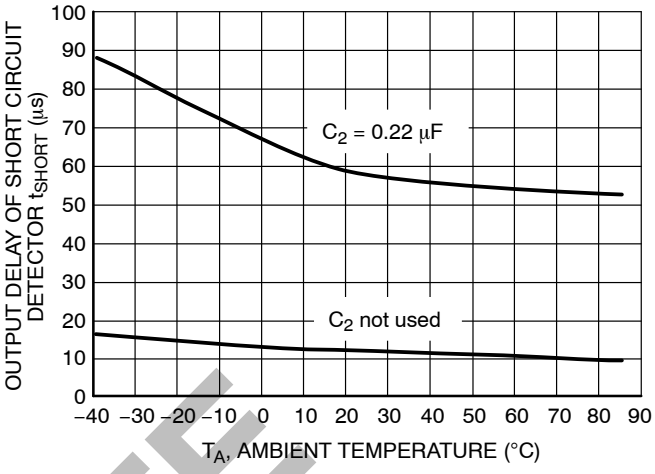


Figure 10. Output Delay of Short Circuit Detector vs. Temperature

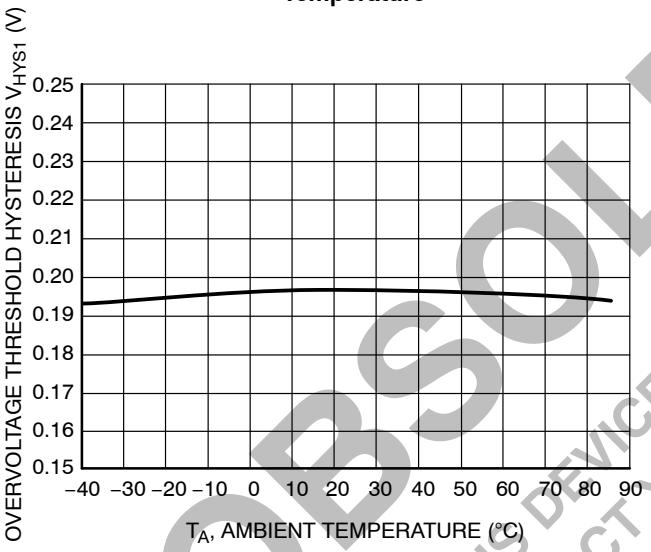


Figure 11. Overvoltage Threshold Hysteresis vs. Temperature

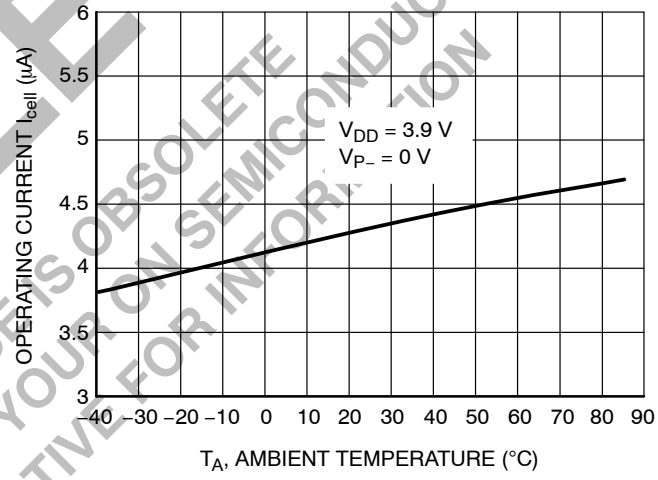


Figure 12. Operating Current vs. Temperature

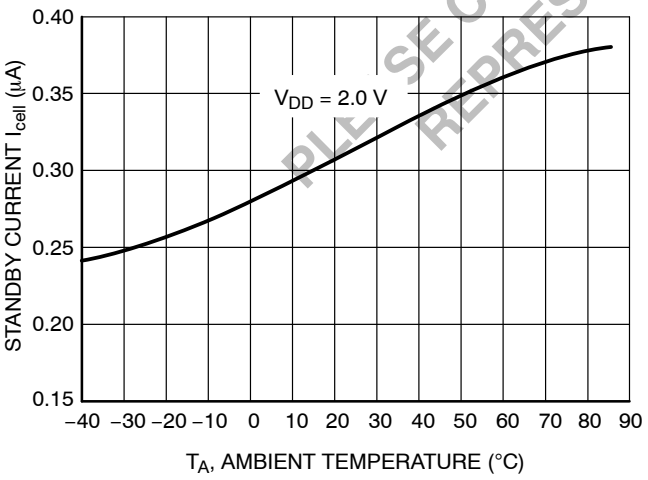


Figure 13. Standby Current vs. Temperature

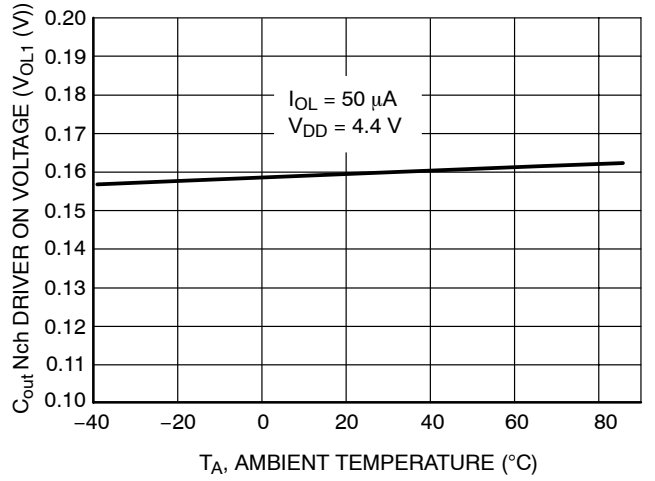


Figure 14. C_{out} Nch Driver On Voltage vs. Temperature

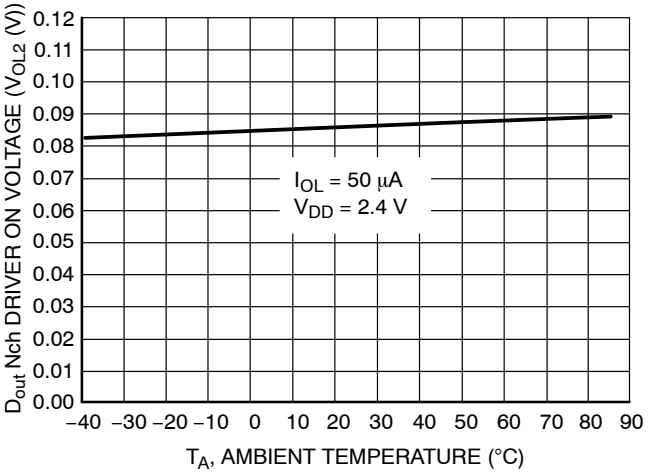


Figure 15. D_{out} Nch Driver On Voltage vs. Temperature

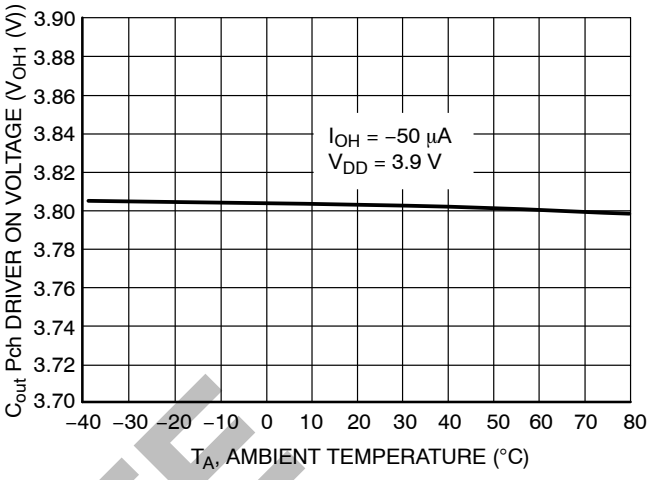


Figure 16. C_{out} Pch Driver On Voltage vs. Temperature

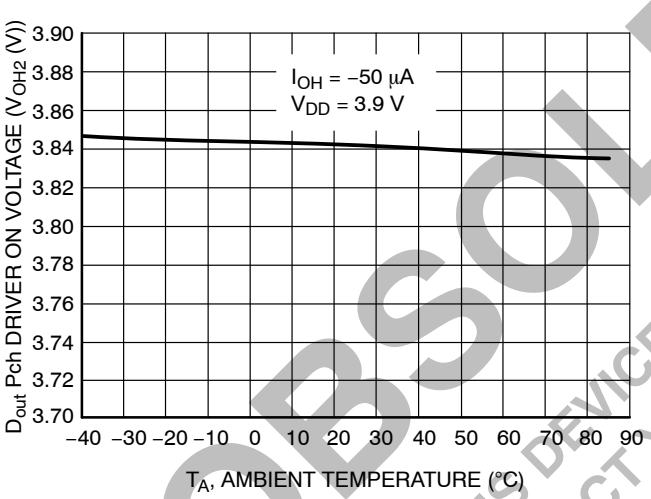


Figure 17. D_{out} Pch Driver On Voltage vs. Temperature

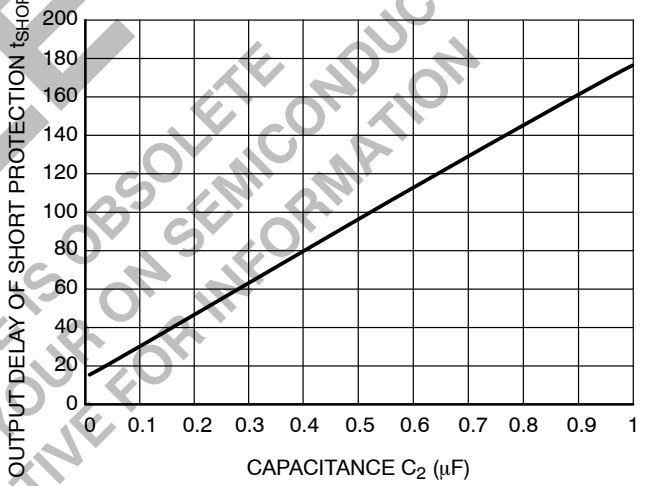


Figure 18. Short Protection Delay Time vs. Capacitance C_2

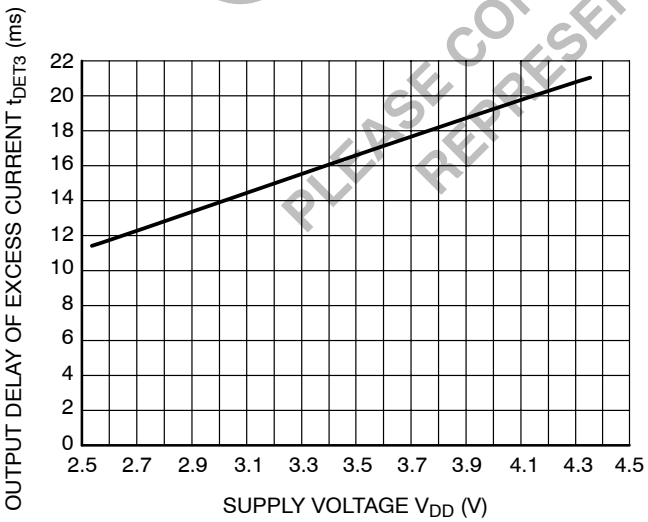


Figure 19. Excess Current Delay Time vs. V_{DD}

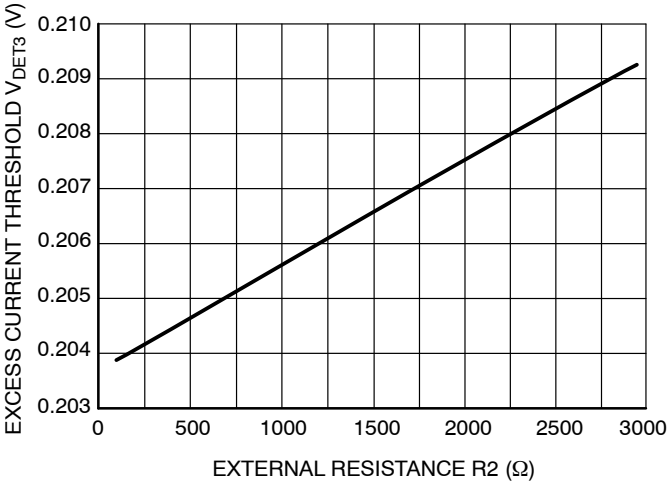


Figure 20. Excess Current Threshold vs. External Resistance R2

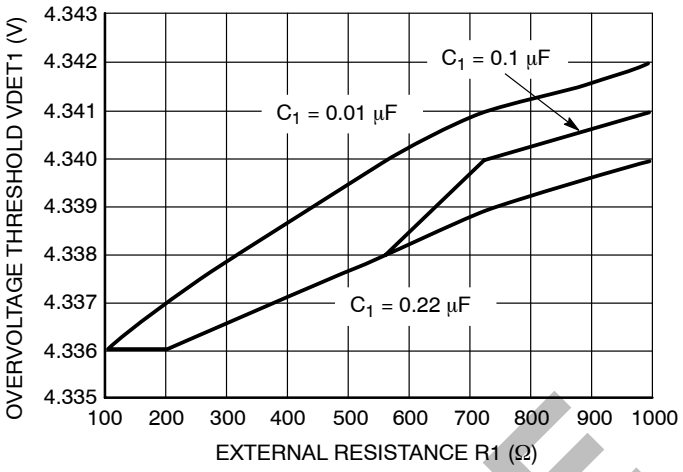


Figure 21. Overvoltage Threshold vs. External Resistance R1

OPERATING DESCRIPTION

VD1 / Over−Charge Detector

VD1 monitors the voltage at the V_{CELL} pin (V_{DD}). When it exceeds the over−charge detector threshold, V_{DET1}. VD1 senses an over−charging condition, the CO pin goes to a "Low" level, and the external charge control, Nch−MOSFET turns off.

Resetting VD1 allows resumption of the charging process. VD1 resets under two conditions, thus, making the CO pin level "High." The first case occurs when the cell voltage drops below "$V_{DET1}-V_{HYS1}$." (V_{HYS1} is typically 200 mV). In the second case, disconnecting the charger from the battery pack can reset VD1 after V_{DD} drops between "V_{DET1}" and "$V_{DET1}-V_{HYS1}$".

After detecting over−charge, connecting a load to the battery pack allows load current to flow through the parasitic diode of the external charge control FET. The CO level goes "High" when the cell voltage drops below V_{DET1} due to load current draw through the parasitic diode.

An external capacitor connected between the GND pin and Ct pin sets the output delay time for over−charge detection. The external capacitor sets up a delay time from the moment of over−charge detection to the time CO outputs a signal, which enables the charge control FET to turn off. If the voltage fault occurs within the time delay window. CO will not turn off the charge control FET. The output delay time can be calculated as follows:

$$t_{DET1}[sec] = (Ct[F] \times (VDD[V] - 0.7)/(0.48 \times 10^{-6})$$

A level shifter incorporated in a buffer driver for the CO pin drives the "Low" level of CO pin to the P− pin voltage. A CMOS buffer sets the "High" level of CO pin to V_{DD}.

VD2 / Over−Discharge Detector

VD2 monitors the voltage at the V_{CELL} pin (V_{DD}). When it drops below the over−discharge detector threshold, V_{DET2}, VD2 senses an over−discharge condition, the DO pin goes to a "Low" level, and the external discharge control Nch MOSFET turns off. The IC enters a low current standby mode after detection of an over−discharged voltage by VD2. Supply current then reduces to approximately 0.3 μA. During standby mode, only the charger detector operates.

VD2 can only reset after connecting the pack to a charger. While V_{DD} remains under the over−discharge detector threshold, V_{DET2}, discharge current can flow through the parasitic diode of the external discharge control FET. The DO level goes "High" when the cell voltage rises above V_{DET2} due to the charging current through the parasitic diode. Connecting a charger to the battery pack will instantly set DO "High" if this causes V_{DD} to rise above V_{DET2}.

Output delay time for the over−discharge detection (t_{DET2}) is fixed internally. If the voltage fault occurs within the time delay window, DO will not turn off the discharge control FET.

A CMOS buffer sets the output of the DO pin to a "High" level of V_{DD} and a "Low" level of GND.

VD3 / Excess Current Detector, Short Circuit Detector

Both the excess current detector and the short circuit detector can work when the two control FET's are on. When the voltage at the P− pin rises to a value between the short circuit protection voltage, V_{SHORT}, and the excess current threshold, V_{DET3}, the excess current detector operates. Increasing $V_{(P-)}$ higher than V_{SHORT} enables the short circuit detector. The DO pin then goes to a "Low" level, and the external discharge control Nch MOSFET turns off.

Output delay time for excess current detection (t_{DET3}) is fixed internally. If the excess current fault occurs within the time delay window, DO will not turn off the discharge control FET. However, when the short circuit protector is enabled, DO can turn off the discharge control FET. Its delay time is approximately 10 μs.

The P−pin has a built−in pull down resistor, typically 100 kΩ, which connects to the GND pin. Once an excess current or short circuit fault is removed, the internal resistor

pulls $V_{(P-)}$ to the GND pin potential. Therefore, the voltage from P− to GND drops below the current detection thresholds and DO turns the external MOSFET back on.

NOTE: If V_{DD} voltage is higher than the over−discharge voltage threshold, V_{DET2}, when excess current is detected the IC will not enter a standby mode. However, if V_{DD} is below V_{DET2} when excess current is detected, the IC will enter a standby mode. This will not occur when the short circuit detector activates.

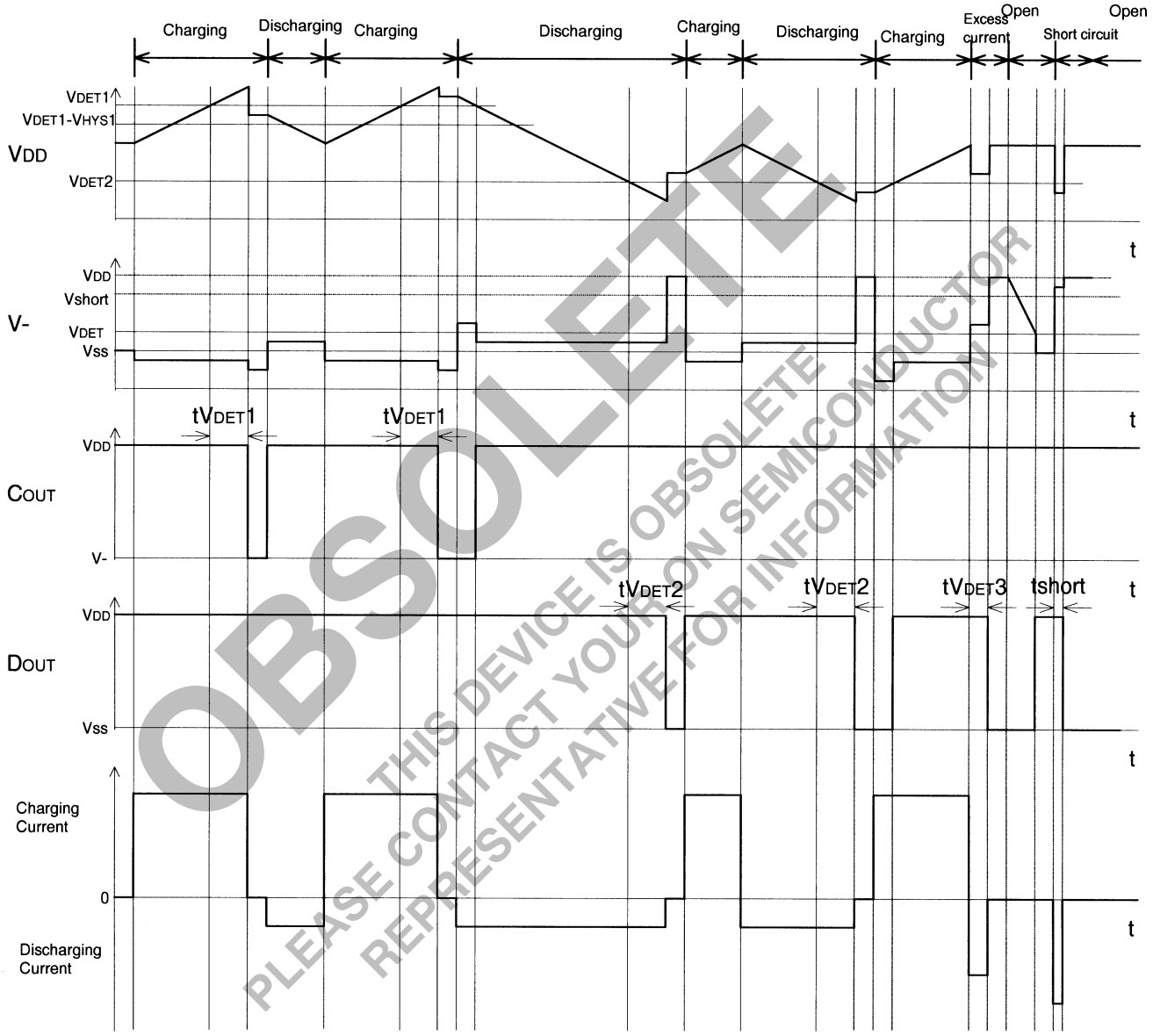


Figure 22. Timing Diagram / Operational Description

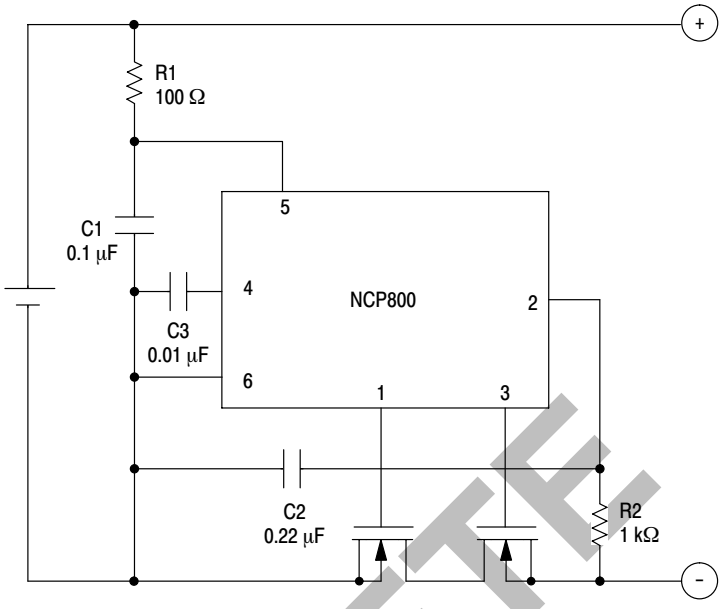


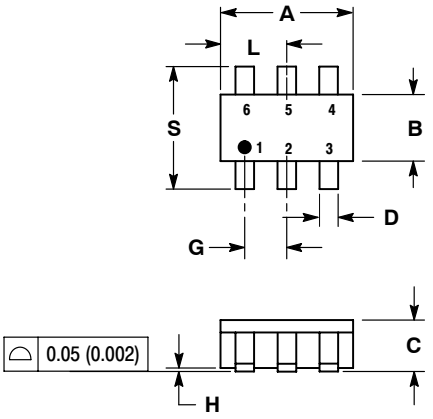
Figure 23. Typical Application Circuit

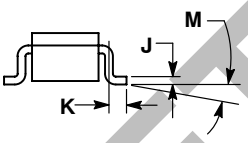
Technical Notes

R1 and C1 will stabilize a supply voltage to the NCP800. A recommended R1 value is less than 1 kΩ. A larger value of R1 leads to higher detection voltage because of shoot through current into the IC.
R2 and C2 stabilize P− pin voltage. Larger R2 values could possibly disable reset from over−discharge by connecting a charger. Recommended values are less than 1 kΩ. After an over−charge detection even connecting a battery pack to a system could probably not allow a system to draw load current if one uses a larger R2C2 time constant. The recommended C2 value is less than 1 μF.
R1 and R2 can operate as a current limiter against setting cell reverse direction or for applying excess charging voltage to the IC and battery pack. Smaller R1 and R2 values may cause excessive power consumption over the specified power dissipation rating. Therefore R1 + R2 should be more than 1 kΩ.
The time constants R1C1 and R2C2 must have a relation as follows:
$R1C1 \leq R2C2$
If the R1C1 time constant for the Vcell pin is larger than the R2C2 time constant for the P− pin, the IC might enter a standby mode after detecting excess current. This was noted in the operating description of the current detectors.

PACKAGE DIMENSIONS

TSOP−6
SN SUFFIX
CASE 318G−02
ISSUE H





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NCP800/D