# NCP81156

*Product Preview*

# MOSFET Driver

The NCP81156 is a high−performance dual MOSFET gate driver in a small 2 mm x 2 mm package, optimized to drive the gates of both high−side and low−side power MOSFETs in a buck or buck−boost application. VCC UVLO ensures the MOSFETs are off when supply voltages are low. A bi−directional Enable pin provides a fault signal to the controller when a UVLO fault is detected.

### Features

- Space−Efficient 2 mm x 2 mm DFN8 Thermally−Enhanced Package
- VCC Range of 4.5 V to 13.2 V
- Integrated Bootstrap Diode
- Compatible with 3.3 V and 5 V PWM Inputs
- Bi−Directional Enable Feature Pulls Enable Pin low during a UVLO Fault.
- Adaptive Anti−Cross Conduction Circuit Protects against Cross−Conduction during FET Turn−on and Turn−off
- Output Disable Control Turns Off Both MOSFETs
- VCC Under−voltage Lockout
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

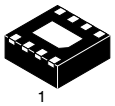
### Typical Applications

- E−Cigarettes
- Unmanned Aerial Vehicles (UAV)

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

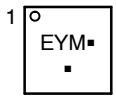
**ON Semiconductor®**

www.onsemi.com



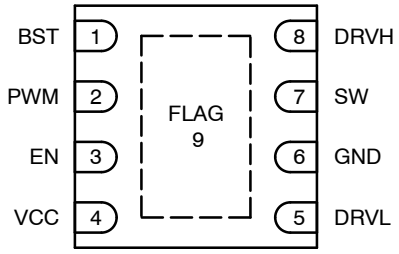

**DFN8**
**MN SUFFIX**
**CASE 506AA**

**MARKING DIAGRAM**




EY = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PINOUT DIAGRAM**




(Top View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NCP81156MNTBG | DFN8 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

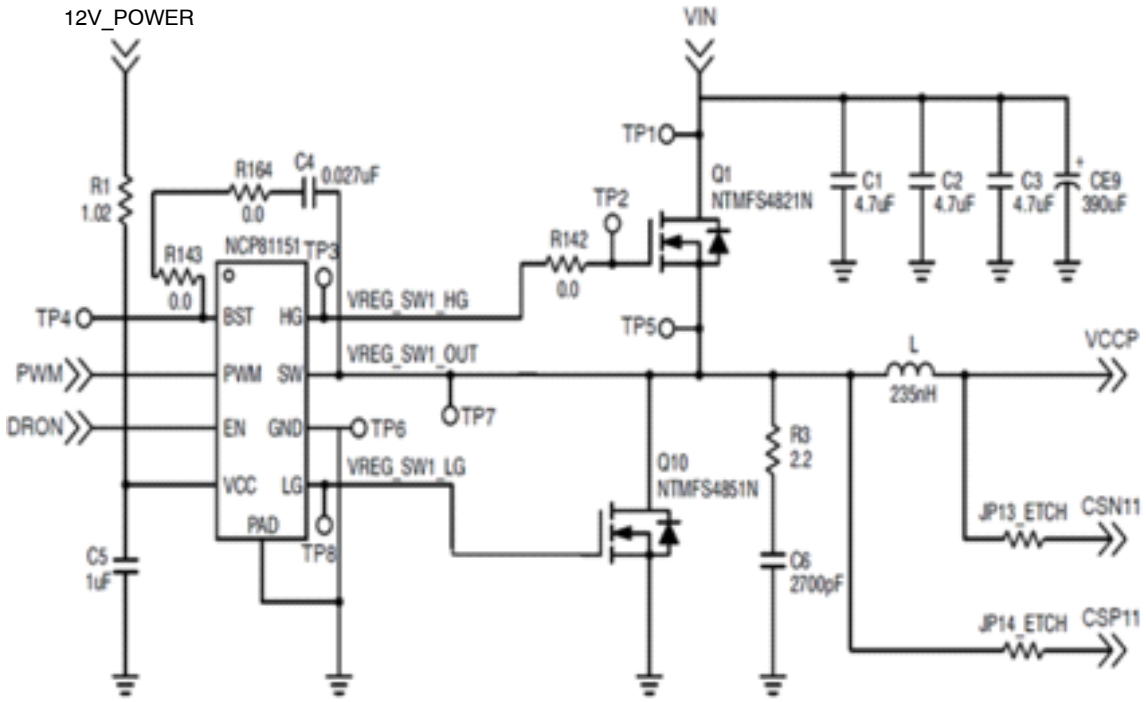



**Figure 1. Typical Application Schematic**

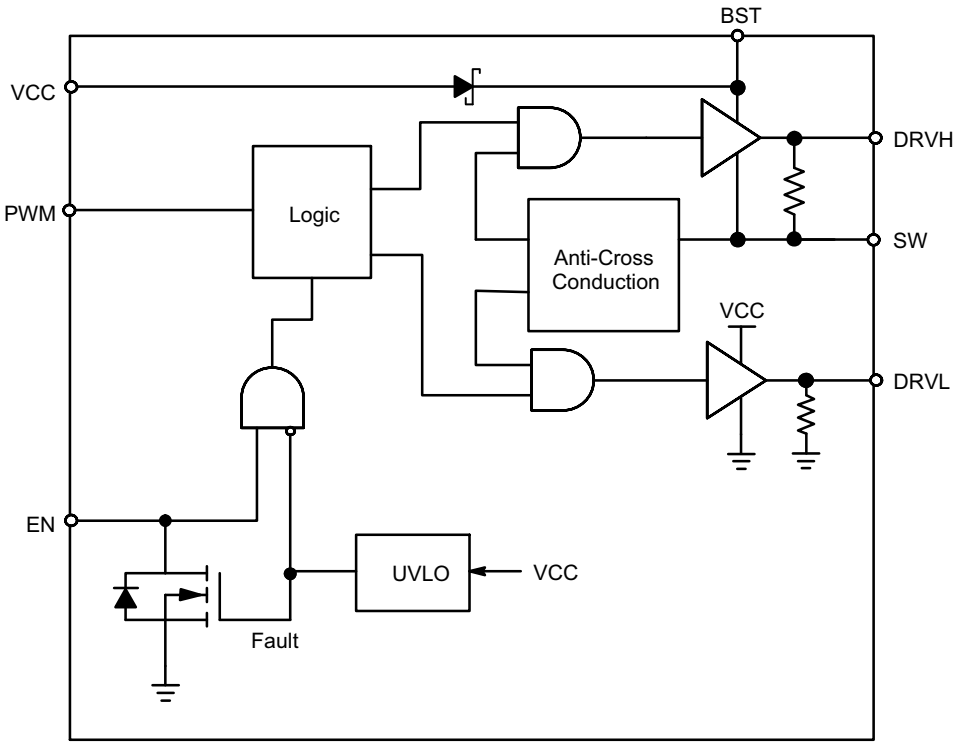



**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | BST | Bootstrap supply voltage. Connect a MLCC capacitor of at least 0.1μF from this pin to SW. |
| 2 | PWM | Two−state Input. |
| 3 | EN | Enable Input. |
| 4 | VCC | 5.0 V power supply for the control logic circuit. |
| 5 | DRVL | Low−side gate drive output. Connect to the gate of low−side MOSFET. |
| 6 | GND | Analog Ground. |
| 7 | SW | Switch−node Output. |
| 8 | DRVH | High−side gate drive output. Connect to the gate of high−side MOSFET. |
| 9 | FLAG | Thermal Flag. Connect to ground plane. |

**Table 2. ABSOLUTE MAXIMUM RATINGS** (Electrical Information − all signals referenced to GND unless noted otherwise.)

| Pin Symbol | Pin Name | VMAX | VMIN |
|---|---|---|---|
| VCC | Main Supply Voltage Input | 15 V<br>16 V (< 50 ns) | −0.3 V |
| BST | Bootstrap Supply Voltage | 35 V wrt/ GND<br>40 V ≤ 50 ns wrt/ GND 15 V wrt/ SW | −0.3 V wrt/SW |
| SW | Switching Node (Bootstrap Supply Return) | 35 V<br>40 V ≤ 50 ns | −5 V<br>−10 V (200 ns) |
| DRVH | High Side Driver Output | BST+0.3 V<br>SW + 15 V (< 80 ns) | −0.3 V wrt/SW<br>−2 V (<200 ns) wrt/SW |
| DRVL | Low Side Driver Output | VCC+0.3 V 15 V (< 80 ns) | −0.3 V DC<br>−5 V (<200 ns) |
| PWM | DRVH and DRVL Control Input | 6.5 V | −0.3 V |
| EN | Enable Pin | 6.5 V | −0.3 V |
| GND | Ground | 0 V | 0 V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. THERMAL INFORMATION**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance (Note 1) | $R_{\theta JA}$ | 74 | °C/W |
| Operating Junction Temperature Range | $T_J$ | −40 to +125 | °C |
| Operating Ambient Temperature Range | $T_A$ | −10 to +125 | °C |
| Storage Temperature Range | $T_{STG}$ | −55 to +150 | °C |
| Moisture Sensitivity Level − QFN Package | MSL | 1 | |

NOTE: These devices have limited built−in ESD protection. The devices should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the device.

1. Test board conditions:
   a. 1 inches x 1 inches Cu, 1 oz. thickness

**Table 4. ELECTRICAL CHARACTERISTICS**
($V_{VCC}$ = 4.5–13.2 V, $V_{BST}$ – $V_{SW}$ = 4.5–13.2 V, $V_{EN}$ = 5.0 V, $C_{VCC}$ = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCC** | | | | | | |
| Operating Voltage | $V_{VCC}$ | | 4.5 | – | 13.2 | V |
| Operating Current | | EN = 5 V, PWM = 100 kHz | – | 10 | – | mA |
| Enabled Current, No Switching | | EN = 5 V, PWM = 0 V | – | 2 | – | mA |
| | | EN = 5 V, PWM = 5 V | – | 2 | – | mA |
| Disabled Current | | EN = 0 V | – | 0.5 | 1.4 | mA |
| UVLO Threshold | $V_{UVLO}$ | VCC rising | 3.8 | 4.35 | 4.5 | V |
| UVLO Hysteresis | | | 150 | 200 | 250 | mV |
| **EN INPUT** | | | | | | |
| Upper Threshold | $V_{UPPER}$ | | 2 | – | – | V |
| Lower Threshold | $V_{LOWER}$ | | – | – | 1 | V |
| Hysteresis | | $V_{UPPER} - V_{LOWER}$ | – | 500 | – | mV |
| Enable Delay Time | $tpd_{EN\_HI}$ | PWM = 0 V, EN pin transitioning from 0 V to High to DRVL rising to 10% | – | 20 | 40 | ns |
| Pin Sink Current | | | 4 | – | 30 | mA |
| Input Bias Current | | | –1 | – | 1 | μA |
| **PWM INPUT** | | | | | | |
| Input High Voltage | $V_{PWM\_HI}$ | | 2 | – | – | V |
| Input Low Voltage | $V_{PWM\_LO}$ | | – | – | 0.8 | V |
| **DRVH ($V_{VCC}$ = 12 V)** | | | | | | |
| Output Impedance, Sourcing Current | | $V_{BST} - V_{SW}$ = 12 V | – | 1.9 | 3 | Ω |
| Output Impedance, Sinking Current | | $V_{BST} - V_{SW}$ = 12 V | – | 1 | 1.7 | Ω |
| Rise Time | $t_{rDRVH}$ | 3 nF Load | – | 16 | 30 | ns |
| Fall Time | $t_{fDRVH}$ | 3 nF Load | – | 11 | 25 | ns |
| Turn−Off Propagation Delay | $tpdl_{DRVH}$ | 3 nF Load | 8 | 13 | 30 | ns |
| Turn−On Propagation Delay | $tpdh_{DRVH}$ | 3 nF Load | – | – | 30 | ns |
| DRVH Pulldown Resistance | | From DRVH to SW | – | 37.5 | – | kΩ |
| **DRVH ($V_{VCC}$ = 5 V)** | | | | | | |
| Output Impedance, Sourcing Current | | $V_{BST} - V_{SW}$ = 5 V | – | 2.5 | – | Ω |
| Output Impedance, Sinking Current | | $V_{BST} - V_{SW}$ = 5 V | – | 1.6 | – | Ω |
| Rise Time | $t_{rDRVH}$ | 3 nF Load | – | 30 | – | ns |
| Fall Time | $t_{fDRVH}$ | 3 nF Load | – | 27 | – | ns |
| Turn−Off Propagation Delay | $tpdl_{DRVH}$ | 3 nF Load | – | 20 | – | ns |
| Turn−On Propagation Delay | $tpdh_{DRVH}$ | 3 nF Load | – | 27 | – | ns |
| DRVH Pulldown Resistance | | From DRVH to SW | – | 37.5 | – | kΩ |
| **DRVL ($V_{VCC}$ = 12 V)** | | | | | | |
| Output Impedance, Sourcing Current | | | – | 2 | 3 | Ω |
| Output Impedance, Sinking Current | | | – | 0.7 | 1.5 | Ω |
| Rise Time | $t_{rDRVL}$ | 3 nF Load | – | 16 | 35 | ns |
| Fall Time | $t_{fDRVL}$ | 3 nF Load | – | 11 | 20 | ns |
| Turn−Off Propagation Delay | $tpdl_{DRVL}$ | 3 nF Load | – | 15 | 35 | ns |

**Table 4. ELECTRICAL CHARACTERISTICS**
($V_{VCC}$ = 4.5−13.2 V, $V_{BST}$ − $V_{SW}$ = 4.5−13.2 V, $V_{EN}$ = 5.0 V, $C_{VCC}$ = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ $T_J$ ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRVL ($V_{VCC}$ = 12 V)** | | | | | | |
| Turn−On Propagation Delay | $tpdh_{DRVL}$ | 3 nF Load | 8 | – | 30 | ns |
| DRVL Pulldown Resistance | | From DRVH to SW | – | 37.5 | – | kΩ |
| **DRVL ($V_{VCC}$ = 5 V)** | | | | | | |
| Output Impedance, Sourcing Current | | | – | 2.5 | – | Ω |
| Output Impedance, Sinking Current | | | – | 1 | – | Ω |
| Rise Time | $t_{rDRVL}$ | 3nF Load | – | 30 | – | ns |
| Fall Time | $t_{fDRVL}$ | 3nF Load | – | 22 | – | ns |
| Turn−Off Propagation Delay | $tpdl_{DRVL}$ | 3nF Load | – | 22 | – | ns |
| Turn−On Propagation Delay | $tpdh_{DRVL}$ | 3nF Load | – | 12 | – | ns |
| DRVL Pulldown Resistance | | From DRVH to SW | – | 37.5 | – | kΩ |
| **SW** | | | | | | |
| SW Node Leakage Current | | | – | – | 20 | μA |
| **BOOTSTRAP DIODE** | | | | | | |
| Forward Voltage | $V_F$ | $V_{VCC}$ = 12 V, Forward Bias Current = 2.0 mA | 0.1 | 0.4 | 0.6 | V |

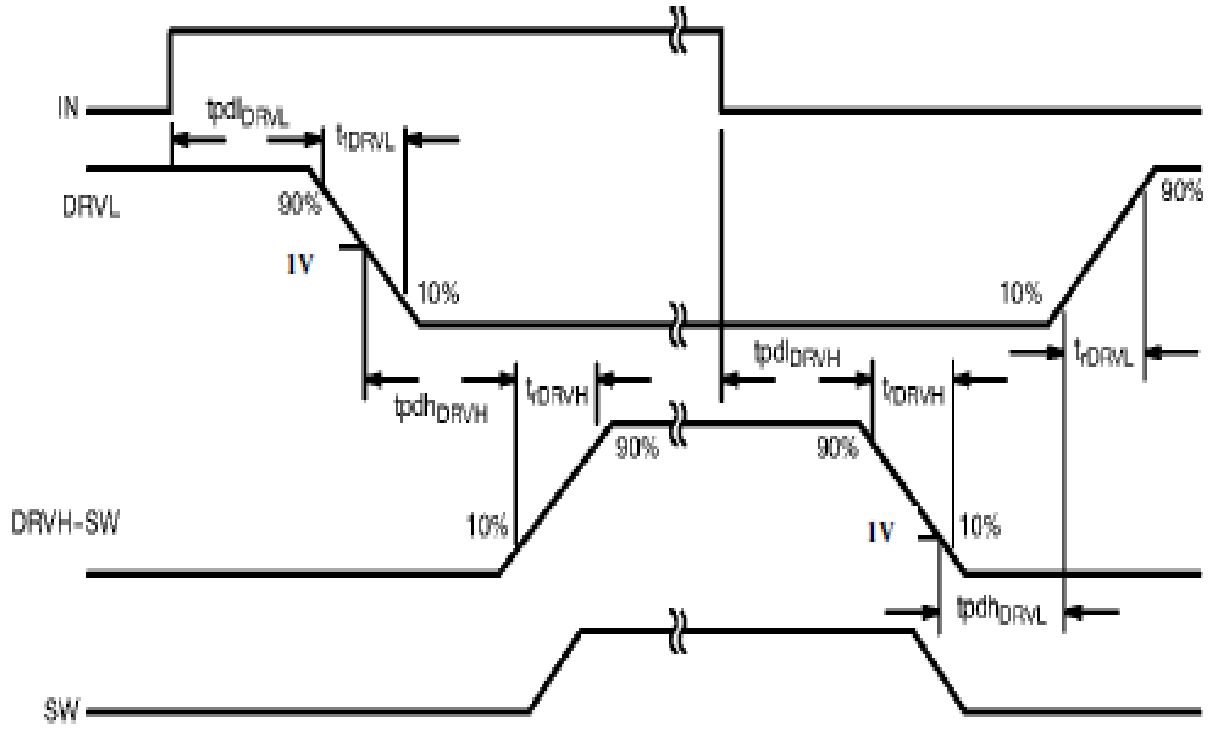



**Figure 3. Timing Diagram**

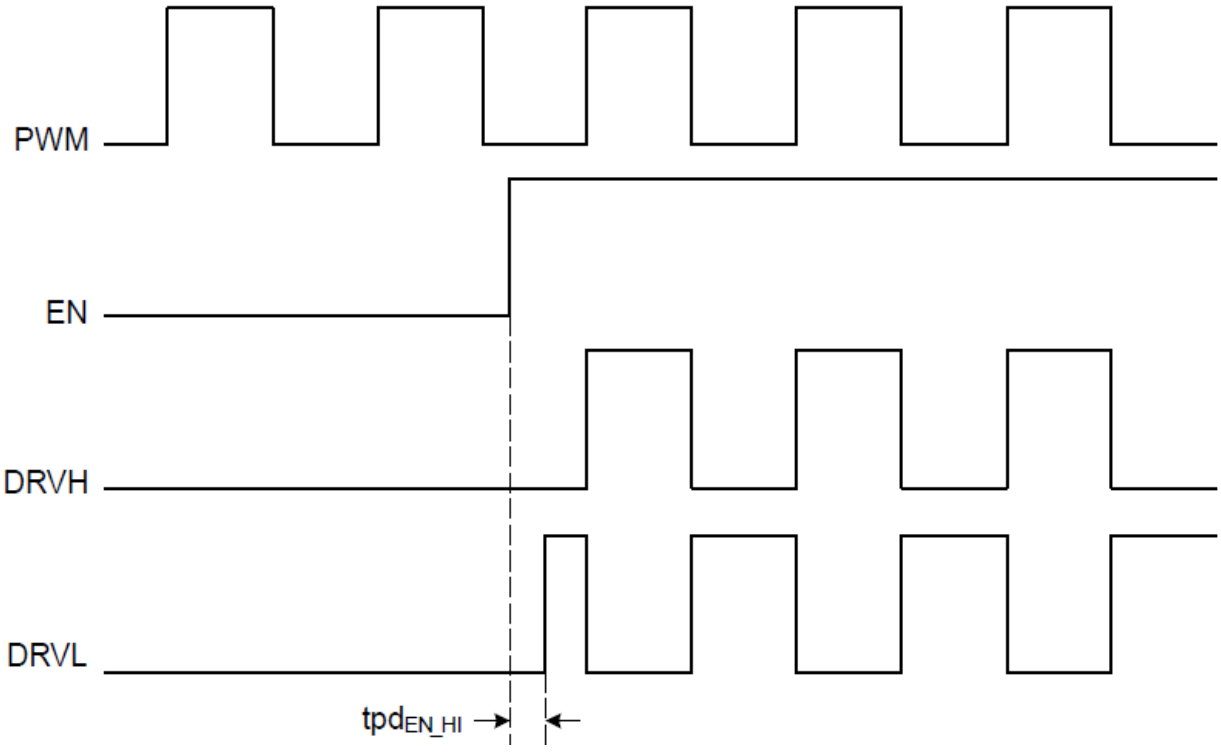



**Figure 4. PWM/EN Logic Diagram**

## Application Information

The NCP81156 is a dual MOSFET gate driver optimized to drive the gates of both high−side and low−side power MOSFETs in a Synchronous Buck Converter. The NCP81156 is a 2 mm x 2 mm DFN8 version of NCP81155.

### High−Side Driver

The high−side driver drives an external N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of an internal diode and an external bootstrap capacitor. When the NCP81156 is starting up, the SW pin is at ground, so the bootstrap capacitor charges up to VCC through the bootstrap diode (see Figure 1). When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the SW pin rises. When the high−side MOSFET is fully on, the SW voltage equals the VIN voltage, with the BST voltage higher than VCC by the amount of voltage on the bootstrap capacitor. The bootstrap capacitor is recharged when the switch- node goes low during the next cycle.

Parasitic inductances and capacitances within the packaging and MOSFETs can cause significant ringing of the SW signal during turn−on and turn−off of the high−side MOSFET. When operating at high input voltages and high output currents, the peak ringing voltages on SW could cause the drain−to−source voltage across the MOSFETs to exceed its maximum rating. Including a resistor in series with the bootstrap capacitor can reduce the peak SW ringing voltages. A resistor value of 4 Ω is recommended when operating at VIN voltages greater than 16 V.

### Low−Side Driver

The low−side driver drives an external ground−referenced N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCC and GND.

### Power Supply Decoupling

The NCP81156 SW pin sources relatively large currents across the drain−source of the MOSFETs. In order to maintain a constant and stable supply voltage (VCC) – a low ESR capacitor should be placed near the power and ground pins. A 1 μF to 4.7 μF multi−layer ceramic capacitor (MLCC) should be placed between VCC pins and GND.

### Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value of at least 0.1 μF should be used as the bootstrap capacitor. The bootstrap capacitor should have a minimum voltage rating of 35 V. As the voltage across the bootstrap capacitor is equal to voltage across VIN and GND and the charge stored during when low–side MOSFET is ON. A 4 Ω resistor in series with CBST is recommended to decrease VSW overshoot.

### Overlap Protection Circuit

As PWM transitions between the logic high and logic low states, the driver circuitry prevents both MOSFETs from being on at the same time which could result in a damage to the device. The NCP81156 prevents cross−conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap (NOL) time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). The control circuitry monitors the gate−source voltage of both MOSFETs and the SW pin voltage in order to determine the conduction status of the MOSFETs. For example, when the PWM input is driven high, the gate−source voltage of the low–side MOSFET will go low after a propagation delay. Then, the internal timer will turn–on and delay the turn–on of the high–side MOSFET. An important point to note is that the time it takes for both the MOSFETs to turn–off is dependent on the capacitance on the gate.

### Under−voltage Lockout (UVLO)

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH and DRVL to prevent the gates of the MOSFETs from accumulating enough charge to turn–on when the driver is powered off.

### Enable Input (EN)

The EN pin disables the high−side MOSFET – if the pin is pulled low in order to prevent power transfer. When EN is above the 2 V threshold, DRVH and DRVL change their states according to the PWM input. A UVLO fault turns on the internal MOSFET that pulls the EN pin towards ground. By connecting EN to the DRON pin of a controller, the controller is alerted when the driver encounters a fault condition.

### Thermal Considerations

As power in the NCP81156 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81156 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81156 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

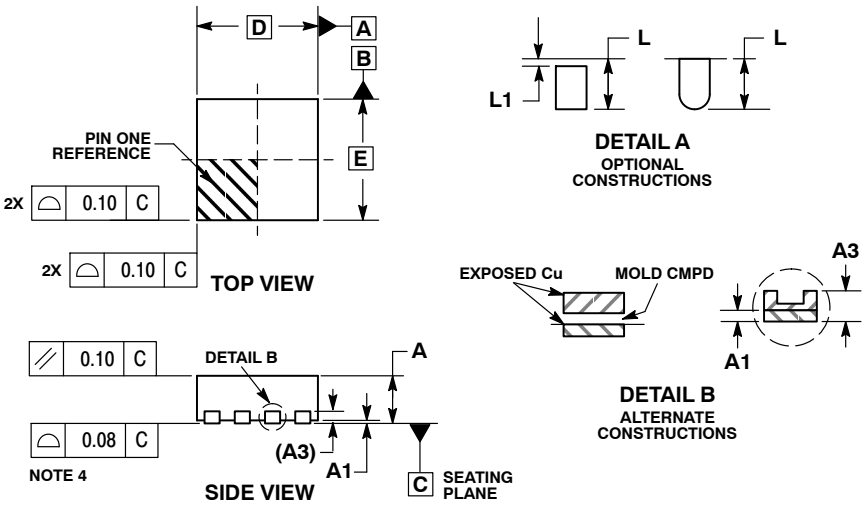
Since $T_J$ is not recommended to exceed 125°C, the NCP81156, soldered on to a 645 $mm^2$ copper area, using 1 oz. copper and FR4, can dissipate up to 2.3 W when the ambient temperature ($T_A$) is 25°C. The power dissipated by the NCP81156 can be calculated from the following equation:

$$P_D \cong V_{CC} \times \left[(n_{HS} \times Qg_{HS} \times n_{LS} \times Qg_{LS}) \times f + I_{STANDBY}\right] \quad \text{(eq. 2)}$$

Where $n_{HS}$ and $n_{LS}$ are the number of high−side and low−side FETs, respectively, $Qg_{HS}$ and $Qg_{LS}$ are the gate charges of the high−side and low−side FETs, respectively and *f* is the switching frequency of the converter.

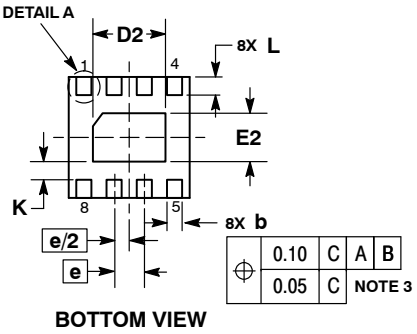
## PACKAGE DIMENSIONS

**DFN8 2x2, 0.5P**
CASE 506AA
ISSUE F

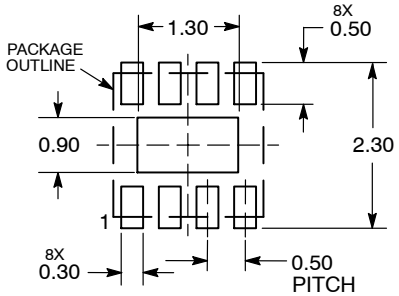



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |




### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative