NCP81220

Dual Output 4 & 2 Phase Controller with SVID Interface for Desktop and Notebook CPU Applications

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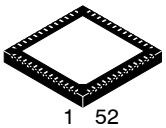
The NCP81220 dual output four plus two phase buck solution is optimized for Intel's IMVP8 CPUs. The controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed−forward, and adaptive voltage positioning to provide accurately regulated power for notebook applications.

The control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing providing an ultra fast initial response to dynamic load events and reduced system cost. The NCP81220 provides the mechanism to shed phases during light load operation and can auto frequency scale in light load conditions while maintaining excellent transient performance.

Dual high performance operational error amplifiers are provided to simplify compensation of the complete system. Patented Dynamic Reference Injection further simplifies loop compensation by eliminating the need to compromise between closed−loop transient response and Dynamic VID performance. Patented Total Current Summing provides highly accurate current monitoring for droop and digital current monitoring.



QFN52
MN SUFFIX
CASE 485BE

MARKING DIAGRAM

NCP81220 = Specific Device Code
F = Wafer Fab Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81220MNTXG	QFN52 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Features

- Meets Intel's IMVP8 Specification
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- Dual High Performance Operational Error Amplifier
- One Digital Soft Start Ramp for Both Rails
- Dynamic Reference Injection
- Accurate Total Summing Current Amplifier
- DAC with Droop Feed−forward Injection
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase−to−Phase Dynamic Current Balancing
- "Lossless" DCR Current Sensing for Current Balancing
- Pb−free and Halide−free Packages are Available
- Summed Compensated Inductor Current Sensing for Droop
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 180 KHz – 1.17 MHz
- Startup into Pre−Charged Loads while Avoiding False OVP
- Power Saving Phase Shedding
- Vin Feed Forward Ramp Slope
- Over Voltage Protection (OVP) & Under Voltage Protection (UVP)
- Over Current Protection (OCP)
- Dual Power Good Output with Internal Delays

Applications

- IMVP8 Desktop
- Gaming

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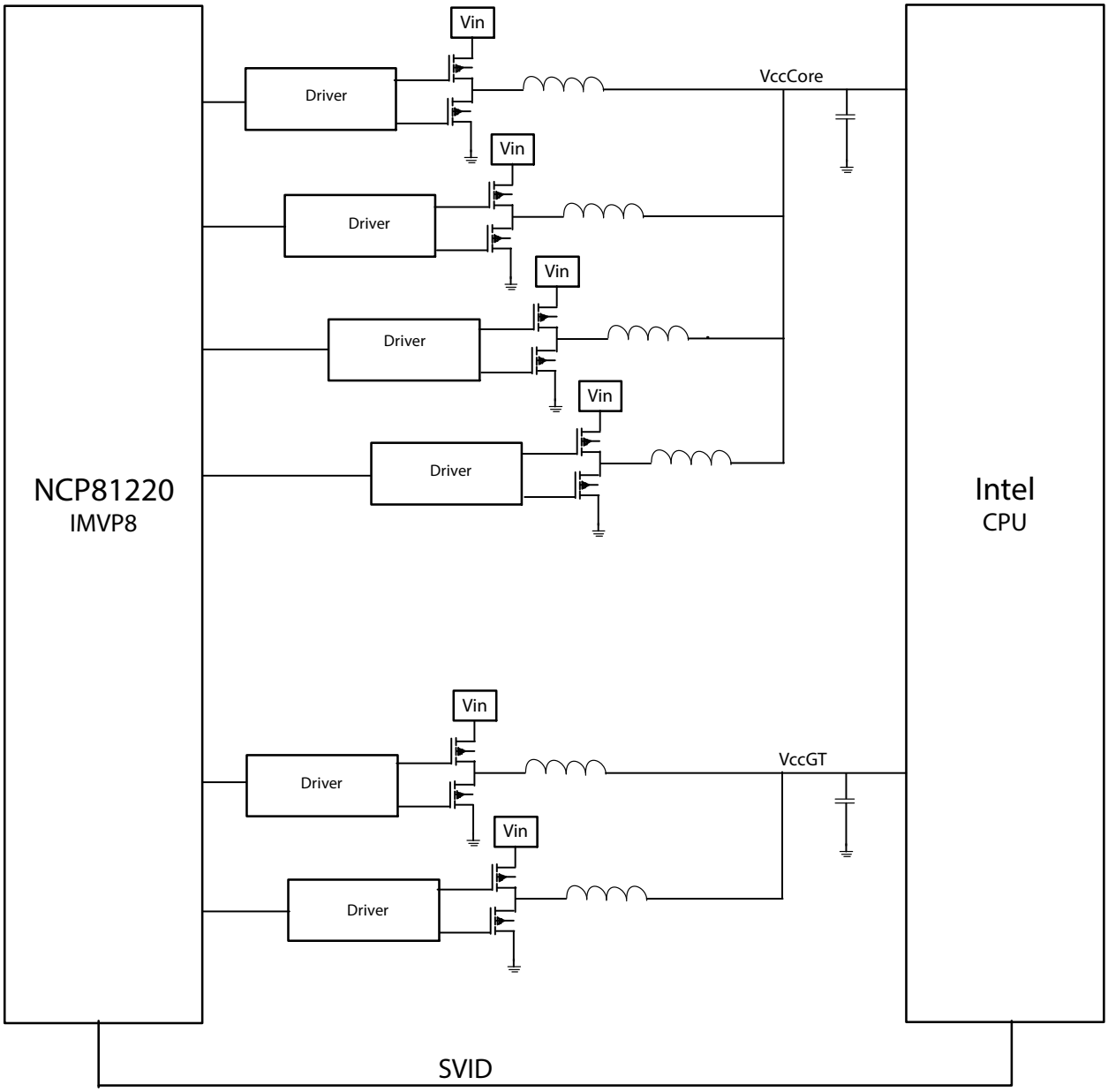

Figure 1. Block Diagram

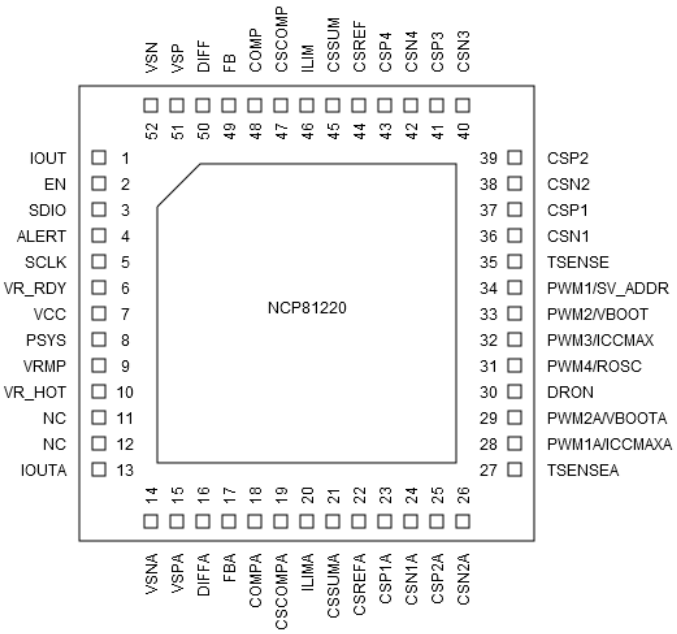

Table 1. QFN52 PIN DESCRIPTION

Pin No.	Symbol	Description
1	IOUT	Total output current monitor for four−phase regulator
2	EN	Enable. High enables both rails
3	SDIO	Serial VID data interface
4	ALERT	Serial VID ALERT
5	SCLK	Serial VID clock
6	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
7	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
8	PSYS	System power signal input
9	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes
10	VR_HOT	OD output. Indicates high VR temperature threshold crossed
11	NC	
12	NC	
13	IOUTA	Total output current monitor for two−phase regulator
14	VSNA	Differential output voltage positive sense for two−phase rail
15	VSPA	Differential output voltage negative sense for two−phase rail
16	DIFFA	Output of the two−phase regulator□s differential remote sense amplifier
17	FBA	Error amplifier voltage feedback for two−phase regulator
18	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators for two−phase regulator
19	CSCOMPA	Output of total−current−sense amplifier for two−phase regulator
20	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA for two−phase regulator
21	CSSUMA	Inverting input of total−current−sense amplifier for two−phase regulator
22	CSREFA	Total−current−sense amplifier reference voltage input for two−phase regulator
23	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 of two−phase regulator.
24	CSN1A	Inverting input to the current−balance amplifier for Phase 1 of two−phase regulator.

Table 1. QFN52 PIN DESCRIPTION

Pin No.	Symbol	Description
25	CSP2A	Non−inverting input to current−balance amplifier for Phase 2 of the two−phase regulator. Pull this pin to Vcc to disable Phase 2.
26	CSN2A	Inverting input to the current−balance amplifier for Phase 2 of the two−phase regulator
27	TSENSEA	Temperature sense input for two−phase regulator
28	PWM1A / ICCMAXA	PWM1 output for two−phase regulator During startup, ICCMAX for two−phase regulator is programmed with a pull−down resistor
29	PWM2A / VBOOTA	PWM2 output for two−phase regulator Pin−program for two−phase Vboot.
30	DRON	External FET driver enable for discrete driver or ONSemi DrMOS
31	PWM4 / ROSC	PWM4 output for four−phase regulator / Pulldown on this pin programs the operating frequency for both rails
32	PWM3 / ICCMAX	PWM3 output for four−phase regulator / Pulldown on this pin programs ICCMAX for four−phase rail during startup
33	PWM2 / VBOOT	PWM2 output for four−phase regulator / Pin−program for four−phase Vboot.
34	PWM1 / SV_ADDR	PWM1 output for four−phase regulator / Pulldown on this pin configures SVID address
35	TSENSE	Temperature sense input for four−phase regulator
36	CSN1	Differential current sense negative for Phase 1 of four−phase rail
37	CSP1	Differential current sense positive for Phase 1 of four−phase rail
38	CSN2	Differential current sense negative for Phase 2 of four−phase rail
39	CSP2	Differential current sense positive for Phase 2 of four−phase rail
40	CSN3	Differential current sense negative for Phase 3 of four−phase rail
41	CSP3	Differential current sense positive for Phase 3 of four−phase rail
42	CSN4	Differential current sense negative for Phase 4 of four−phase rail
43	CSP4	Differential current sense positive for Phase 4 of four−phase rail
44	CSREF	Total−current−sense amplifier reference voltage input for four−phase regulator
45	CSSUM	Inverting input of total−current−sense amplifier for four−phase regulator
46	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for four−phase regulator
47	CSCOMP	Output of total−current−sense amplifier for four−phase regulator
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for four−phase regulator
49	FB	Error amplifier voltage feedback for four−phase regulator
50	DIFF	Output of the four−phase regulator□s differential remote sense amplifier
51	VSP	Differential output voltage sense positive for four−phase regulator
52	VSN	Differential output voltage sense negative for four−phase regulator
53	Flag	GND

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP, COMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP, CSCOMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
DIFF, DIFFA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWM1, PWM2, PWM3, PWM4, PWM1A, PWM2A	VCC + 0.3 V	−0.3 V		
VSN, VSNA	GND + 300 mV	GND − 300 mV	1 mA	1 mA
VRDY	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VCC	6.5 V	−0.3 V		
VRMP	+25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*All signals referenced to GND unless noted otherwise.

Table 3. THERMAL INFORMATION

Description	Symbol	Value	Unit
Thermal Characteristic − QFN Package (Note 1)	R_{JA}	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−10 to +125	°C
Operating Ambient Temperature Range		−10 to +100	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Moisture Sensitivity Level − QFN Package	MSL	1	
ESD Human Body Model	HBM	2500	V
ESD Machine Model	MM	200	V
ESD Charged device model	CDM	1000	V

*The maximum package power dissipation must be observed.
1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. NCP81220 (4+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Units
ERROR AMPLIFIER					
Input Bias Current		−400		400	nA
Open Loop DC Gain	CL = 20 pF to GND, RL = 10 KΩ to GND		80		dB
Open Loop Unity Gain Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		20		MHz
Slew Rate	ΔVin = 100 mV, G = −10 V/V, ΔVout = 0.75 V − 1.52 V, CL = 20 pF to GND, DC Load = 10 k to GND		20		V/μs
Maximum Output Voltage	I_{SOURCE} = 2.0 mA	3.5	−	−	V
Minimum Output Voltage	I_{SINK} = 2.0 mA	−	−	1	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−400	−	400	nA
VSP Input Voltage Range		−0.3	−	3.0	V
VSN Input Voltage Range		−0.3	−	0.3	V
−3 dB Bandwidth	CL = 20 pF to GND, RL = 10 KΩ to GND		12		MHz

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Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL SUMMING AMPLIFIER					
Closed Loop DC gain VS to DIFF	VS+ to VS− = 0.5 to 1.3 V		1		V/V
Droop Accuracy	CSREF−DROOP = 80 mV DAC = 0.8 V to 1.2 V	−42	−40	−38	mV
Maximum Output Voltage	I_{SOURCE} = 2 mA	3.0	–	–	V
Minimum Output Voltage	I_{SINK} = 2 mA	–	–	0.5	V
CURRENT SUMMING AMPLIFIER					
Offset Voltage (Vos)		−300		300	μV
Input Bias Current	CSSUM = CSREF = 1 V	−7.5		7.5	μA
Open Loop Gain			80		dB
Current Sense Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 KΩ to GND		10		MHz
Maximum CSCOMP (A) Output Voltage	Isource = 2 mA	3.5	–	–	V
Minimum CSCOMP(A) Output Voltage	Isink = 2 mA	–	–	0.1	V
CURRENT BALANCE AMPLIFIER					
Input Bias Current	CSPX = CSNX = 1.2 V	−50	–	50	nA
Common Mode Input Voltage Range	CSPx = CSREF	0	–	2.5	V
Differential Mode Input Voltage Range	CSNx = 1.2 V	−30	–	30	mV
Closed loop Input Offset Voltage Matching	CSPx = 1.2 V, Measured from the average	−1.5	–	1.5	mV
Current Sense Amplifier Gain	0 V < CSPx < 0.1 V	5.7	6.0	6.3	V/V
Multiphase Current Sense Gain Matching	CSREF = CSP = 10 mV to 30 mV		±3		%
−3 dB Bandwidth	Guaranteed by simulation		8		MHz
BIAS SUPPLY					
Supply Voltage Range		4.75		5.25	V
VCC Quiescent Current	PS0			55	mA
VCC Quiescent Current	PS1			55	mA
VCC Quiescent Current	PS2			55	mA
VCC Quiescent Current	PS3		35		mA
VCC Quiescent Current	PS4 (@ 25°C)		230		μA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			V
VCC UVLO Hysteresis		90	300	450	mV
VRMP					
Supply Range		4.5		20	V
VRMP UVLO Threshold	VRMP rising			4.2	V
	VRMP falling	3			V
VRMP UVLO Hysteresis			800		mV
DAC SLEW RATE					
Soft Start/Slow Slew Rate			1/2 SR Fast		mv/μs
Slew Rate Fast			>10		mv/μs

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Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Units
DAC SLEW RATE					
AUX Soft Start/Slow Slew Rate			1/2 SR Fast		mv/μs
AUX Slew Rate Fast			>10		mv/μs
ENABLE INPUT					
Enable High Input Leakage Current		−1	0	1	μA
Upper Threshold	VUPPER	0.8			V
Lower Threshold	VLOWER			0.3	V
Enable Delay Time	Measure time from Enable transitioning HI, VBOOT is not 0 V			2.5	ms
DRON					
Output High Voltage	Sourcing 500 μA	3.0	–	–	V
Output Low Voltage	Sinking 500 μA	–	–	0.1	V
Pull Up Resistances			2.0		kΩ
Rise/Fall Time	CL (PCB) = 20 pF, ΔVo = 10% to 90%	–	160		ns
Internal Pull Down Resistance	VCC = 0 V		70		kΩ
IOUT /IOUTA OUTPUT					
Input Referred Offset Voltage	Ilimit to CSREF	−4		+4	mV
Output current max	Ilimit sink current 30 μA	285	300	315	μA
Current Gain	(Iout current)/(Ilimit Current) Rlim = 20 K, Riout = 5 K DAC = 0.8 V, 1.25 V, 1.52 V	9.5	10	10.5	
OSCILLATOR					
Switching Frequency Range		180		1170	kHz
Switching Frequency Accuracy	180 kHz < Fsw < 1170 kHz	−10	–	10	%
PSYS					
Input current max	rsys = 25 K			100	μA
ADC resolution	8 bit		0.4		μA/Bit
Register update rate			145		μs
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Over Voltage Threshold During Soft−Start	CSREF Rising		2.5		V
Over Voltage Threshold Above DAC	VSP rising	350	400	475	mV
Over Voltage Delay	VSP rising to PWMx low		50		ns
Under Voltage Threshold Below DAC−DROOP	VSP falling	350	400	475	mV
Under−voltage Hysteresis	VSP rising		50		mV
Under Voltage Threshold Below DAC−Droop	VSP falling	370	400	425	mV
Under−voltage Hysteresis	VSP rising		25		mV
Under−Voltage Delay			5		μs
SVID DAC					
System Voltage Accuracy	0.75 V ≤ DAC < 1.52 V 0.5 V< DAC < .745 V 0.25 V < DAC < 0.495 V	−0.5 −8 −10		0.5 8 10	% mV mV

Table 4. NCP81220 (4+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Units
OVERCURRENT PROTECTION					
ILIM Threshold Current (OCP shut-down after 50 μs delay)	Main Rail, Rlim = 20 kΩ	8.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	Main Rail, Rlim = 20 k	13	15	16.5	μA
ILIM Threshold Current (OCP shut-down after 50 μs delay)	Main Rail, RLIM = 20 K (N = number of phases in PS0 mode)		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	Main Rail, RLIM = 20 K (N = number of phases in PS0 mode)		15/N		μA
ILIM Threshold Current (OCP shut-down after 50 μs delay)	Auxiliary Rail, Rlim = 20 k	8.0	10	11.0	μA
ILIM Threshold Current (immediate OCP shutdown)	Auxiliary Rail, Rlim = 20 k	13	15	16.5	μA
ILIM Threshold Current (OCP shut-down after 50 μs delay)	Auxiliary Rail RLIM = 20 K		10/N		μA
ILIM Threshold Current (immediate OCP shutdown)	Auxiliary Rail, RLIM = 20 K		15/N		μA
MODULATORS (PWM COMPARATORS) FOR MAIN RAIL & AUXILIARY RAIL					
PWM Min Pulse Width	Fsw = 350 kHz		60		ns
0% Duty Cycle	COMP voltage when the PWM outputs re-main LO		1.3	–	V
100% Duty Cycle	COMP voltage when the PWM outputs re-main HI VRMP = 12.0 V	–	2.5	–	V
PWM Ramp Duty Cycle Matching	COMP = 2 V, PWM Ton matching		1		%
PWM Phase Angle Error	Between adjacent phases		±5		deg
TSENSE/TSENSEA					
VR_HOT Assert Threshold	106°C Threshold		466		mV
VR_HOT Rising Threshold			490		mV
Alert Assertion Threshold	103°C Threshold		485		mV
Alert Rising Threshold			513		mV
Bias Current		115	120	125	μA
VR_HOT					
Output Low Voltage	Isink = 20 mA			0.3	V
Output Leakage Current	High Impedance State	−1.0	–	1.0	μA
ADC					
Voltage Range		0		2.5	V
Total Unadjusted Error (TUE)		−1.25		+1.25	%
Differential Nonlinearity (DNL)	8−bit			1	LSB
Power Supply Sensitivity			±1		%
Conversion Time			10		μs
Round Robin			145		μs
VRDY OUTPUT					
Output Low Voltage	$I_{VDD(A)\_VRDY}$ = 4 mA	–	–	0.3	V
Rise Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%			150	ns

Table 4. NCP81220 (4+2) ELECTRICAL CHARACTERISTICS
Unless otherwise stated: −10°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Conditions	Min	Typ	Max	Units
VRDY OUTPUT					
Fall Time	External pull−up of 1 KΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%			150	ns
Output Voltage at Power−up	VRDY pulled up to 5 V via 2 KΩ enable low	−	−	0.1	V
Output Leakage Current When High	VRDY = 5.0 V	−1.0	−	1.0	μA
VR_RDY Delay (rising)	EN rising to VRDY (TA)		0	2.5	ms
VRDY Delay (falling)	From OVP		300		ns
	Enable falling to VR_RDY falling (TD+TE)			1.5	μs
PWM (A), OUTPUTS					
Output High Voltage	Sourcing 500 μA	VCC − 0.2 V	−	−	V
Output Mid Voltage	No Load, PS0&1	1.9	2.0	2.1	V
Output Low Voltage	Sinking 500 μA	−	−	0.7	V
Rise and Fall Time	CL (PCB) = 50 pF, ΔVo = 10% to 90% of VCC	−	10		ns
Tri−State Output Leakage	Gx = 2.0 V, x = 1−2, EN = Low	−1.0	−	1.0	μA
PHASE DETECTION					
CSP2, CSP3, CSP4, CSP1A, CSP2A Pin Threshold Voltage		4.7			V
Phase Detect Timer			100		μs
SCLK, SDIO					
V_{IL}	Input Low Voltage			0.45	
V_{IH}	Input High Voltage	0.65			V
V_{OH}	Output High Voltage		1.05		V
V_{OL}	SDIO, ALERT and VR_HOT			0.3	V
Leakage Current				1	μA
VR clock to data delay (Tco) (Note 3)		4		8.3	ns
Setup time (Tsu) (Note 3)		7			ns
Hold time (Thld) (Note 3)		14			ns

3. Guaranteed by design or characterization data, not in production test.

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	0.25	01
0	0	0	0	0	0	1	0	0.255	02
0	0	0	0	0	0	1	1	0.26	03
0	0	0	0	0	1	0	0	0.265	04
0	0	0	0	0	1	0	1	0.27	05
0	0	0	0	0	1	1	0	0.275	06
0	0	0	0	0	1	1	1	0.28	07
0	0	0	0	1	0	0	0	0.285	08
0	0	0	0	1	0	0	1	0.29	09
0	0	0	0	1	0	1	0	0.295	0A
0	0	0	0	1	0	1	1	0.3	0B
0	0	0	0	1	1	0	0	0.305	0C
0	0	0	0	1	1	0	1	0.31	0D
0	0	0	0	1	1	1	0	0.315	0E
0	0	0	0	1	1	1	1	0.32	0F
0	0	0	1	0	0	0	0	0.325	10
0	0	0	1	0	0	0	1	0.33	11
0	0	0	1	0	0	1	0	0.335	12
0	0	0	1	0	0	1	1	0.34	13
0	0	0	1	0	1	0	0	0.345	14
0	0	0	1	0	1	0	1	0.35	15
0	0	0	1	0	1	1	0	0.355	16
0	0	0	1	0	1	1	1	0.36	17
0	0	0	1	1	0	0	0	0.365	18
0	0	0	1	1	0	0	1	0.37	19
0	0	0	1	1	0	1	0	0.375	1A
0	0	0	1	1	0	1	1	0.38	1B
0	0	0	1	1	1	0	0	0.385	1C
0	0	0	1	1	1	0	1	0.39	1D
0	0	0	1	1	1	1	0	0.395	1E
0	0	0	1	1	1	1	1	0.4	1F
0	0	1	0	0	0	0	0	0.405	20
0	0	1	0	0	0	0	1	0.41	21
0	0	1	0	0	0	1	0	0.415	22
0	0	1	0	0	0	1	1	0.42	23
0	0	1	0	0	1	0	0	0.425	24
0	0	1	0	0	1	0	1	0.43	25
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	1	0.44	27
0	0	1	0	1	0	0	0	0.445	28
0	0	1	0	1	0	0	1	0.45	29
0	0	1	0	1	0	1	0	0.455	2A

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	1	0	1	1	0.46	2B
0	0	1	0	1	1	0	0	0.465	2C
0	0	1	0	1	1	0	1	0.47	2D
0	0	1	0	1	1	1	0	0.475	2E
0	0	1	0	1	1	1	1	0.48	2F
0	0	1	1	0	0	0	0	0.485	30
0	0	1	1	0	0	0	1	0.49	31
0	0	1	1	0	0	1	0	0.495	32
0	0	1	1	0	0	1	1	0.5	33
0	0	1	1	0	1	0	0	0.505	34
0	0	1	1	0	1	0	1	0.51	35
0	0	1	1	0	1	1	0	0.515	36
0	0	1	1	0	1	1	1	0.52	37
0	0	1	1	1	0	0	0	0.525	38
0	0	1	1	1	0	0	1	0.53	39
0	0	1	1	1	0	1	0	0.535	3A
0	0	1	1	1	0	1	1	0.54	3B
0	0	1	1	1	1	0	0	0.545	3C
0	0	1	1	1	1	0	1	0.55	3D
0	0	1	1	1	1	1	0	0.555	3E
0	0	1	1	1	1	1	1	0.56	3F
0	1	0	0	0	0	0	0	0.565	40
0	1	0	0	0	0	0	1	0.57	41
0	1	0	0	0	0	1	0	0.575	42
0	1	0	0	0	0	1	1	0.58	43
0	1	0	0	0	1	0	0	0.585	44
0	1	0	0	0	1	0	1	0.59	45
0	1	0	0	0	1	1	0	0.595	46
0	1	0	0	0	1	1	1	0.6	47
0	1	0	0	1	0	0	0	0.605	48
0	1	0	0	1	0	0	1	0.61	49
0	1	0	0	1	0	1	0	0.615	4A
0	1	0	0	1	0	1	1	0.62	4B
0	1	0	0	1	1	0	0	0.625	4C
0	1	0	0	1	1	0	1	0.63	4D
0	1	0	0	1	1	1	0	0.635	4E
0	1	0	0	1	1	1	1	0.64	4F
0	1	0	1	0	0	0	0	0.645	50
0	1	0	1	0	0	0	1	0.65	51
0	1	0	1	0	0	1	0	0.655	52
0	1	0	1	0	0	1	1	0.66	53
0	1	0	1	0	1	0	0	0.665	54
0	1	0	1	0	1	0	1	0.67	55

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	1	0	1	1	0	0.675	56
0	1	0	1	0	1	1	1	0.68	57
0	1	0	1	1	0	0	0	0.685	58
0	1	0	1	1	0	0	1	0.69	59
0	1	0	1	1	0	1	0	0.695	5A
0	1	0	1	1	0	1	1	0.70	5B
0	1	0	1	1	1	0	0	0.705	5C
0	1	0	1	1	1	0	1	0.71	5D
0	1	0	1	1	1	1	0	0.715	5E
0	1	0	1	1	1	1	1	0.72	5F
0	1	1	0	0	0	0	0	0.725	60
0	1	1	0	0	0	0	1	0.73	61
0	1	1	0	0	0	1	0	0.735	62
0	1	1	0	0	0	1	1	0.74	63
0	1	1	0	0	1	0	0	0.745	64
0	1	1	0	0	1	0	1	0.75	65
0	1	1	0	0	1	1	0	0.755	66
0	1	1	0	0	1	1	1	0.76	67
0	1	1	0	1	0	0	0	0.765	68
0	1	1	0	1	0	0	1	0.77	69
0	1	1	0	1	0	1	0	0.775	6A
0	1	1	0	1	0	1	1	0.78	6B
0	1	1	0	1	1	0	0	0.785	6C
0	1	1	0	1	1	0	1	0.79	6D
0	1	1	0	1	1	1	0	0.795	6E
0	1	1	0	1	1	1	1	0.8	6F
0	1	1	1	0	0	0	0	0.805	70
0	1	1	1	0	0	0	1	0.81	71
0	1	1	1	0	0	1	0	0.815	72
0	1	1	1	0	0	1	1	0.82	73
0	1	1	1	0	1	0	0	0.825	74
0	1	1	1	0	1	0	1	0.83	75
0	1	1	1	0	1	1	0	0.835	76
0	1	1	1	0	1	1	1	0.84	77
0	1	1	1	1	0	0	0	0.845	78
0	1	1	1	1	0	0	1	0.85	79
0	1	1	1	1	0	1	0	0.855	7A
0	1	1	1	1	0	1	1	0.86	7B
0	1	1	1	1	1	0	0	0.865	7C
0	1	1	1	1	1	0	1	0.87	7D
0	1	1	1	1	1	1	0	0.875	7E
0	1	1	1	1	1	1	1	0.88	7F
1	0	0	0	0	0	0	0	0.885	80

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	0	0	0	1	0.89	81
1	0	0	0	0	0	1	0	0.895	82
1	0	0	0	0	0	1	1	0.90	83
1	0	0	0	0	1	0	0	0.905	84
1	0	0	0	0	1	0	1	0.91	85
1	0	0	0	0	1	1	0	0.915	86
1	0	0	0	0	1	1	1	0.92	87
1	0	0	0	1	0	0	0	0.925	88
1	0	0	0	1	0	0	1	0.93	89
1	0	0	0	1	0	1	0	0.935	8A
1	0	0	0	1	0	1	1	0.94	8B
1	0	0	0	1	1	0	0	0.945	8C
1	0	0	0	1	1	0	1	0.95	8D
1	0	0	0	1	1	1	0	0.955	8E
1	0	0	0	1	1	1	1	0.96	8F
1	0	0	1	0	0	0	0	0.965	90
1	0	0	1	0	0	0	1	0.97	91
1	0	0	1	0	0	1	0	0.975	92
1	0	0	1	0	0	1	1	0.98	93
1	0	0	1	0	1	0	0	0.985	94
1	0	0	1	0	1	0	1	0.99	95
1	0	0	1	0	1	1	0	0.995	96
1	0	0	1	0	1	1	1	1	97
1	0	0	1	1	0	0	0	1.005	98
1	0	0	1	1	0	0	1	1.01	99
1	0	0	1	1	0	1	0	1.015	9A
1	0	0	1	1	0	1	1	1.02	9B
1	0	0	1	1	1	0	0	1.025	9C
1	0	0	1	1	1	0	1	1.03	9D
1	0	0	1	1	1	1	0	1.035	9E
1	0	0	1	1	1	1	1	1.04	9F
1	0	1	0	0	0	0	0	1.045	A0
1	0	1	0	0	0	0	1	1.05	A1
1	0	1	0	0	0	1	0	1.055	A2
1	0	1	0	0	0	1	1	1.06	A3
1	0	1	0	0	1	0	0	1.065	A4
1	0	1	0	0	1	0	1	1.07	A5
1	0	1	0	0	1	1	0	1.075	A6
1	0	1	0	0	1	1	1	1.08	A7
1	0	1	0	1	0	0	0	1.085	A8
1	0	1	0	1	0	0	1	1.09	A9
1	0	1	0	1	0	1	0	1.095	AA
1	0	1	0	1	0	1	1	1.1	AB

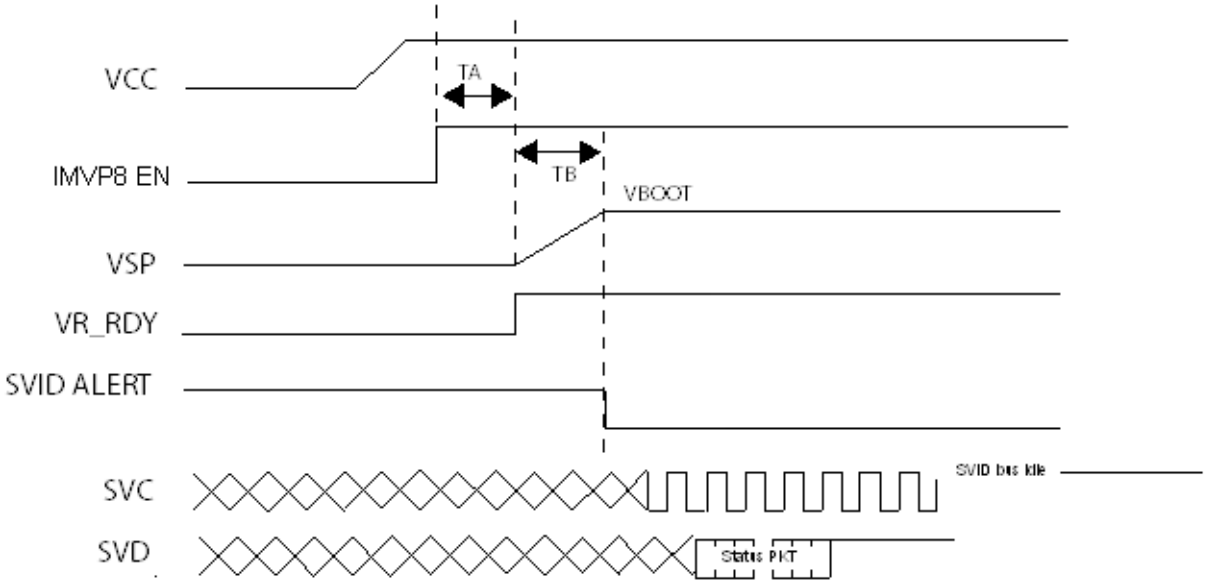
Table 5. IMVP8 VID CODES

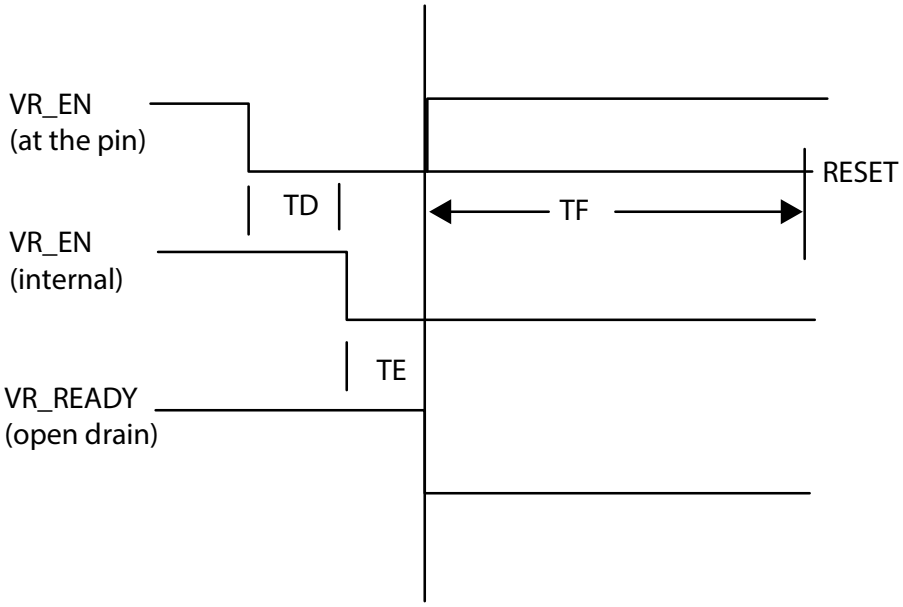
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	1	0	0	1.105	AC
1	0	1	0	1	1	0	1	1.11	AD
1	0	1	0	1	1	1	0	1.115	AE
1	0	1	0	1	1	1	1	1.12	AF
1	0	1	1	0	0	0	0	1.125	B0
1	0	1	1	0	0	0	1	1.13	B1
1	0	1	1	0	0	1	0	1.135	B2
1	0	1	1	0	0	1	1	1.14	B3
1	0	1	1	0	1	0	0	1.145	B4
1	0	1	1	0	1	0	1	1.15	B5
1	0	1	1	0	1	1	0	1.155	B6
1	0	1	1	0	1	1	1	1.16	B7
1	0	1	1	1	0	0	0	1.165	B8
1	0	1	1	1	0	0	1	1.17	B9
1	0	1	1	1	0	1	0	1.175	BA
1	0	1	1	1	0	1	1	1.18	BB
1	0	1	1	1	1	0	0	1.185	BC
1	0	1	1	1	1	0	1	1.19	BD
1	0	1	1	1	1	1	0	1.195	BE
1	0	1	1	1	1	1	1	1.2	BF
1	1	0	0	0	0	0	0	1.205	C0
1	1	0	0	0	0	0	1	1.21	C1
1	1	0	0	0	0	1	0	1.215	C2
1	1	0	0	0	0	1	1	1.22	C3
1	1	0	0	0	1	0	0	1.225	C4
1	1	0	0	0	1	0	1	1.23	C5
1	1	0	0	0	1	1	0	1.235	C6
1	1	0	0	0	1	1	1	1.24	C7
1	1	0	0	1	0	0	0	1.245	C8
1	1	0	0	1	0	0	1	1.25	C9
1	1	0	0	1	0	1	0	1.255	CA
1	1	0	0	1	0	1	1	1.26	CB
1	1	0	0	1	1	0	0	1.265	CC
1	1	0	0	1	1	0	1	1.27	CD
1	1	0	0	1	1	1	0	1.275	CE
1	1	0	0	1	1	1	1	1.28	CF
1	1	0	1	0	0	0	0	1.285	D0
1	1	0	1	0	0	0	1	1.29	D1
1	1	0	1	0	0	1	0	1.295	D2
1	1	0	1	0	0	1	1	1.3	D3
1	1	0	1	0	1	0	0	1.305	D4
1	1	0	1	0	1	0	1	1.31	D5
1	1	0	1	0	1	1	0	1.315	D6

Table 5. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	0	1	0	1	1	1	1.32	D7
1	1	0	1	1	0	0	0	1.325	D8
1	1	0	1	1	0	0	1	1.33	D9
1	1	0	1	1	0	1	0	1.335	DA
1	1	0	1	1	0	1	1	1.34	DB
1	1	0	1	1	1	0	0	1.345	DC
1	1	0	1	1	1	0	1	1.35	DD
1	1	0	1	1	1	1	0	1.355	DE
1	1	0	1	1	1	1	1	1.36	DF
1	1	1	0	0	0	0	0	1.365	E0
1	1	1	0	0	0	0	1	1.37	E1
1	1	1	0	0	0	1	0	1.375	E2
1	1	1	0	0	0	1	1	1.38	E3
1	1	1	0	0	1	0	0	1.385	E4
1	1	1	0	0	1	0	1	1.39	E5
1	1	1	0	0	1	1	0	1.395	E6
1	1	1	0	0	1	1	1	1.4	E7
1	1	1	0	1	0	0	0	1.405	E8
1	1	1	0	1	0	0	1	1.41	E9
1	1	1	0	1	0	1	0	1.415	EA
1	1	1	0	1	0	1	1	1.42	EB
1	1	1	0	1	1	0	0	1.425	EC
1	1	1	0	1	1	0	1	1.43	ED
1	1	1	0	1	1	1	0	1.435	EE
1	1	1	0	1	1	1	1	1.44	EF
1	1	1	1	0	0	0	0	1.445	F0
1	1	1	1	0	0	0	1	1.45	F1
1	1	1	1	0	0	1	0	1.455	F2
1	1	1	1	0	0	1	1	1.46	F3
1	1	1	1	0	1	0	0	1.465	F4
1	1	1	1	0	1	0	1	1.47	F5
1	1	1	1	0	1	1	0	1.475	F6
1	1	1	1	0	1	1	1	1.48	F7
1	1	1	1	1	0	0	0	1.485	F8
1	1	1	1	1	0	0	1	1.49	F9
1	1	1	1	1	0	1	0	1.495	FA
1	1	1	1	1	0	1	1	1.5	FB
1	1	1	1	1	1	0	0	1.505	FC
1	1	1	1	1	1	0	1	1.51	FD
1	1	1	1	1	1	1	0	1.515	FE
1	1	1	1	1	1	1	1	1.52	FF

Startup Timing

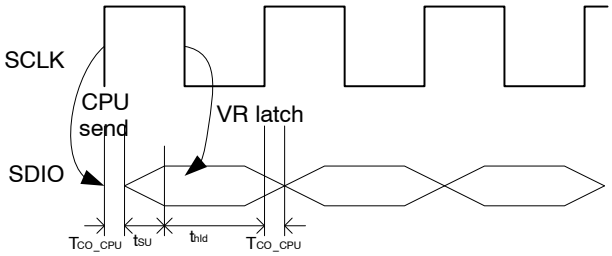




	Min	Typ	Max
TA			2.5 ms
TB			VID / Slow
TD	0 μs		1 μs
TE			500 ns

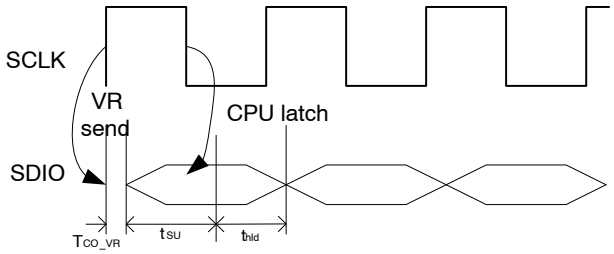
SVID Timing Diagram

CPU Driving, Single Data Rate



T_{co_CPU} = clock to data delay in CPU
$tsu = 0.5 * T - T_{co\_CPU}$
$thld = 0.5 * T + T_{co\_CPU}$

VR Driving, Single Data Rate



T_{co_VR} = clock to data delay in VR
$tsu = T - 2 * T_{fly} - T_{co\_VR}$
$thld = 2 * T_{fly} + T_{co\_VR}$
T_{fly} propagation time on Serial VID bus

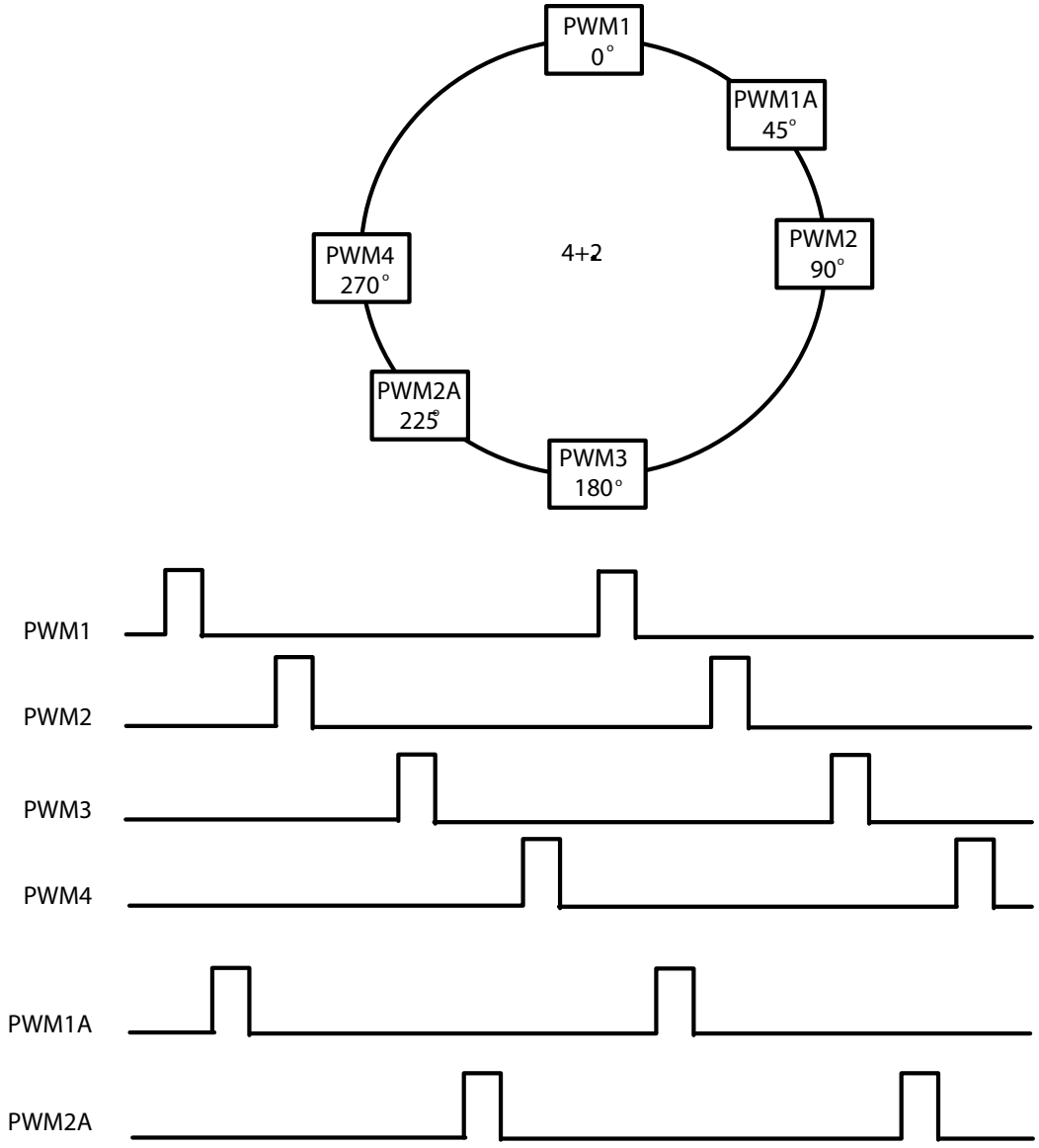
General

The NCP81220 is a dual rail four plus two phase dual edge modulated multiphase PWM controller, with a serial SVID interface. The NCP81220 is optimized to meet Intel's IMVP8 Specifications and implements PS0, PS1, PS2, PS3 and PS4 power saving states. The NCP81220 is designed to work in desktop and gaming applications.

Power Status	PWM Output Operating Mode
PS0	Multi−phase PWM interleaving output
PS1	Single−phase RPM CCM mode (Selectable 1 or 2 phase count)
PS2	Single−phase RPM DCM mode (PWM1 only, PWM2~3 stay in Mid)
PS3	Single−phase RPM DCM mode (PWM1 only, PWM2~3 stay in Mid)
PS4	Vout to 0 V, no phase state

Phase Interleaving

Phase interleaving is only possible when both rails are programmed with the same Fsw. If the Fsw is different, it is impossible to keep phases from different rails from firing at the same time.



SVID Addresses/Phase Configuration

During startup, Pin 34 (PWM1/SV_ADDR) is sampled to determine the SVID address and the phase configuration. More details in the table below:

Resistor	"main" SVID Address	"A" Address	4+2 or 3+3
10 kΩ	0 (Core)	1 (GT)	4+2
25 kΩ	1 (GT)	0 (Core)	4+2
45 kΩ	0 (Core)	2 (SA)	4+2
70 kΩ	1 (GT)	3 (GTUS)	4+2
95 kΩ	0 (Core)	1 (GT)	3+3
125 kΩ	1 (GT)	0 (Core)	3+3
165 kΩ	0 (Core)	2 (SA)	3+3
220 kΩ	1 (GT)	3 (GTUS)	3+3

The table above shows how to configure the part as either a 4+2 or a 3+3, however, if an alternative configuration such as 2+2 or 3+2 is desired then the phase that is no longer required must have its CSP pin shorted to 5 V. If any more than 2 phases are required on the GT rail then one of the 3+3 options in the table above must be selected.

I.e. if a 2+2 configuration is required, you must select a 4+2 configuration from the table above and then disable 2 phases from the Core rail by shorting CSP2 and CSP4 to 5 V.

If a 2+3 configuration is required, you will select a 3+3 configuration from the table above and disable the third phase of the Core rail by shorting CSP3 to 5 V. In this instance PWM4 is used on the GT rail.

Serial VID Interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the NCP81220 (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT. The SCLK is unidirectional and generated by the master. The SDIO is bi−directional, used for transferring data from the CPU to the NCP81220 and from the NCP81220 to the CPU. The ALERT is an open drain output from the NCP81220 to signal to the master that the Status Register should be read.

SCLK, SDIO and ALERT should be pulled high to CPU I/O voltage Vtt (which is typically 1.0 to 1.1 V) using 55 Ω Resistors.

The SVID bus will operate at a max frequency of 43 MHz.

VID code change is supported by SVID interface with three options as below:

Option	SVID Command Code	Feature Description	Register Address (Indicating the slew rate of VID code change)
SetVID_Fast	01h	>10mV/us VID code change slew rate	24h
SetVID_Slow	02h	=1/2 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

Serial VID

The NCP81220 supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT). The table of supported registers is shown below.

Table 6. SVID REGISTER MAP

Index	Name	Description	Access	Default
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	20h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	
03h	Product date code ID		R	
05h	Protocol ID	Identifies the SVID Protocol the controller supports	R	05h
06h	Capability	Informs the Master of the controller's Capabilities, 1 = supported, 0 = not supported Bit 7 = Iout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1 Bit 6 = ADC Measurement of Temp Supported = 1 Bit 5 = ADC Measurement of P_{IN} Supported = 0 Bit 4 = ADC Measurement of V_{IN} Supported = 0 Bit 3 = ADC Measurement of I_{IN} Supported = 0 Bit 2 = ADC Measurement of P_{OUT} Supported = 1 Bit 1 = ADC Measurement of V_{OUT} Supported = 1 Bit 0 = ADC Measurement of I_{OUT} Supported = 1	R	D7h
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R	01h
16h	V_out	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 9.8 mV	R	01h
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C=64h. A value of 00h indicates this function is not supported	R	01h
18h	P_out	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported	R	01h

Table 6. SVID REGISTER MAP

Index	Name	Description	Access	Default
1Ah	Input Voltage	8 bit binary word ADC of voltage, optional for control IC that supports direct ADC conversion of average input voltage. A value of 00h indicates this function is not supported	R	00h
1Bh	Input Power	Required for Input Power Domain Address 0Dh	R	
1Ch	Status2_last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 106°C and programmable over the SVID Interface	R/W	6Ah
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us.	R	0Eh
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/us. FAST/2 is default for IMVP8	R	07h
26h	Vboot	The boot voltage is programmed at startup using a resistor to GND and subsequently controlled from here. The controller will ramp to Vboot and hold at Vboot until it receives a new SVID SetVID command to move to a different voltage.	R	00h
2Ah	SR_Slow selector	01 = Fast_SR/2: default 02 = Fast_SR/4 04 = Fast_SR/8 08 = Fast_SR/16	R/W	01h
2Bh	PS4 exit latency	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp	R	8Ch
2Ch	PS3 exit latency	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h
2Dh	EN to Ready for SVID command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format.	RW	FBh
31h	VID setting	Data register containing currently programmed VID voltage. VID data format.	RW	00h
32h	Pwr State	Register containing the current programmed power state.	RW	00h

33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.
		00h=no margin
		01h=+1 VID step
		02h=+2 VID steps
		FFh=−1 VID step
		FEh=−2 VID steps.
			RW	00h

34h	MultiVR Config		RW	01h
35h	SetRegADR	Scratch pad register for temporary storage of SetRegADR pointer register	RW	
42h	IVID1−VID		RW	00h
43h	IVID1−I	Maximum instantaneous current for single phase operation. Threshold set based on IVID1−I = (IccMax/Num of Phases + 8). *Note: IVID−I must not be programmed with a value greater than IccMax.*	RW	
44h	IVID2−VID		RW	00h
45h	IVID2−I	Maximum instantaneous current for IVID 2 state. Default matches IVID1−I. *Note: IVID−I must not be programmed with a value greater than IccMax.*	RW	
46h	IVID3−VID		RW	00h
47h	IVID3−I	Maximum instantaneous current for DCM/CCM decision threshold. *Note: IVID−I must not be programmed with a value greater than IccMax.*	RW	

BOOT Voltage Programming

The NCP81220 has a V_{BOOT} voltage register that can be externally programmed for both core and Auxiliary boot−up output voltages (pins 29 and 33). The V_{BOOT} voltage for main and auxiliary rails can be programmed with a resistor from V_{BOOT} and V_{BOOTA} pin to GND. The V_{BOOT} value can be read back over the SVID interface in register (0x26). Pin 33 (PWM2/V_{BOOT}) is used to set the boot voltage for the main rail, pin 29 (PWM2A/V_{BOOTA}) is used to configure the Auxiliary rail. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. Table 7 shows the resistor values that should be used and the corresponding V_{BOOT} options.

Table 7. VBOOT PROGRAMMABILITY

Resistor	V_{BOOT}
10 kΩ	0
30 kΩ	0.8
60 kΩ	1.05
100 kΩ	1.2
160 kΩ	1.4
220 kΩ	1.5

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed by a resistor to ground on the ROSC pin. The oscillator frequency range is between 180 KHz/phase to 1.17 MHz/phase. The ROSC pin provides approximately 2 V out and the source current is mirrored into the internal ramp oscillator. Available frequency options are as follows:

Resistor (kΩ)	Frequency (kHz)
10	180
14.7	225
20	270
26.1	315
33.2	360
41.2	405
49.9	450
60.4	495
71.5	540
84.5	630
100	720
118.3	810
136.6	900
157.7	990
182.1	1080
249	1170

IVID and Phase Shedding

In PS0, the each rail of the NCP81220 can change its operating mode based on output current and/or programmed VID. As the IMVP8 SVID IVID registers only define a maximum current associated with specific VIDs, each rail can make phase−shed decisions based on the IOUT level in addition to the programmed VID. If IOUT is less than IVID2−I for longer than 2 ms, the multiphase rail will shed the phase and operate in single−phase mode, even if VID is greater than IVID2−VID. The second phase can also be turned off without the 2 ms delay if programmed VID is less than IVID2−VID, and IOUT is verified to be less than IVID2−I.

Also while in PS0, the operating mode can drop to single−phase DCM operation if programmed VID is less than IVID3−VID. Each rail will not drop into DCM mode based on IOUT alone.

The controller exits Efficiency Optimized Modes and turns on all phases when any SetVID command is issued, if a transient load is detected, or if output loading crosses the IVID2−I threshold.

If a SetPS command is received, the controller will place itself in the lowest appropriate state. For example, if in PS0 the controller has automatically transitioned into DCM RPM and receives a SetPS = 1 command, the PS register will be updated, but the controller will remain in DCM RPM mode. If while in PS1 the current increases or a transient is detected, the controller will move into CCM mode.

See IMVP8 specification for more details on IVID

PSYS

The psys pin is an analog input to the NCP81220. It is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the NCP81220 facilitates reporting back current and through the SVID interface at address 0Dh.

PSYS Disable

The PSYS feature can be disabled by pulling the PSYS pin to 5 V.

Phase Disable

If a lower number of phases is required then phases can be disabled by pulling the relevant CSP pin directly to 5 V. For the Core rail here are the options for active phases:

4 Phase	All phases active
3 Phase	PWM4 is disabled by connecting CSP4 to 5 V.
2 Phase	PWM2 and PWM4 are disabled by connecting CSP2 and CSP4 to 5 V.
1 Phase	Only PWM1 is active, CSP2, CSP3 and CSP4 are tied to 5 V.

For the GT rail PWM1A & PWM2A can be disabled by connecting CSP1A & CSP2A to 5 V.

Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

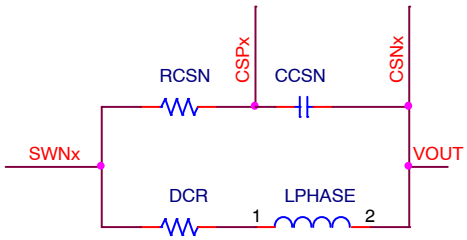
This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type III compensation circuit is normally used to compensate the system.

Differential Current Feedback Amplifiers

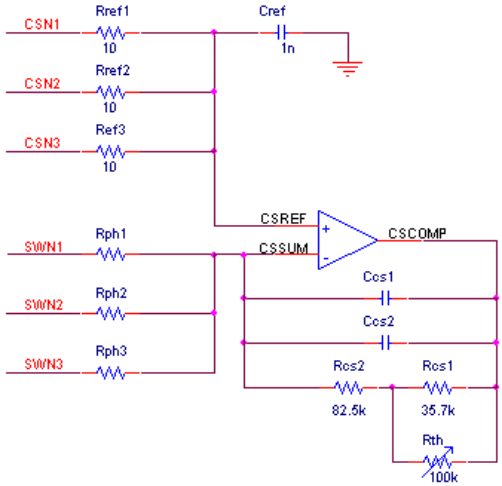
Each phase has a low offset differential amplifier to sense that phase current for current balance. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.



$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \cdot DCR}$$

Total Current Sense Amplifier

The NCP81220 uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Ref(n) resistors sum the signals from the output side of the inductors to create a low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.



The DC gain equation for the current sensing:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot (Iout_{Total} \cdot DCR)$$

Set the gain by adjusting the value of the Rph resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The values of Rcs1 and Rcs2 are set based on the 100 k NTC and the temperature effect of the inductor and should not need to be changed. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. Ccs1 and Ccs2 are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR@25C}{2 \cdot PI \cdot L_{Phase}}$$

Programming the Current Limit

The NCP81220 compares a programmable current−limit set point to the voltage from the output of the current−summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP. The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current limit current I_{CL}. If the current generated through this resistor into

the ILIM pin (Ilim) exceeds the internal current−limit threshold current (I_{CL}), an internal latch−off counter starts, and the controller shuts down if the fault is not removed after 50 μs (shut down immediately for 150% load current) after which the outputs will remain disabled until the Vcc voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per−phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over−current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations,

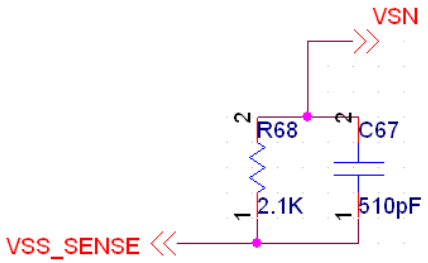
Equation related to the Rilim,:

$$R_{ILIM} = \frac{I_{LIM} \cdot DCR \cdot R_{CS}/R_{PH}}{I_{CL}}$$

Where I_{CL} = 10 μA

Programming DAC Feed−Forward Filter

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.

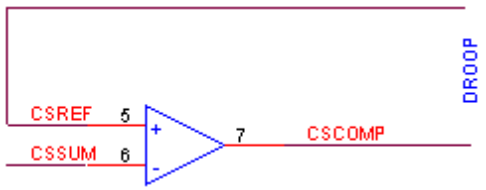


$$Rvsn = Cout \cdot Rout \cdot 453.6 \times 10^6$$

$$Cvsn = \frac{Rout \cdot Cout}{Rvsn}$$

Programming DROOP

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.



Droop = DCR * (R_{CS} / R_{ph})

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.5\ V \cdot R_{LIMIT}}{10 \cdot \frac{Rcs2 + \frac{Rcs1 \cdot Rth}{Rcs1 + Rth}}{Rph} \cdot \left(Iout_{ICC\_MAX} \cdot DCR\right)}$$

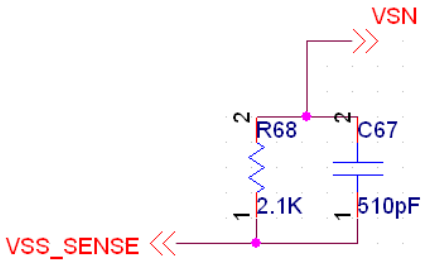
Programming ICC_MAX

The SVID interface provides the platform ICC_MAX value at register 21h for. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10 k.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 255\ A}{2.5\ V}$$

Programming DAC Feed−Forward Filter

The DAC feed−forward implementation is realized by having a filter on the VSN pin. Programming Rvsn sets the gain of the DAC feed−forward and Cvsn provides the time constant to cancel the time constant of the system per the following equations. Cout is the total output capacitance and Rout is the output impedance of the system.

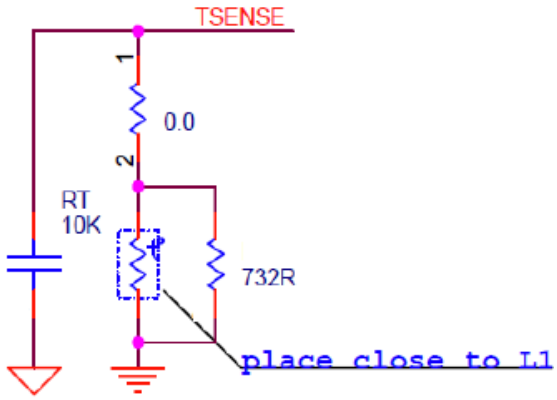


$$Rvsn = Cout \cdot Rout \cdot 453.6 \times 10^6$$

$$Cvsn = \frac{Rout \cdot Cout}{Rvsn}$$

Programming TSENSE

A temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 10 k NTC similar to the TSM0B103H3371RZ should be used. Rcomp1 is mainly used for noise. See the specification table for the thermal sensing voltage thresholds and source current.



Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. The oscillator frequency range is between 180 kHz/phase to 1170 kHz/phase. The operating frequency can be programmed using a resistor to ground from PWM4.

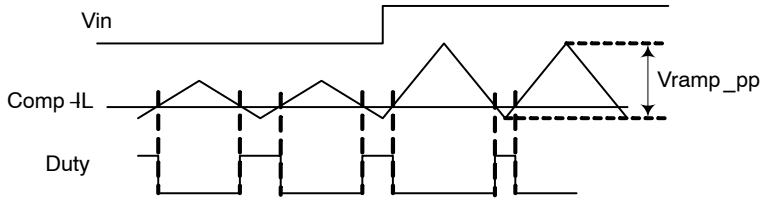
The oscillator generates triangle ramps that are 0.5~1.3 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation. The ramps are equally spaced out of phase with respect to each other and the signal phase rail is set half way between phases 1 and 2 of the multi phase rail for minimum input ripple current.

Programming the Ramp Feed−Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage feed−forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a 4 V UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp time is changed according to the following,

$$V_{RAMPpk=pk_{PP}} = 0.1 \cdot V_{VRMP}$$



PWM Comparators

The non−inverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current (I*DCR*Phase Balance Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately Vout/Vin. During a transient event, the controller will operate in a hysteretic mode with the duty cycles pull in for all phases as the error amp signal increases with respect to all the ramps.

Protection Features

Under Voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. NCP81220 monitors the 5 V VCC supply. The gate driver monitors both the gate driver VCC and the BST voltage. When the voltage on the gate driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off its startup sequence. In this case the PWM is set to the MID state to begin soft start.

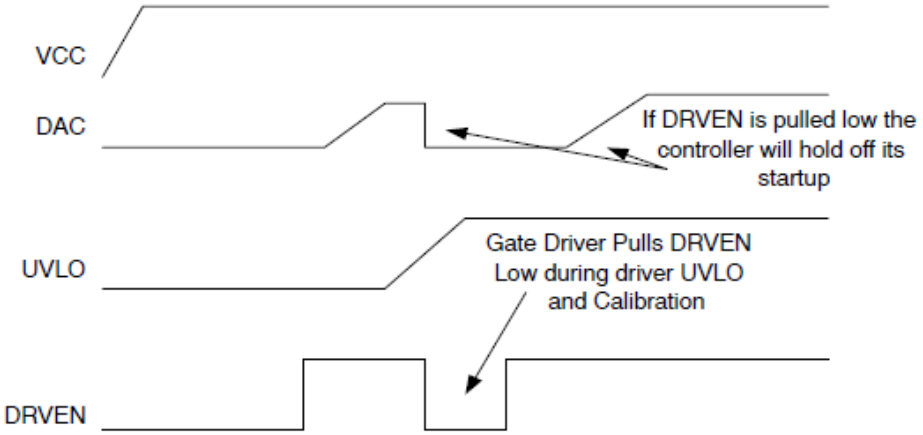


Figure 2. Gate Driver UVLO Restart

Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined rate in the spec table. The PWM signals will start out open with a test current to collect data on phase count and for setting internal registers. After the configuration data is collected, if the controller is enabled the PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When the controller is disabled the PWM signal will return to the MID state.

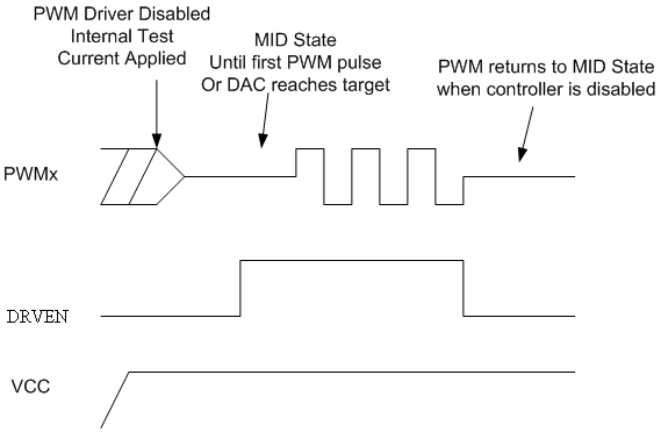


Figure 3. Soft−Start Sequence

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage (DAC voltage includes offset) by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V. At the same time, the high side gate drivers are all turned off and the low side gate drivers are all turned on. The part will stay in this mode until the Vcc voltage or EN is toggled.

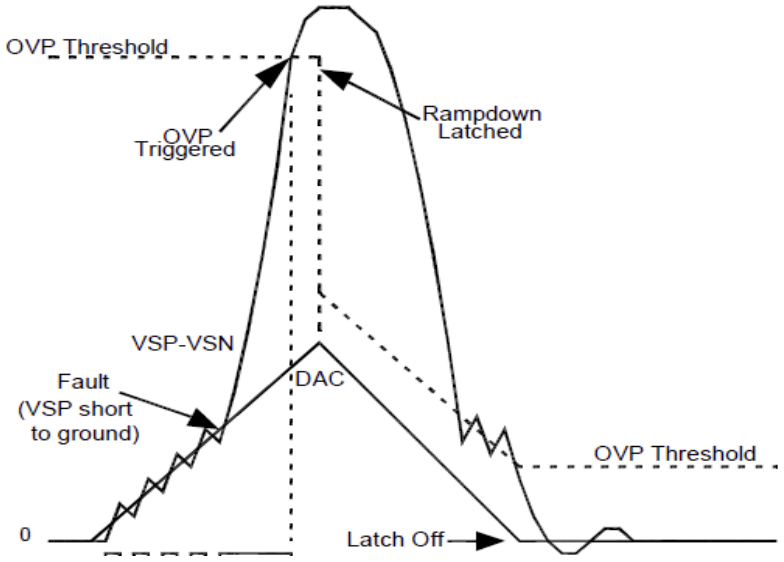


Figure 4. OVP Behavior at Startup

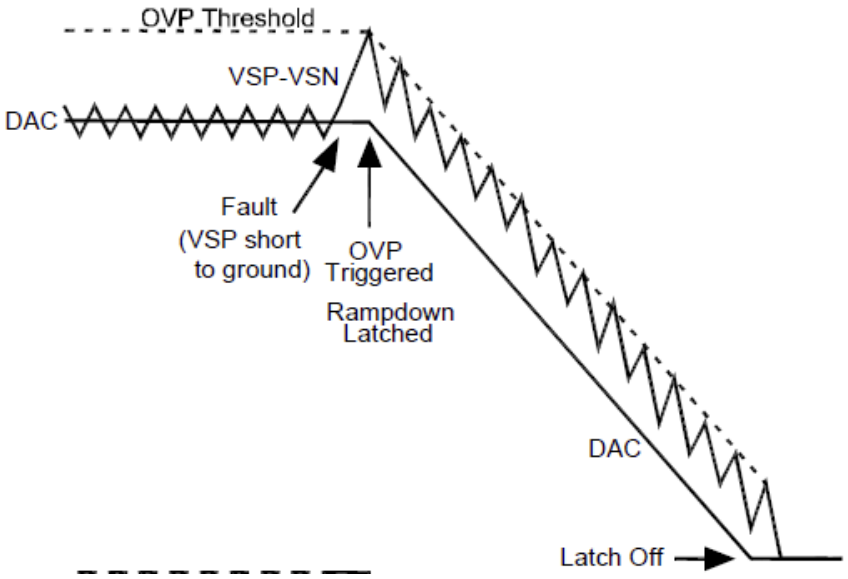
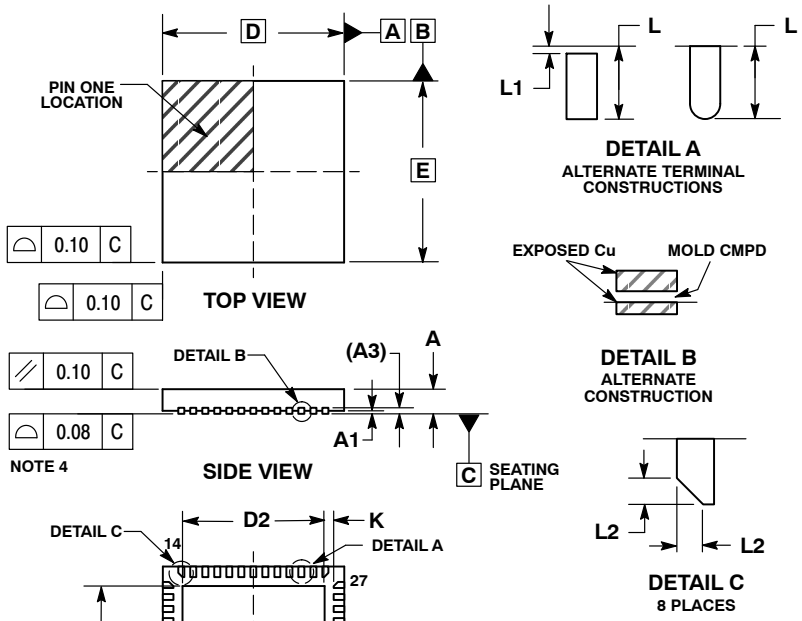
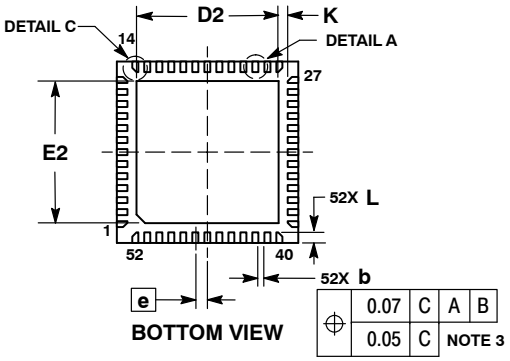


Figure 5. OVP During Normal Operation Mode

PACKAGE DIMENSIONS

QFN52 6x6, 0.4P
CASE 485BE
ISSUE B

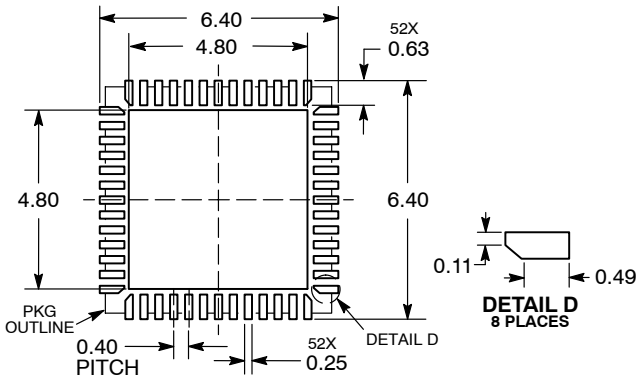




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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