NCP81231

High Resolution Buck Controller with Full USB PD Features and 100% Duty Operation

The NCP81231 is a synchronous buck that is optimized for converting battery voltage or adaptor voltage into power supply rails required in notebook, tablet, and desktop systems, as well as many other consumer devices using USB PD standard and C−Type cables. The NCP81231 is fully compliant to the USB Power Delivery Specification when used in conjunction with a USB PD or C−Type Interface Controller. NCP81231 is designed for applications requiring dynamically controlled slew rate limited output voltage.

Features

- Wide Input Voltage Range: from 4.5 V to 28 V
- Dynamically Programmed Frequency from 150 kHz to 1.2 MHz
- I^2C Interface
- Real Time Power Good Indication
- Controlled Slew Rate Voltage Transitioning
- Feedback Pin with Internally Programmed Reference
- High Resolution DAC Voltage
- Two Independent Current Sensing Inputs
- Support Inductor DCR Sensing
- Over Temperature Protection
- Adaptive Non−Overlap Gate Drivers
- Filter Capacitor Switch Control
- 100% Duty Cycle Operation
- Latched Over−Voltage and Over−Current Protection
- Dead Battery Power Support
- 5 x 5 mm QFN32 Package

Typical Application

- Notebooks, Tablets, Desktops
- Gaming
- Monitors, TVs, and Set Top Boxes
- Consumer Electronics
- Car Chargers
- Docking Stations
- Power Banks

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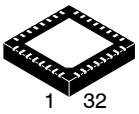


QFN32 5x5, 0.5P
CASE 485CE

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81231MNTXG	QFN32 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

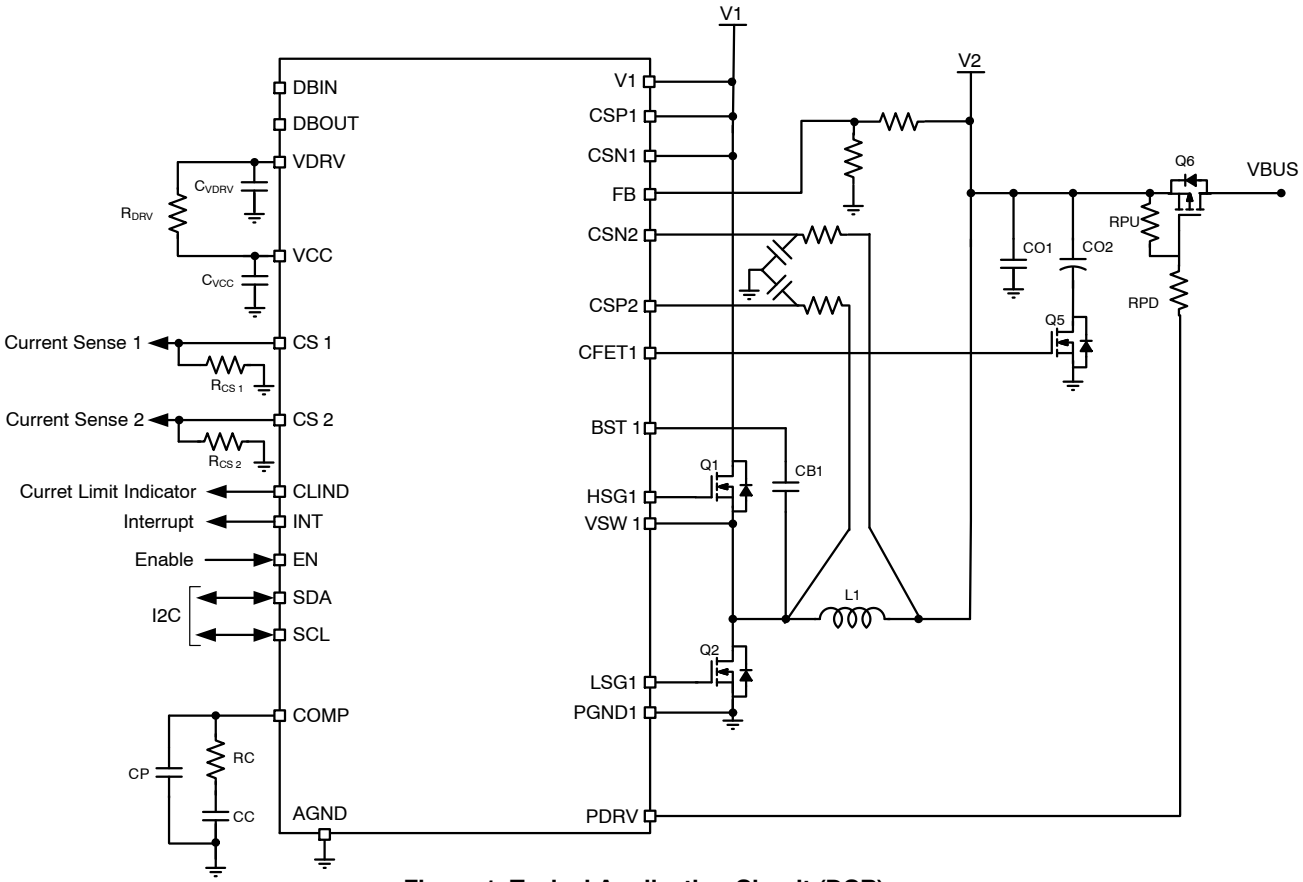


Figure 1. Typical Application Circuit (DCR)

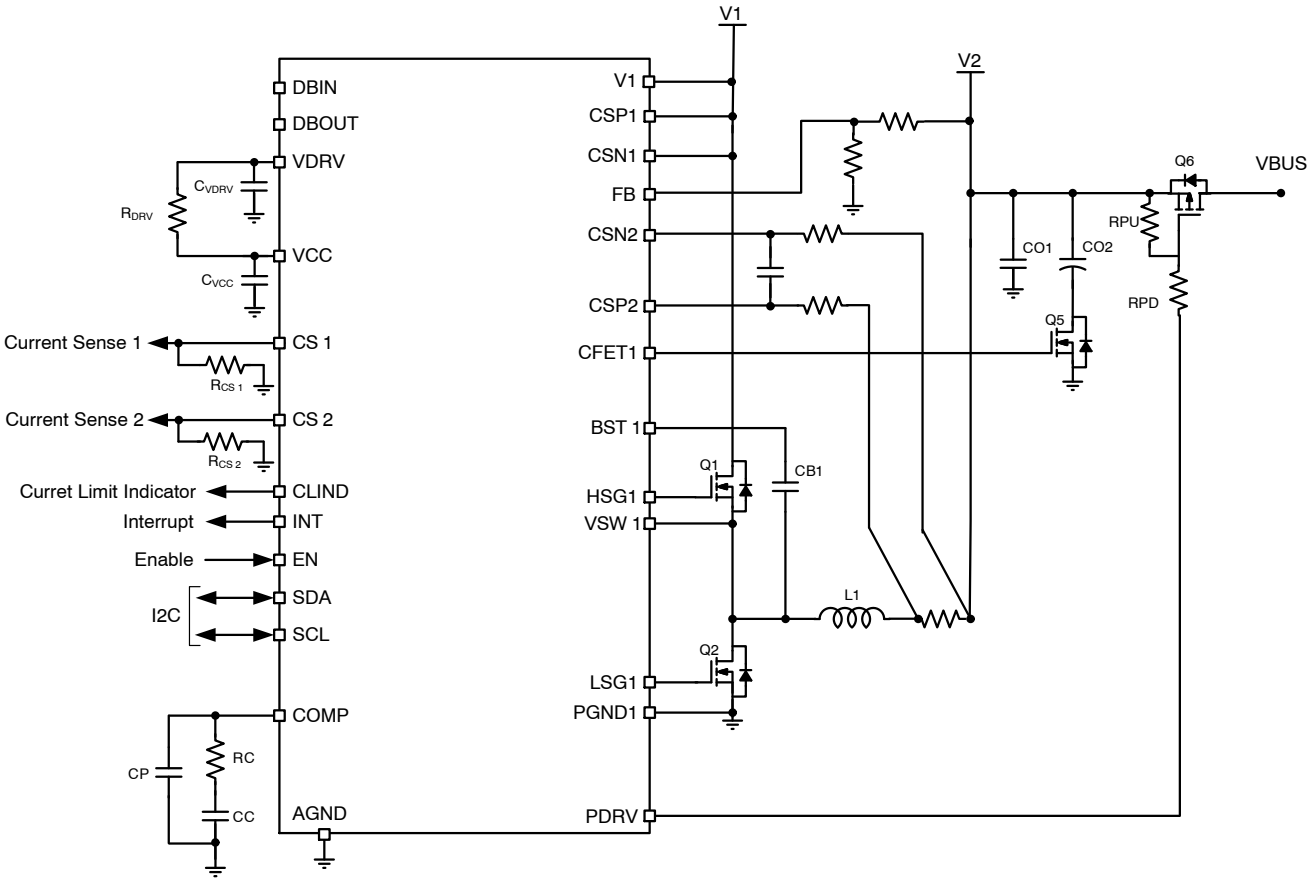


Figure 2. Typical Application Circuit (Rsense)

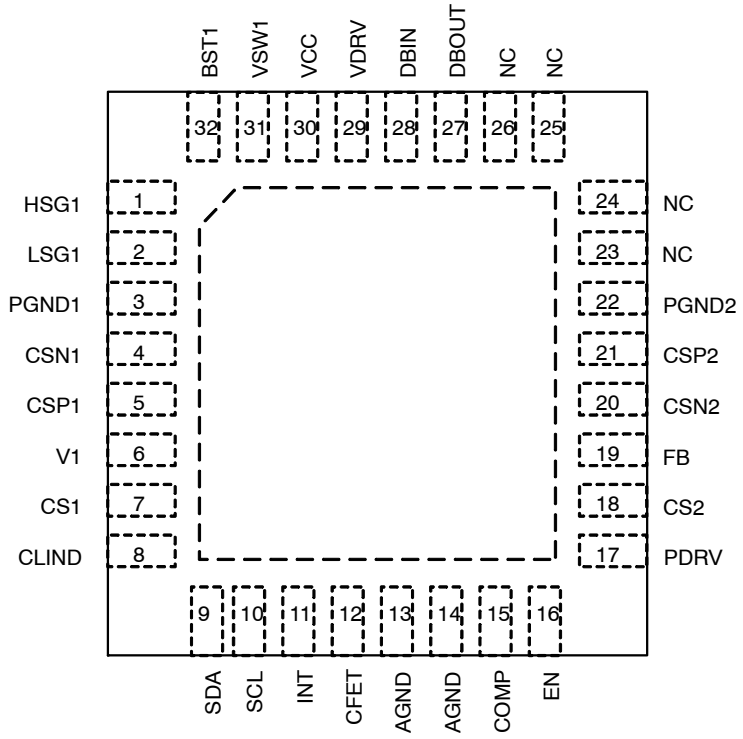


Figure 3. Pinout

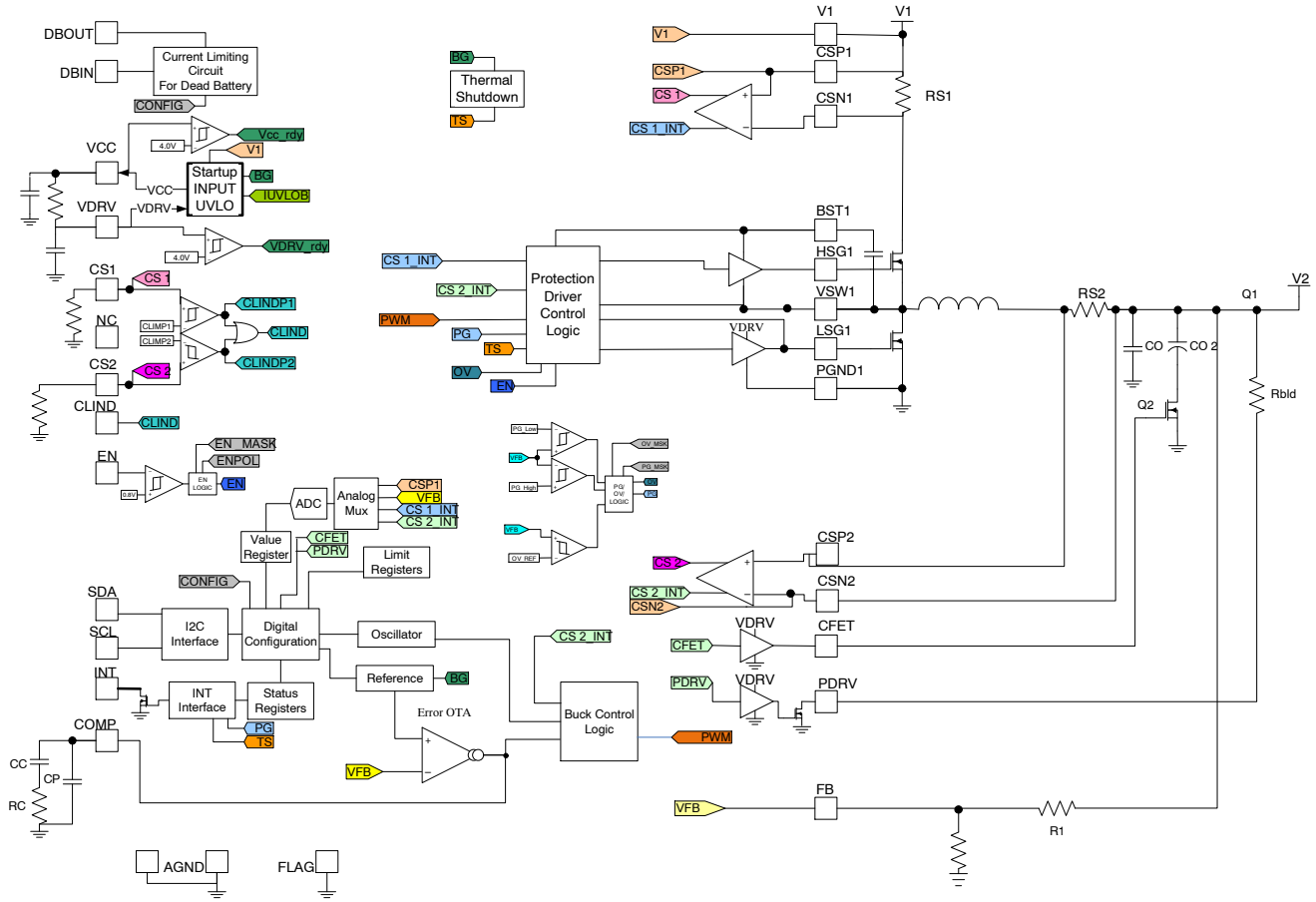


Figure 4. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	HSG1	S1 gate drive. Drives the S1 N−channel MOSFET with a voltage equal to VDRV superimposed on the switch node voltage VSW1.
2	LSG1	Drives the gate of the S2 N−channel MOSFET between ground and VDRV.
3, 22	PGND	Power ground for the low side MOSFET drivers. Connect these pins closely to the source of the bottom N−channel MOSFETs.
4	CSN1	Negative terminal of the current sense amplifier.
5	CSP1	Positive terminal of the current sense amplifier.
6	V1	Input voltage of the converter
7	CS1	Current sense amplifier output. CS1 will source a current that is proportional to the voltage across CSP1/CSN1. Connect CS1 to a high impedance monitoring input.
8	CLIND	Open drain output to indicate that the CS1 or CS2 voltage has exceeded the I^2C programmed limit.
9	SDA	I^2C interface data line.
10	SCL	I^2C interface clock line.
11	INT	Interrupt is an open drain output that indicates the state of the output power, the internal thermal trip, and other I^2C programmable functions.
12	CFET	Controlled drive of an external MOSFET that connects a bulk output capacitor to the output of the power converter. Necessary to adhere to low capacitance limits of the standard USB Specifications for power prior to USB PD negotiation.
13, 14	AGND	The ground pin for the analog circuitry.
15	COMP	Output of the transconductance amplifier used for stability in closed loop operation.

Table 1. PIN FUNCTION DESCRIPTION (continued)

Pin	Pin Name	Description
16	EN	Precision enable starts the part and places it into default configuration when toggled.
17	PDRV	The open drain output used to control a PMOSFET or connect to an external resistor.
18	CS2	Current sense amplifier output. CS2 will source a current that is proportional to the voltage across CSP1/CSN1. Connect CS2 to a high impedance monitoring input.
19	FB	Feedback voltage of the output, negative terminal of the gm amplifier.
20	CSN2	Negative terminal of the current sense amplifier.
21	CSP2	Positive terminal of the current sense amplifier.
23−25	NC	No connection.
26	NC	No connection.
27	DBOUT	The output of the dead battery circuit which can also be used for the VCONN voltage supply.
28	DBIN	The dead battery input to the converter where 5 V is applied. A 1 μF capacitor should be placed close to the part to decouple this line.
29	VDRV	Internal voltage supply to the driver circuits. A 1 μF capacitor should be placed close to the part to decouple this line.
30	VCC	The VCC pin supplies power to the internal circuitry. The VCC is the output of a linear regulator which is powered from V1. Can be used to supply up to a 100 mA load. Pin should be decoupled with a 1 μF capacitor for stable operation.
31	VSW1	Switch Node. VSW1 pin swings from a diode voltage drop below ground up to V1.
32	BST1	Driver Supply. The BST1 pin swings from a diode voltage below VDRV up to a diode voltage below V1 + VDRV. Place a 0.1 μF capacitor from this pin to VSW1.
33	THPAD	Center pad, recommended to connect to AGND.

Table 2. MAXIMUM RATINGS
(Over operating free−air temperature range unless otherwise noted)

Rating	Symbol	Min	Max	Unit
Input of the Dead Battery Circuit	DBIN	−0.3	5.5	V
Output of the Dead Battery Circuit	DBOUT	−0.3	5.5	V
Driver Input Voltage	VDRV	−0.3	5.5	V
Internal Regulator Output	VCC	−0.3	5.5	V
Output of Current Sense Amplifiers	CS1, CS2	−0.3	3.0	V
Current Limit Indicator	CLIND	−0.3	VCC + 0.3	V
Interrupt Indicator	INT	−0.3	VCC + 0.3	V
Enable Input	EN	−0.3	5.5	V
I^2C Communication Lines	SDA, SCL	−0.3	VCC + 0.3	V
Compensation Output	COMP	−0.3	VCC + 0.3	V
V1 Power Stage Input Voltage	V1	−0.3	32 V, 40 V (20 ns)	V
Positive Current Sense	CSP1	−0.3	32 V, 40 V (20 ns)	V
Negative Current Sense	CSN1	−0.3	32 V, 40 V (20 ns)	V
Positive Current Sense	CSP2	−0.3	32 V, 40 V (20 ns)	V
Negative Current Sense	CSN2	−0.3	32 V, 40 V (20 ns)	V
Feedback Voltage	FB	−0.3	5.5	V
CFET Driver	CFET	−0.3	VCC + 0.3	V
Driver Positive Rail	BST1	−0.3 V wrt/PGND −0.3 V wrt/VSW	37 V, 40 V (20 ns) wrt/PGND 5.5 V wrt/VSW	V

Table 2. MAXIMUM RATINGS (continued)
(Over operating free−air temperature range unless otherwise noted)

Rating	Symbol	Min	Max	Unit
High Side Driver	HSG1	−0.3 V wrt/PGND −0.3 V wrt/VSW	37 V, 40 V (20 ns) wrt/GND 5.5 V wrt/VSW	V
Switching Node and Return Path of Driver	VSW1	−5.0 V	32 V, 40 V (20 ns)	V
Low Side Driver	LSG1	−0.3 V	5.5	V
PMOSFET Driver	PDRV	−0.3	40	V
Voltage Differential	AGND to PGND	−0.3	0.3	V
CSP1−CSN1, CSP2−CSN2 Differential Voltage	CS1DIF, CS2DIF	−0.5	0.5	V
PDRV Maximum Current	PDRVI	0	10	mA
PDRV Maximum Pulse Current (100 ms on time, with > 1 s interval)	PDRVIPUL	0	200	mA
Maximum VCC Current	VCCI	0	80	mA
Operating Junction Temperature Range (Note 1)	TJ	−40	150	°C
Operating Ambient Temperature Range	TA	−40	100	°C
Storage Temperature Range	TSTG	−55	150	°C
Thermal Characteristics (Note 2) QFN 32 5mm x 5mm Maximum Power Dissipation @ TA = 25°C Thermal Resistance Junction−to−Air with Solder	 PD RΘJA	 4.1 30		 W °C/W
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3)	RF	260 Peak		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The maximum package power dissipation limit must not be exceeded.
2. The value of ΘJA is measured with the device mounted on a 3in x 3in, 4 layer, 0.062 inch FR−4 board with 1.5 oz. copper on the top and bottom layers and 0.5 ounce copper on the inner layers, in a still air environment with T_A = 25°C.
3. 60−180 seconds minimum above 237°C.

Table 3. ELECTRICAL CHARACTERISTICS
(V1 = 12 V, V_{out} = 5.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V1 Operating Input Voltage	V1		4.5		28	V
VDRV Operating Input Voltage	VDRV		4.5	5	5.5	V
VCC UVLO Rising Threshold	VCC_{START}			4.26		V
UVLO Hysteresis for VCC	$VCCV_{HYS}$	Falling Hysteresis		320		mV
VDRV UVLO Rising Threshold	$VDRV_{START}$			4.27		V
UVLO Hysteresis for VDRV	$VDRV_{HYS}$	Falling Hysteresis		340		mV
VCC Output Voltage	VCC	With no external load	4.96	5		V
VCC Drop Out Voltage	VCCDROOP	30 mA load		160		mV
VCC Output Current Limit	$IOUT_{VCC}$	VCC Loaded to 4.3 V	80	97		mA
V1 Shutdown Supply Current	IVCC_SD	EN = 0 V, 4.2 V ≤ V1 ≤ 28 V		6.7	7.7	mA
VDRIVE Switching Current Buck	IV1_SW	EN = 5 V, Cgate = 2.2 nF, VSW = 0 V, FSW = 600 kHz		15		mA

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V1 = 12 V, V_{out} = 5.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VOLTAGE OUTPUT						
Voltage Output Accuracy	VFB	DAC_TARGET = 00110010 DAC_TARGET = 01111000 DAC_TARGET = 11001000	0.495 1.188 1.98	0.5 1.2 2.0	0.505 1.212 2.02	V
Voltage Accuracy Over Temperature	VFB_T	−40°C < T_A < 100°C VFB > 0.5 V VFB < 0.5 V	 −1.0 −5		 1.0 5	 % mV
	VFB_R	T_A = 25°C VFB > 0.5 V	 −0.45		 0.45	 %
TRANSCONDUCTANCE AMPLIFIER						
Gain Bandwidth Product	GBW	3 db (Note 4)		5.2		MHz
Transconductance	GM1	Default		500		μS
Max Output Source Current limit	GMSOC		60	83		μA
Max Output Sink Current limit	GMSIC		60	84		μA
Voltage Ramp	Vramp			0.7		V
INTERNAL BST DIODE						
Forward Voltage Drop	VFBOT	I_F = 10 mA, T_A = 25°C	0.35	0.46	0.55	V
Reverse−Bias Leakage Current	DIL	BST−VSW = 5 V V_{SW} = 28 V, T_A = 25°C		0.05	1	μA
BST−VSW UVLO	$BST1_{UVLO}$	Rising (Note 4)		3.5		V
BST−VSW Hysteresis	BST_{HYS}	(Note 4)		300		mV
OSCILLATOR						
Oscillator Frequency	FSW_0	FSW = 000, default	528	600	672	kHz
	FSW_1	FSW = 001	132	150	168	kHz
	FSW_7	FSW = 110	1056	1200	1344	kHz
Oscillator Frequency Accuracy	FSWE		−12		12	%
Minimum On Time	MOT	Measured at 10% to 90% of VCC, −40°C < T_A < 100°C		50		ns
Minimum Off Time	MOFT	Measured at 90% to 10% of VCC, −40°C < T_A < 100°C		90		ns
INT THRESHOLDS						
Interrupt Low Voltage	VINTI	IINT(sink) = 2 mA			0.2	V
Interrupt High Leakage Current	INII	3.3 V		3	100	nA
Interrupt Startup Delay	INTPG	Soft Start end to PG positive edge		2.1		ms
Interrupt Propagation Delay	PGI	Delay for power good in		3.3		ms
	PGO	Delay for power good out		100		ns
Power Good Threshold	PGTH	Power Good in from high		105		%
	PGTH	Power Good in from low		95		%
	PGTHYS	PG falling hysteresis		2.5		%
FB Overvoltage Threshold	FB_OV			140		%
Overvoltage Propagation Delay	VFB_OVDL			1 Cycle		

4. Ensured by design. Not production tested.

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V1 = 12 V, V_{out} = 5.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
EXTERNAL CURRENT SENSE (CS1,CS2)						
Positive Current Measurement High	CS10	CSP1−CSN1 or CSP2−CSN2 = 100 mV		500		μA
Transconductance Gain Factor	CSGT	Current Sense Transconductance Vsense = 1 mV to 100 mV		5		mS
Transconductance Deviation	CSGE		−20		20	%
Current Sense Common Mode Range	CSCMMR		3		28	V
−3dB Small Signal Bandwidth	CSBW	VSENSE (AC) = 10 mVPP, RGAIN = 10 kΩ (Note 4)		30		MHz
Input Sense Voltage Full Scale	ISVFS				100	mV
CS Output Voltage Range	CSOR	VSENSE = 100 mV Rset = 6k	0		3	V
EXTERNAL CURRENT LIMIT (CLIND)						
Current Limit Indicator Output Low	CLINDL	Input current = 500 μA		10	100	mV
Current Limit Indicator Output High Leakage Current	ICLINDH	Pull up to 5 V		500		μA
INTERNAL CURRENT SENSE						
Internal Current Sense Gain for PWM	ICG	CSPx−CSNx = 100 mV	9.2	9.9	10.5	V/V
Positive Peak Current Limit Trip	PPCLT	INT_CL = 00	34	39	44	mV
SWITCHING MOSFET DRIVERS						
HSG Pullup Resistance	HSG_PU	BST−VSW = 4.5 V		2.9		Ω
HSG Pulldown Resistance	HSG_PD	BST−VSW = 4.5 V		1.1		Ω
LSG Pullup Resistance	LSG_PU	LSG −PGND = 2.5 V		3.4		Ω
LSG Pulldown Resistance	LSG_PD	LSG −PGND = 2.5 V		1.1		Ω
HSG Falling to LSG Rising Delay	HSLSD			15		ns
LSG Falling to HSG Rising Delay	LSHSD			15		ns
CFET						
CFET Drive Voltage	CFETDV			VCC		V
Source/Sink Current	CFETSS	CFET clamped to 2 V		2		μA
Pull Down Delay	CFETD	Measured at 10% to 90% of VCC, −40°C < T_A < 100°C		10		ms
CFET Pull Down Resistance	CFETR	Measured with 1 mA Pull up Current, after 10 ms rising edge delay		1.3		kΩ
SLEW RATE/SOFT START						
Charge Slew Rate	SLEWP	Slew = 00, FB = 0.1 VOUT Slew = 11, FB = 0.1 VOUT		0.6 4.8		mV/μs
Discharge Slew Rate	SLEWN	Slew = 00, FB = 0.1 VOUT Slew = 11, FB = 0.1 VOUT		−0.6 −4.8		mV/μs
DEAD BATTERY/VCONN						
Dead Battery Input Voltage Range	VDB		4.5	5	5.25	V
Dead Battery Output Voltage	VIO	VDB = 5 V, −40°C < T_A < 100°C, Output Current 32 mA	4	4.7	5	V
Dead Battery Current Limit	DB_LIM	VDB = 5 V, DBOUT > 2 V	29	57		mA

4. Ensured by design. Not production tested.

Table 3. ELECTRICAL CHARACTERISTICS (continued)
($V1$ = 12 V, V_{out} = 5.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ENABLE						
EN High Threshold Voltage	ENHT	EN_MASK = ENPU = ENPOL = 0		800	820	mV
EN Low Threshold Voltage	ENLT		640	667		mV
EN Pull Up Current	IEN_UP	EN = 0 V		5		μA
EN Pull Down Current	IEN_DN	EN = VCC		5		μA
I²C INTERFACE						
Voltage Threshold	I2CVTH		0.95	1	1.05	V
Propagation Delay	I2CPD	(Note 4)		25		ns
Communication Speed	I2CSP	(Note 4)			1	MHz
INTERNAL ADC						
Range	ADCRN		0		2.55	V
LSB Value	ADCLSB	(Note 4)		20		mV
Error	ADCFE	(Note 4)			1	LSB
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TSD	(Note 4)		151		°C
Thermal Shutdown Hysteresis	TSDHYS	(Note 4)		28		°C
PDRV						
PDRV Operating Range			0		28	V
PDRV Leakage Current	PDRV_IDS	FET OFF, VPDRV = 28 V		480		nA
PDRV Saturation Voltage	PDRV_VDS	ISNK = 10 mA		0.20		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Ensured by design. Not production tested.

APPLICATION INFORMATION

Feedback and Output Voltage Profile

The feedback of the converter output voltage is connected to the FB pin of the device through a resistor divider. Internally FB is connected to the inverting input of the internal transconductance error amplifier. The non−inverting input of the gm amplifier is connected to the internal reference. The internal reference voltage is by default 0.5 V. Therefore, for example, a 10:1 resistor divider from the converter output to the FB will set the output voltage to 5 V in default. The reference voltage can be adjusted with 10 mV(default) or 5 mV steps from 0.3 V to 2.55 V through the voltage profile register (01H), which makes the continuous output voltage profile possible through an external resistor divider. For example, if the external resistor divider has a 10:1 ratio, the output voltage profile will be able to vary from 3 V to 25.5 V with 100 mV steps but not above V1 voltage.

Table 4. VOLTAGE PROFILE SETTINGS

dac_taget								dac_target_LSB	Voltage Profile Hex Value	Reference Voltage (mV)
bit_8	bit_7	bit_6	bit_5	bit_4	bit_3	bit_2	bit_1			
0	0	0	0	0	0	0	0	0	00H	Reserved
0	0	0	0	0	0	0	0	1	00H	Reserved
0	0	0	0	0	0	0	1	0	01H	Reserved
…	…	…	…	…	…	…	…	…	…	…
0	0	0	1	1	1	0	1	1	1DH	Reserved
0	0	0	1	1	1	1	0	0	1EH	300
0	0	0	1	1	1	1	0	1	1EH	305
…	…	…	…	…	…	…	…	…	…	…
0	0	1	1	0	0	1	0	0	32H	500 (Default)
…	…	…	…	…	…	…	…	…	…	…
1	1	0	0	1	0	0	0	0	C8H	2000
…	…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	0	FFH	2550
1	1	1	1	1	1	1	1	1	FFH	2555

Transconductance Voltage Error Amplifier

To maintain loop stability under a large change in capacitance, the NCP81231 can change the gm of the internal transconductance error amplifier from 87 μS to 1000 μS allowing the DC gain of the system to be increased more than a decade triggered by the adding and removal of the bulk capacitance or in response to another user input. The default transconductance is 500 μS.

Table 5. AVAILABLE TRANSCONDUCTANCE SETTING

AMP_2	AMP_1	AMP_0	Amplifier GM Value (μS)
0	0	0	87
0	0	1	100
0	1	0	117
0	1	1	333
1	0	0	400
1	0	1	500
1	1	0	667
1	1	1	1000

Programmable Slew Rate

The slew rate of the NCP81231 is controlled via the I^2C registers with the default slew rate set to 0.6 mV/μs (FB = 0.1 VOUT, assume the resistor divider ratio is 10:1) which is the slowest allowable rate change. The slew rate is used when the output voltage starts from 0 V to a user selected profile level, changing from one profile to another,

or when the output voltage is dynamically changed. The output voltage is divided by a factor of the external resistor divider and connected to FB pin. The 9 Bit DAC is used to increase the reference voltage in 10 or 5 mV increments. The slew rate is decreased by using a slower clock that results in a longer time between voltage steps, and conversely increases by using a faster clock. The step monotonicity depends on the bandwidth of the converter where a low bandwidth will result in a slower slew rate than the selected value. The available slew rates are shown in Table 6. The selected slew rate is maintained unless the current limit is tripped, in which case the increased voltage will be governed by the positive current limit until the output voltage falls or the fault is cleared.

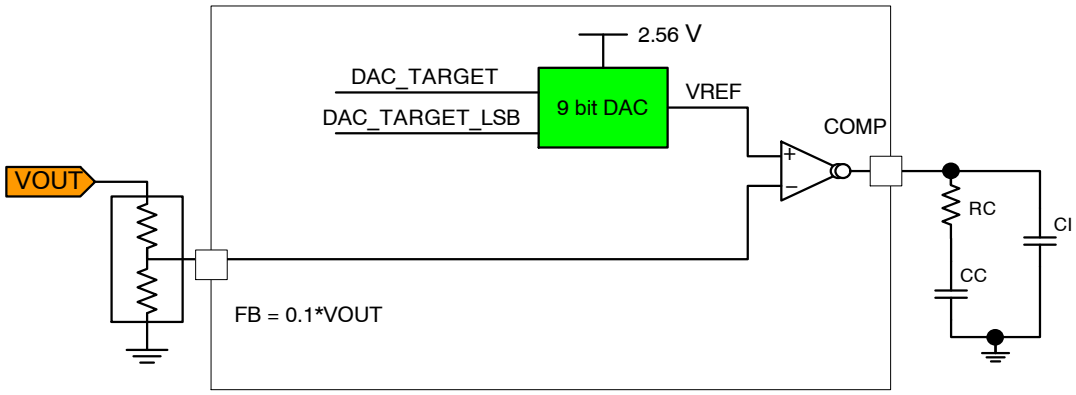


Figure 5. Slew Rate Limiting Block Diagram and Waveforms

Table 6. SLEW RATE SELECTION

Slew Bits	Soft Start or Voltage Transition (FB = 0.1*VOUT)
Slew_0	0.6 mV/μs
Slew_1	1.2 mV/μs
Slew_2	2.4 mV/μs
Slew_3	4.8 mV/μs

The discharge slew rate is accomplished in much the same way as the charging except the reference voltage is decreased rather than increased.

Soft Start

During a 0 V soft start, standard converters can start in synchronous mode and have a monotonic rising of output voltage. If a prebias exists on the output and the converter starts in synchronous mode, the prebias voltage will be discharged. The NCP81231 controller ensures that if a prebias is detected, the soft start is completed in a non−synchronous mode to prevent the output from discharging.

It takes at least 3.3 ms for the digital core to reset all the registers, so it is recommended not to restart a soft start until at least 3.3 ms after the output voltage ramp down to steady state.

Frequency Programming

The switching frequency of the NCP81231 can be programmed from 150 kHz to 1.2 MHz via the I^2C interface. The default switching frequency is set to 600 kHz. Once the part is enabled, the frequency is set and cannot be changed while the part remains enabled. The part must be disabled with no switching prior to writing the frequency bits into the appropriate I^2C register.

Table 7. FREQUENCY PROGRAMMING TABLE

Name	Bit	Definition	Description
Freq1	03H [2:0]	Frequency Setting	3 Bits that Control the Switching Frequency from 150 kHz to 1 MHz. 000: 600 kHz 001: 150 kHz 010: 300 kHz 011: 450 kHz 100: 750 kHz 101: 900 kHz 110: 1.2 MHz 111: Reserved

100% Duty Cycle Operation

NCP81231 can operate in a 100% duty cycle mode when the high side switch works as a bypass switch. A detection circuit will constantly monitor the high side gate voltage and turn on low side switch to refresh the boost capacitor when the voltage across the boost capacitor is below the boost UVLO voltage. If the system stays in the 100% duty cycle operation, the output will always follow the input regardless the COMP voltage and COMP is likely to creep up. If a fast COMP recovery is required, the following clamping circuitry can be considered with a larger than 1.5 V clamping voltage set as the target.

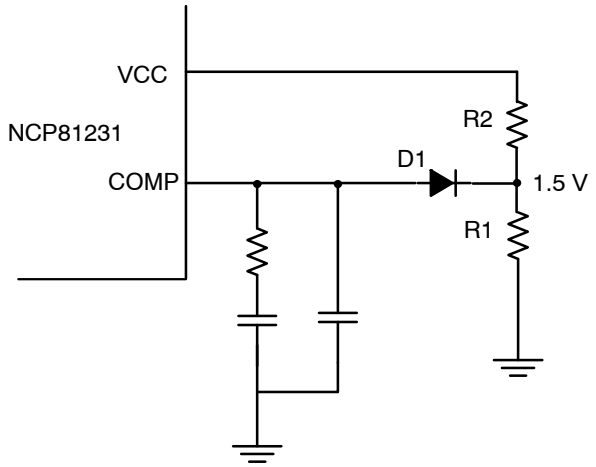


Figure 6. External Comp Clamping Circuit

Current Sense Amplifiers

Internal differential amplifiers measure the potential between the terminal CSP1/CSN1 or CSP2/CSN2. The potential difference between CSPx and CSNx is level shifted from the high voltage domain to the low voltage VCC domain.

Both current sense signals can be monitored externally by CS1 and CS2 pins. They are fixed gm amplifier outputs, allowing users to set output gain by shunting resistors. CS1 correlates to the CSP1/CSN1 reading, CS2 correlates to the CSP2/CSN2 reading. When not used, CSP1/CSN1 pin can be shorted therefore CS1 reading is omitted.

NCP81231 also uses CSP2/CSN2 current sense signal for current mode modulation and cycle by cycle positive and negative peak current limiting. The inputs of CSP2/CSN2 can be a current sense resistor or configured for inductor DCR sensing shown as Figure 8. A resistor Rs1 connects from switch node to CSP2 and Rs2 connects from the output voltage to CSN2 respectively. Two capacitors, Cs1 and Cs2, are common mode filtering capacitors from CSP2 and CSN2 to the ground. Choose Rs1=Rs2=Rs, Cs1=Cs2=Cs; In order to replicate inductor current sensing information, Rs*Cs needs to be equal or slightly higher than the ratio of output inductance over its DC resistance or L/DCR. Additional resistor network may be added to expand the actual current limit tripping range.

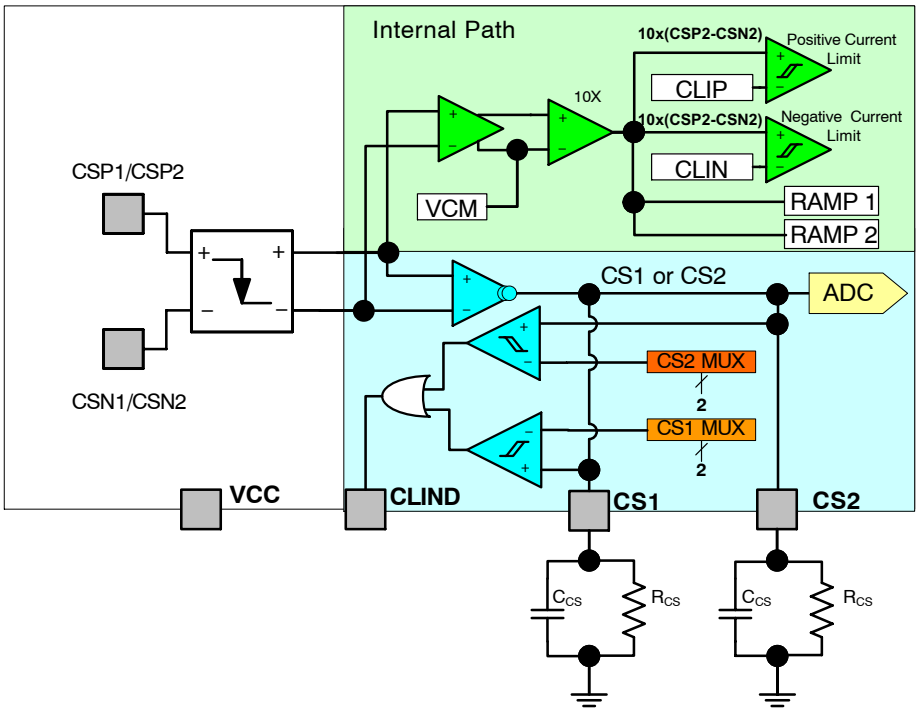


Figure 7. Block Diagram for Current Sense Channel

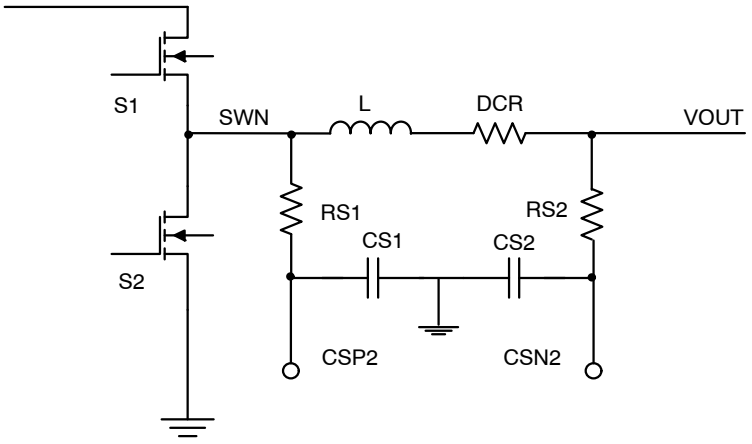


Figure 8. Inductor DCR Sensing Using CSP2/CSN2

Positive Current Limit Internal Path

The NCP81231 has a pulse by pulse current limiting function activated when a positive current limit triggers. When a positive current limit is triggered, the current pulse is truncated. For NCP81231, the CSP2/CSN2 pins will be the positive current limit sense channel.

The S1 switch is turned off to limit the energy during an over current event. The current limit is reset every switching cycle and waits for the next positive current limit trigger. In this way, current is limited on a pulse by pulse basis. Pulse by pulse current limiting is advantageous for limiting energy into a load in over current situations but are not up to the task of limiting energy into a low impedance short. To address the low impedance short, the NCP81231 will go to latch up mode if pulse by pulse current limiting continues for more than 4 cycles. Toggling the enable pin or resetting the input voltage (V1) will clear the latched OCP fault.

Table 8. INTERNAL PEAK CURRENT LIMIT

CLIP_1	CLIP_0	CLIM delta Value (mV)	CSP2−CSN2 (mV)	Trip Current Inductor DCR = 2 mΩ (A)
0	0	380	38	19
0	1	230	23	11.5
1	0	110	11	5.5
1	1	700	70	35

External Path (CS1, CS2, CLIND)

The voltage drop across CSP1/CSN1 or CSP2/CSN2 as a result of the load can be observed on the CS1 and CS2 pins. The voltage drop is converted into a current by a transconductance amplifier with a typical GM of 5 mS. The final gain of the output is determined by the end users selection of the R_{CS} resistors or the inductor DCR resistor. The output voltage of the CS pin can be calculated from Equation 1. The user must be careful to keep the dynamic range below 3.0 V when considering the maximum short circuit current.

$$V_{CS} = (I_{LOAD\_MAX} * R_{SENSE} * Trans) * R_{CS} \rightarrow$$

$$\rightarrow 2.967\ V = (8.5\ A * 5\ m\Omega * 5\ mS) * 13.96\ k\Omega$$

$$R_{CS} = \frac{V_{CS}}{I_{LOAD} * R_{SENSE} * Trans} \rightarrow$$

$$\rightarrow 13.96\ k\Omega = \frac{2.967\ V}{8.5\ A * 5\ m\Omega * 5\ mS} \quad \text{(eq. 1)}$$

The speed and accuracy of the dual amplifier stage allows the reconstruction of the input and output current signal, creating the ability to limit the peak current. If the user would like to limit the mean DC current of the switch, a capacitor can be placed in parallel with the R_{CS} resistors.

The external CS voltages are connected to 2 high speed low offset comparators. The comparators output can be used to suspend operation until reset or restart of the part depending on I^2C configuration. When one of the comparators trips if not masked, the external CLIND flag is triggered to indicate that the internal comparator has exceeded the preset limit. The default comparator setting is 250 mV which is a limit of 500 mA with a current sense resistor of 5 mΩ and an R_{CS} resistor of 20 kΩ. The block diagram in Figure 9 shows the programmable comparators and the settings are shown in Table 9.

CLIND may misbehave when EN toggles. It is because the internal analog circuit is not fully functional when EN is just asserted. One solution is to force the CLIND low during EN is low and release CLIND after certain time after EN goes high.

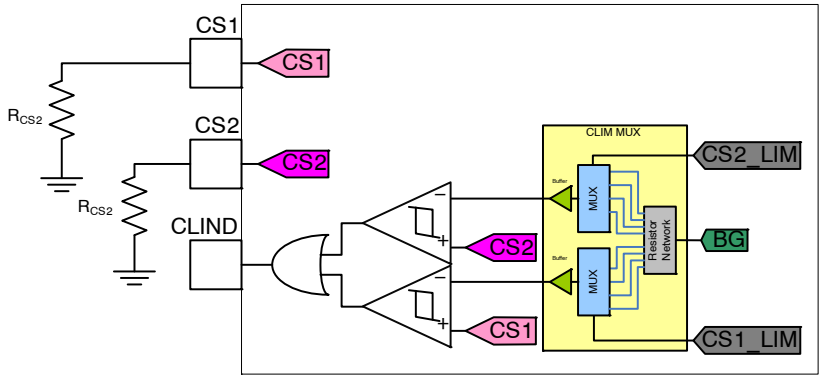


Figure 9. Block Diagram for CLIM Comparator

Table 9. REGISTER SETTING FOR THE CLIM COMPARATORS

CLIMx_1	CLIMx_0	CSx_LIM (V)	Current at RSENSE = 5 mΩ RSET = 20 kΩ (A)	Current at RSENSE = 5 mΩ RSET = 10 kΩ (A)
0	0	0.25	.5	1
0	1	0.75	1.5	3
1	0	1.5	3	6
1	1	2.5	5	10

Overvoltage Protection (OVP)

When the divided output voltage is 140% (typical) above the internal reference voltage, a latched OV fault will be triggered. At 0 V reference voltage, it's easy to trigger OVP falsely. So one should avoid using output voltage profile under 0.3 V for safety in normal operation. When 0 V output voltage is needed, one can disable NCP81231 by pulling EN pin down, instead of setting output voltage profile to 0 via I2C. Toggling the enable pin will not clear the latched OVP fault. Only resetting the input voltage (V1) can clear it.

Power Good Monitor (PG)

NCP81231 provides two window comparators to monitor the internal feedback voltage. The target voltage window is ±5% of the reference voltage (typical). Once the feedback voltage is within the power good window, a power good indication is asserted once a 3.3 ms timer has expired. If the feedback voltage falls outside a ±7.5% window for greater than 1 switching cycle, the power good register is reset. Power good is indicated on the INT pin if the related I^2C register is set to display the PG state. During startup, INT is set until the feedback voltage is within the specified range for 3.3 ms.

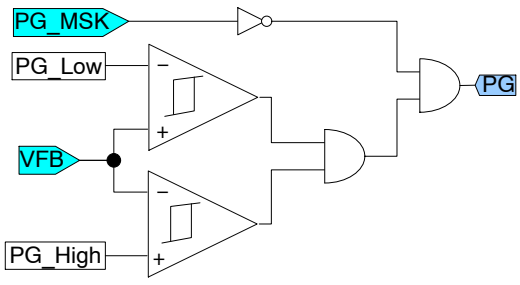


Figure 10. PG Block Diagram

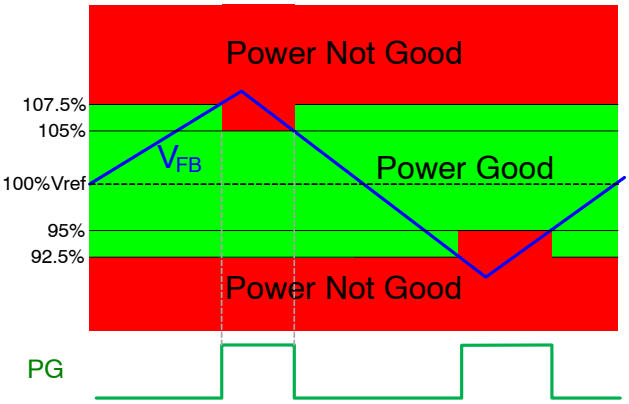


Figure 11. PG Diagram

Table 10. POWER GOOD MASKING

PG_MSK	Description
0	PG Action and Indication Unmasked
1	PG Action and Indication Masked

Thermal Shutdown

The NCP81231 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold (typically 150°C), all MOSFETs will be driven to the off state, and the part will wait until the temperature decreases to an acceptable level. The fault will be reported to the fault register and the INT flag will be set unless it is masked. When the junction temperature drops below 125°C (typical), the part will discharge the output voltage to 0 V.

CFET Turn On

The CFET is used to engage the output bulk capacitance after successful negotiations between a consumer and a provider. The USB Power Delivery Specification requires that no more than 30 μF of capacitance be present on the VBUS rail when sinking power. Once the consumer and provider have completed a power role swap, a larger capacitance can be added to the output rail to accommodate a higher power level. The bulk capacitance must be added in such a way as to minimize current draw and reduce the voltage perturbation of the bus voltage. The NCP81231 incorporates a right drive circuit that regulates current into the gate of the MOSFET such that the MOSFET turns on slowly reducing the drain to source resistance gradually. Once the transition from high to low has occurred in a controlled way, a strong pulldown driver is used to ensure normal operation does not turn on the power N−MOSFET engaging the bulk capacitance. The CFET must be activated through the I^2C interface where it can be engaged and disengaged. The default state is to have the CFET disengaged.

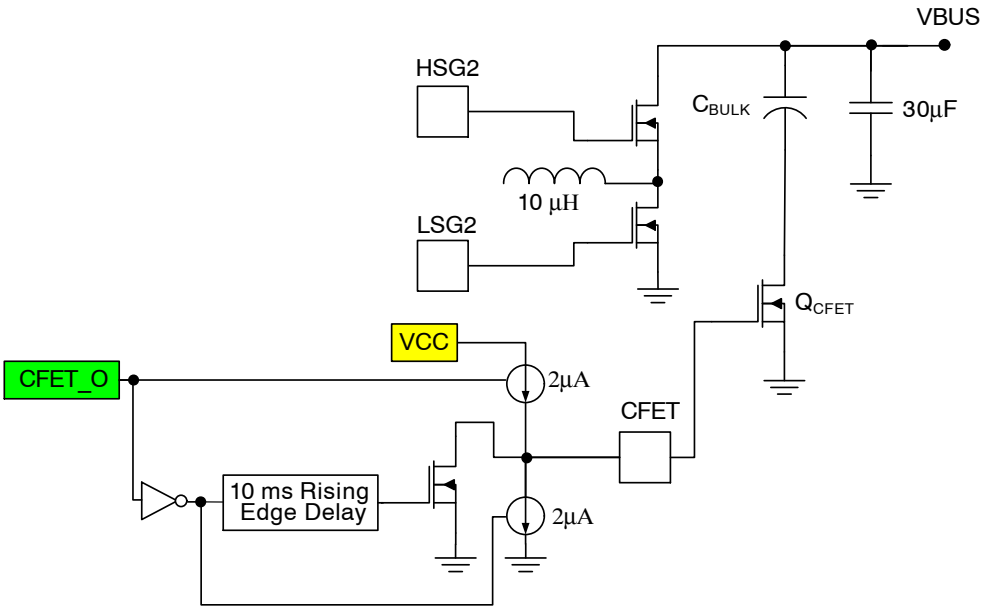


Figure 12. CFET Drive

Table 11. CFET ACTIVATION TABLE

CFET_0	Description
0	CFET Pin Pulldown
1	CFET Pin Pull Up

PFET Drive

The PMOS drive is an open drain output used to control the turn on and turn off of PMOSFET switches at a floating potential or to create an external discharging path. The RDSon of the pulldown NMOSFET is typically 20 Ω allowing the user to quickly turn on for a fast output discharge or to control the external pass FETs.

Table 12. PFET ACTIVATION TABLE

PFET_DRV	Description
0	NFET OFF (Default)
1	NFET ON

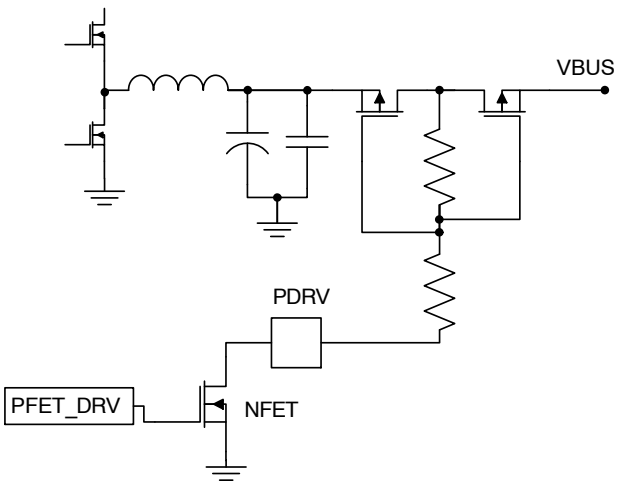


Figure 13. PFET Drive

Analog to Digital Converter

The analog to digital converter is a 7−bit A/D which can be used as an event recorder, an input voltage sampler, output voltage sampler, input current sampler, or output current sampler. The converter digitizes real time data during the sample period. The internal precision reference is used to provide the full range voltage; in the case of input voltage V1 or the feedback voltage FB (with 10:1 external resistor divider) the full range is 0 V to 25.5 V. V1 is internally divided down by 10 before it is digitized by the ADC, thus the range of the measurement is 0 V−2.55 V, same as FB. The resolution of the V1 and FB voltage is 20 mV at the analog mux, but since the voltage is divided by 10 output voltage resolution will be 200 mV. When CS1 and CS2 are sampled, the range is 0 V−2.55 V. The resolution will be 20 mV in the CS monitoring case. The actual current can be calculated by dividing the CS1 or CS2 values with the factor of Rsense*5mS*RCSx, the total gain from the current input to the external current monitoring outputs.

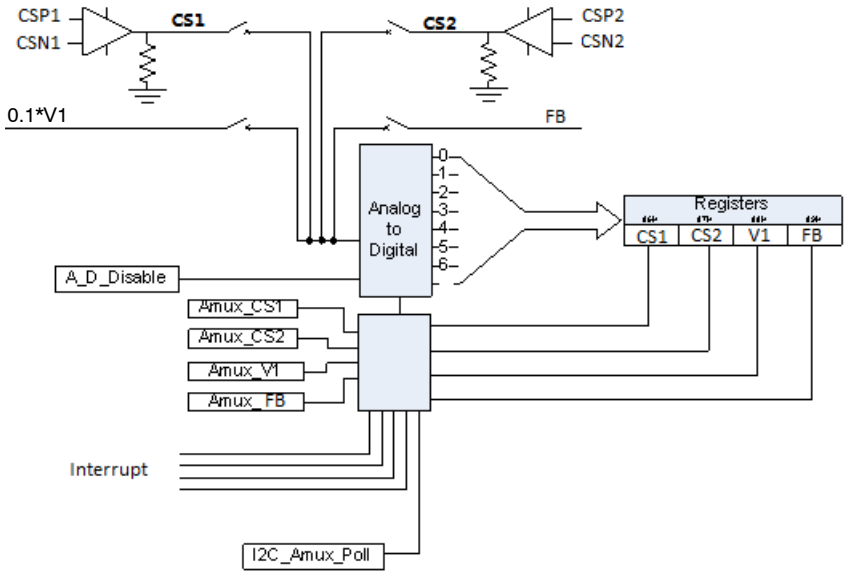


Figure 14. Analog to Digital Converter

Table 13. ADC BYTE

	MSB	5	4	3	2	1	LSB
DATA	D6	D5	D4	D3	D2	D1	D0

Table 14. REGISTER SETTING FOR ENABLING DESIRED ADC BEHAVIOUR

ADC_1	ADC_0	Description
0	0	Sets Amux to VFB
0	1	Sets Amux to V1
1	0	Sets Amux to CS2
1	1	Sets Amux to CS1

Interrupt Control

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected. Individual bits generating interrupts will be set to 1 in the INTACK register (I^2C read only registers), indicating the interrupt source. All interrupt sources can be masked by writing 1 in register INTMSK. Masked sources will never generate an interrupt request on the INT pin. The INT pin is an open drain output. A non−masked interrupt request will result in the INT pin being driven high. Figure 15 illustrates the interrupt process.

The interrupt source registers (14h,15h) always read 0 when any interrupt happens. The solution is to first keep Int_mask_XXX registers (09h) low by default. INT can toggle after any fault happens. Then set int_mask_XXX registers to high, it will flag the corresponding interrupt source registers if the fault is still there. Now the interrupt source registers can be read. In the end, set int_mask_XXX registers to low again after reading interrupt status registers.

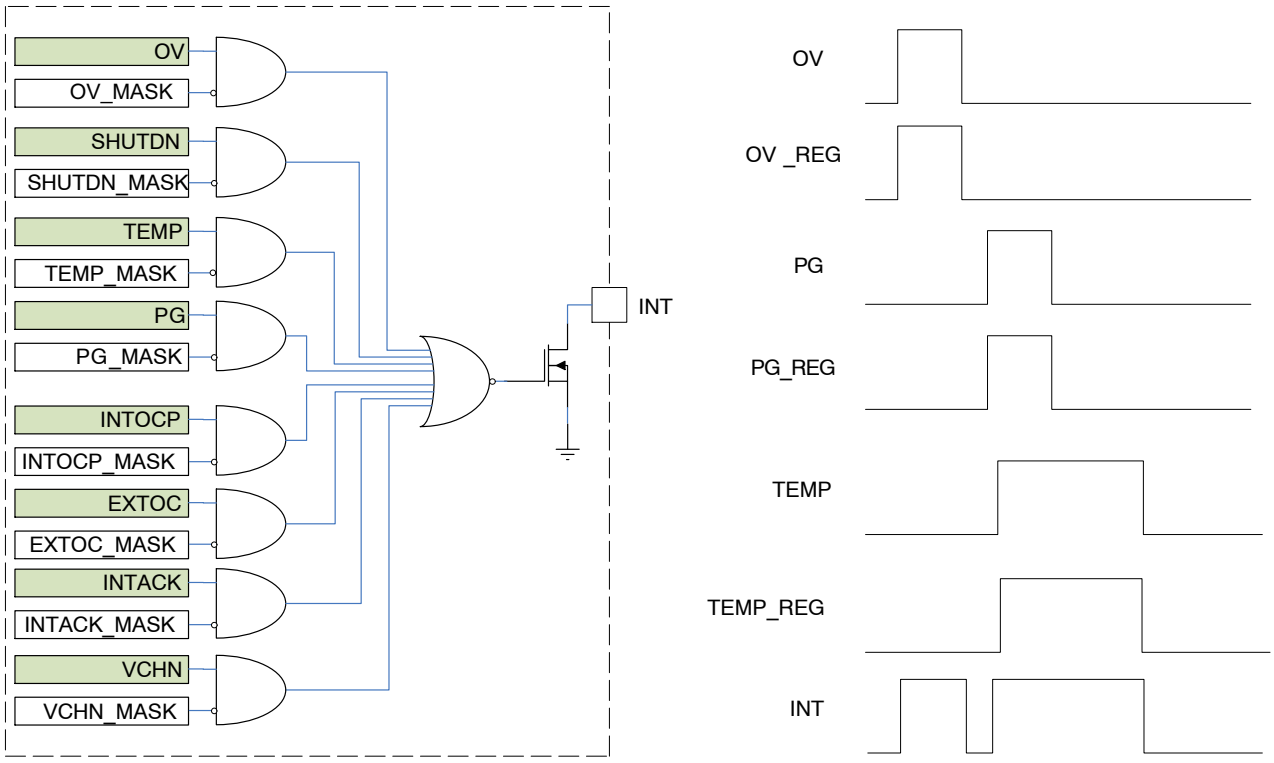


Figure 15. Interrupt Logic

Table 15. INTERPRETATION TABLE

Interrupt Name	Description
OV	Output Over Voltage
Shutdown	Shutdown Detection (EN=low)
TEMP	IC Thermal Trip
PG	Power Good Trip Thresholds Exceeded
INTOCP	Internal Current Limit Trip
EXTOC	External Current Trip from CLIND
VCHN	Output Negative Voltage Change
INTACK	I2C ACK signal to the host

I²C Address

The default address is set to 77h.

Table 16. I²C ADDRESS

I²C Address	Hex	A6	A5	A4	A3	A2	A1	A0
ADD0 (default)	0x77	1	1	1	0	1	1	1

I²C interface

The I²C interface can support 5 V TTL, LVTTL, 2.5 V and 1.8 V interfaces with two precision SCL and SDA comparators with 1V thresholds shown in Figure 16. The part cannot support 5 V CMOS levels as there can be some ambiguity in voltage levels.

I²C Compatible Interface

The NCP81231 can support a subset of I²C protocol as detailed below. The NCP81231 communicates with the external processor by means of a serial link using a 400 kHz up to 1.2 MHz I²C two−wire interface protocol. The I²C interface provided is fully compatible with the Standard, Fast, and High−Speed I²C modes. The NCP81231 is not intended to operate as a master controller; it is under the control of the main controller (master device), which controls the clock (pin SCL) and the read or write operations through SDA. The I²C bus is an addressable interface (7−bit addressing only) featuring two Read/Write addresses.

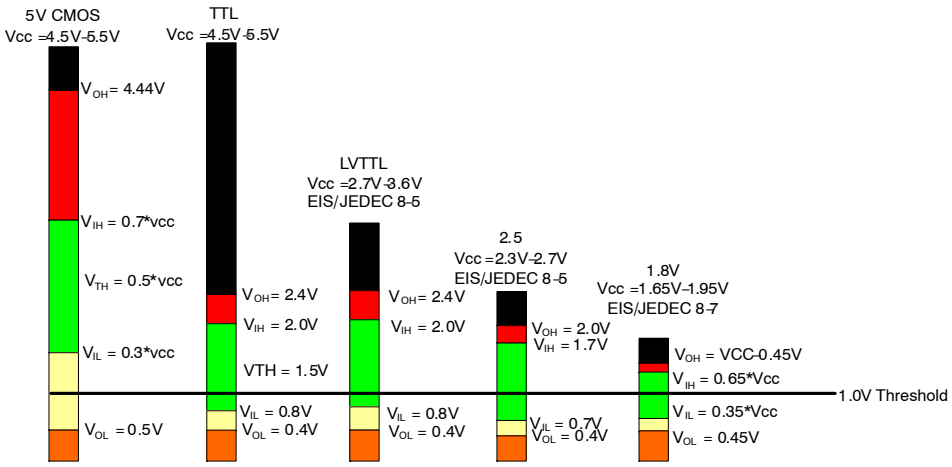


Figure 16. I²C Thresholds and Comparator Thresholds

I²C Communication Description

The first byte transmitted is the chip address (with the LSB bit set to 1 for a Read operation, or set to 0 for a Write operation). Following the 1 or 0, the data will be:

- In case of a Write operation, the register address (@REG) pointing to the register for which it will be written is followed by the data that will written in that location. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented, and the next data byte is placed in the location pointed to @REG + 1 ..., etc.
- In case of a Read operation, the NCP81231 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.

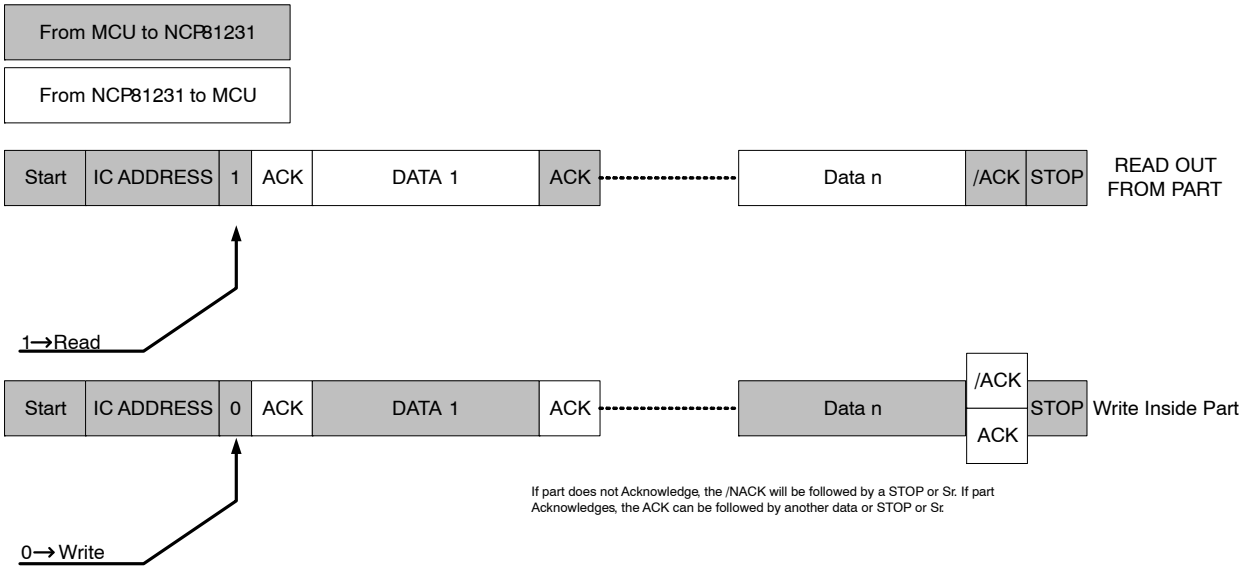


Figure 17. General Protocol Description

Read out from part

The master will first make a “Pseudo Write” transaction with no data to set the internal address register. Then, a stop then start or a repeated start will initiate the Read transaction from the register address the initial Write transaction was pointed to:

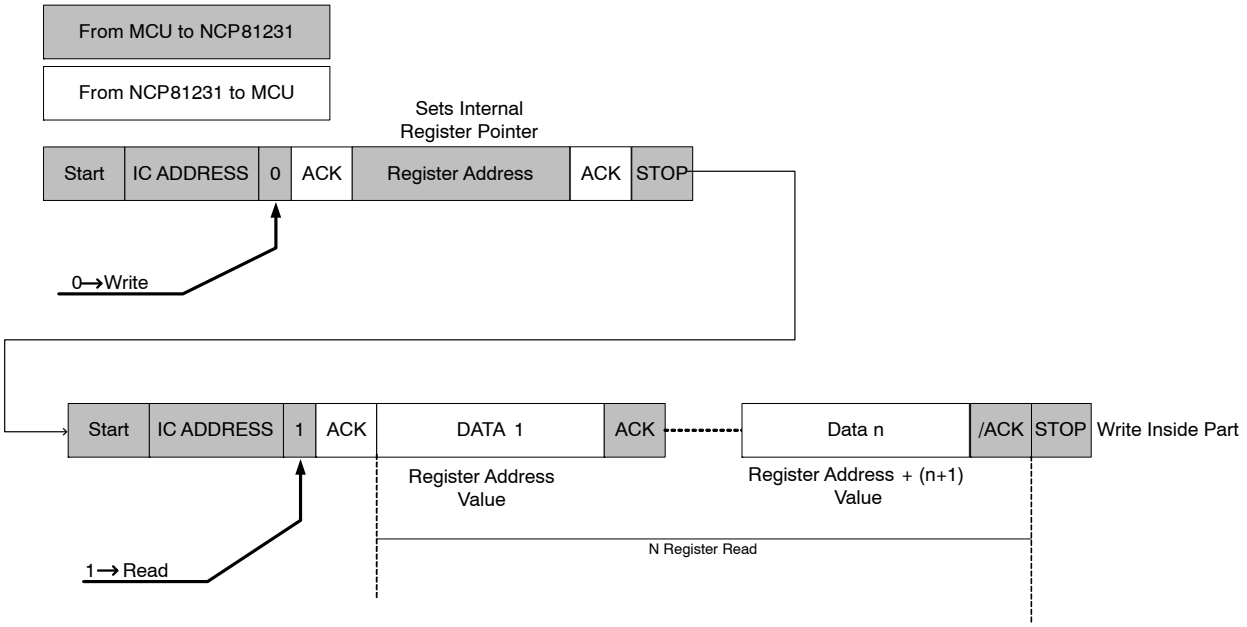


Figure 18. Read Out From Part

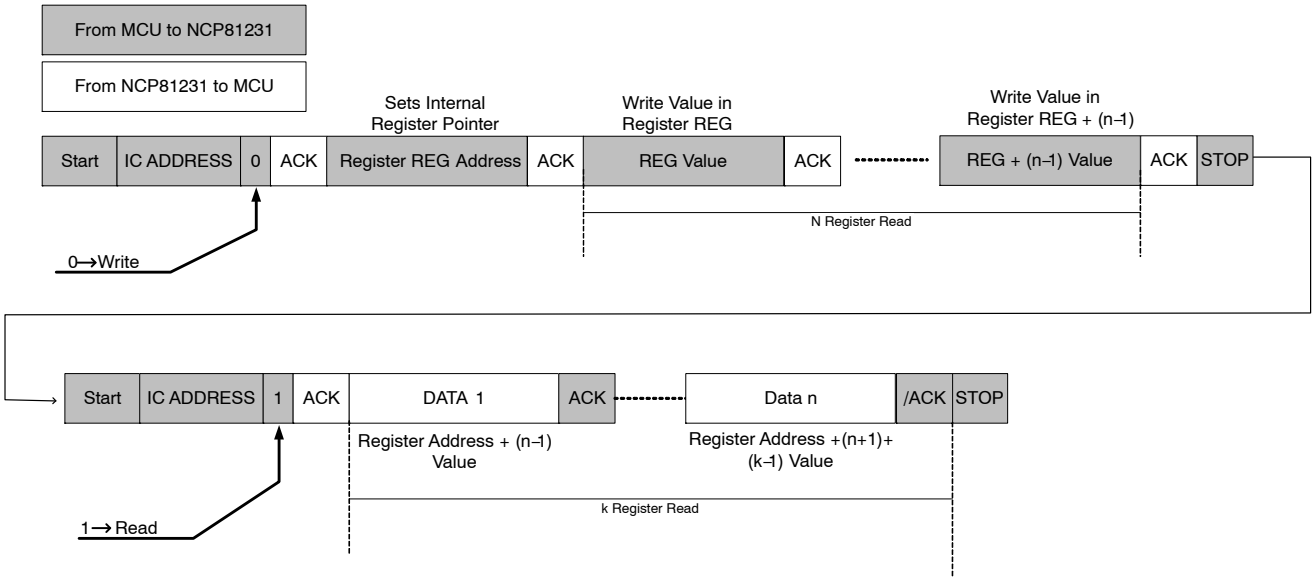


Figure 19. Write Followed by Read Transaction

Write In Part

Write operation will be achieved by only one transaction. After the chip address, the MCU first data will be the internal register desired to access, the following data will be the data written in REG, REG + 1, REG + 2, ..., REG + (n−1).

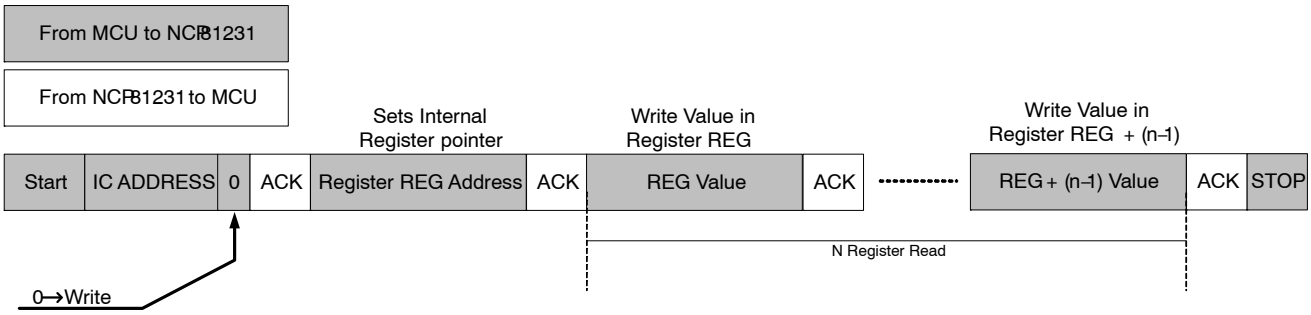


Figure 20. Write in n Registers

DESIGN CONSIDERATIONS

dv/dt Induced False Turn On

In synchronous buck converters, there is a well−known phenomenon called “low side false turn−on,” or “dv/dt induced turn on”, which can be potentially dangerous for the switch itself and the reliability of the entire converter.

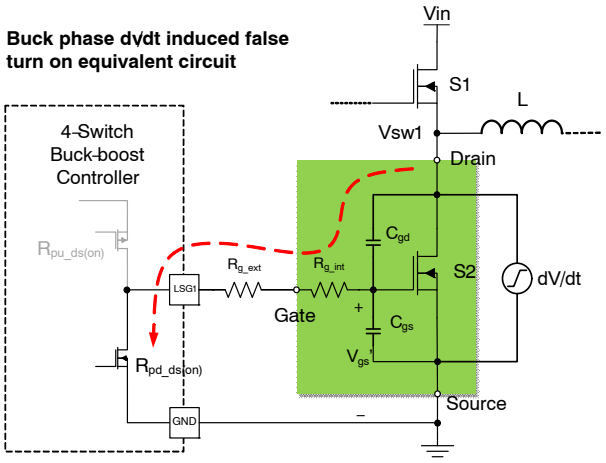


Figure 21. dv/dt Induced False Turn−on Equivalent Circuit of a Buck Converter

Figure 21 shows false turn on equivalent circuit of the buck converter at the moment a positive dv/dt transition appears across the drain−to−source junction. The detailed analysis of this phenomenon can be found in Gate Driver Design Considerations for 4−Switch Buck−Boost Converters.

Select the Switching Power MOSFET

The MOSFETs used in the power stage of the converter should have a maximum drain−to−source voltage rating that exceeds the sum of steady state maximum drain−to−source voltage and the turn−off voltage spike with a considerable margin (20%~50%).

When selecting the switching power MOSFET, the MOSFET gate capacitance should be considered carefully to avoid overloading the 5 V LDO. For one MOSFET, the allowed maximum total gate charge Q_g can be estimated by Equation 2:

$$Q_g = \frac{I_{driver}}{f_{sw}} \quad \text{(eq. 2)}$$

where I_{driver} is the gate drive current and f_{sw} is the switching frequency.

It is recommended to select the MOSFETs with smaller than 3 nF input capacitance (C_{iss}). The gate threshold voltage should be higher than 1.0 V due to the internal adaptive non−overlap gate driver circuit.

In order to prevent dv/dt induced turn−on, the criteria for selecting a rectifying switch is based on the $Q_{gd}/Q_{gs(th)}$ ratio. $Q_{gs(th)}$ is the gate−to−source charge before the gate voltage reaches the threshold voltage. Lowering C_{gd} will reduce dv/dt induced voltage magnitude. Moreover, it also depends on dt/C_{gs}, V_{ds} and threshold voltage V_{th}. One way of interpreting the dv/dt induced turn−on problem is when V_{ds} reaches the input voltage, the Miller charge should be smaller than the total charge on C_{gs} at the V_{th} level, so that the rectifying switches will not be turned on. Then we will have the following relation:

$$V_{gs} = \frac{C_{gd}}{C_{gd} + C_{gs}} \times V_{ds} < V_{gs(th)} \quad \text{(eq. 3)}$$

$$Q_{gd} < Q_{GS(th)} \quad \text{(eq. 4)}$$

We can simply use Equation 4 to evaluate the rectifying device’s immunity to dv/dt induced turn on. Ideally, the charge Q_{gd} should not be greater than $2*Q_{gs(th)}$ in order to leave enough margin.

Select Gate Drive Resistors

To increase the converter’s dv/dt immunity, the dv/dt control is one approach which is usually related to the gate driver circuit. A first intuitive method is to use higher pull up resistance and gate resistance for the active switch. This would slow down the turn on of the active switch, effectively decreasing the dv/dt. Table 17 shows the recommended value for MOSFETs’ external gate drive resistors.

Table 17. RECOMMENDED VALUE FOR EXTERNAL GATE DRIVE RESISTORS

HSG1	(3.3~5.1)Ω
LSG1	0Ω

An alternative approach is to add an RC snubber circuit to the switching nodes VSW1. This is the most direct way to reduce the dv/dt. The side effect of the above two methods are that losses would be increased because of slow switching speed.

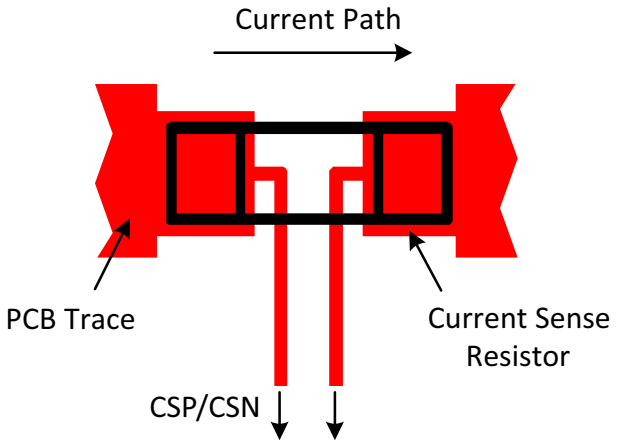
LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction.

- **Current Sensing:** Run two dedicated trace with decent width in parallel (close to each other to minimize the loop area) from the two terminals of the input side or output side current sensing resistor to the IC. Place the common−mode RC filter components in general proximity of the controller.

Route the traces into the pads from the inside of the current sensing resistor. The drawing below shows how to rout the traces.



- **Gate Driver:** Run the high side gate, low side gate and switching node traces in a parallel fashion with decent width. Avoid any sensitive analog signal trace from crossing over or getting close. Recommend routing VSW1 trace to high−side MOSFET source pin instead of copper pour area. The controller should be placed close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. It's OK to place the controller on the opposite side of the MOSFETs.
- **I2C Communication:** SDA and SCL pins are digital pins. Run SDA and SCL traces in parallel and reduce the loop area. Avoid any sensitive analog signal trace or noise source from crossing over or getting close.
- **V1 Pin:** Input for the internal LDO. Place a decoupling capacitor in general proximity of the controller. Run a dedicated trace from system input bus to the pin and do not route near the switching traces.
- **VCC Decoupling:** Place decoupling caps as close as possible to the controller VCC pin. Place the RC filter connecting with VDRV pin in general proximity of the controller. The filter resistor should be not higher than 10 Ω to prevent large voltage drop.
- **VDRV Decoupling:** Place decoupling caps as close as possible to the controller VDRV pin.
- **Input Decoupling:** The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to the input port. Place these capacitors on the same PCB layer with the MOSFETs instead of on different layers and using vias to make the connection.
- **Output Decoupling:** The output capacitors should be as close as possible to the load.
- **Switching Node:** The converter's switching node should be a copper pour to carry the current, but compact because it is also a noise source of electrical and magnetic field radiation. Place the inductor and the switching MOSFETs on the same layer of the PCB.
- **Bootstrap:** The bootstrap cap and an option resistor need to be in general close to the controller and directly connected between pin BST1 and pin VSW1 respectively.
- **Ground:** It would be good to have separated ground planes for PGND and AGND and connect the AGND planes to PGND through a dedicated net tie or 0 Ω resistor.
- **Voltage Sense:** Route a "quiet" path for the input and output voltage sense. AGND could be used as a remote ground sense when differential sense is preferred.
- **Compensation Network:** The compensation network should be close to the controller. Keep FB trace short to minimize it capacitance to ground.

Thermal Layout Considerations

Good thermal layout helps power dissipation and junction temperature reduction.

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor too close to the IC, thus the heat sources are distributed.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

QFN32 5x5, 0.5P
CASE 485CE
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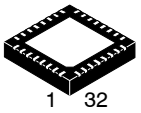
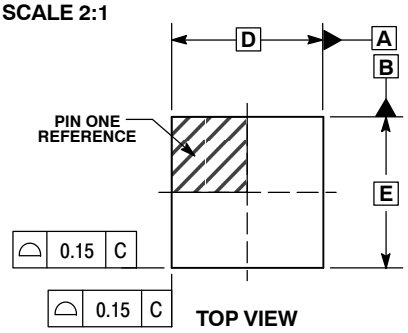
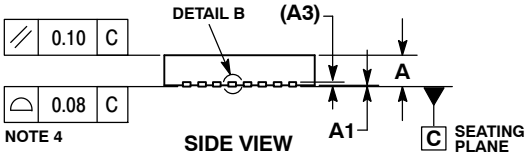


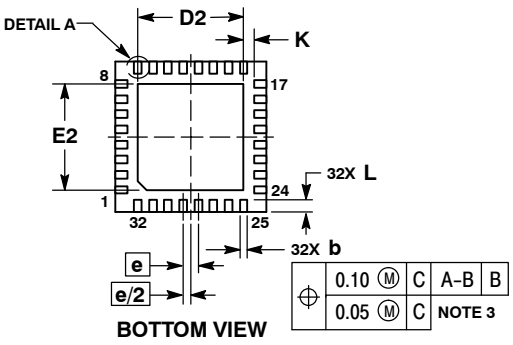
SCALE 2:1



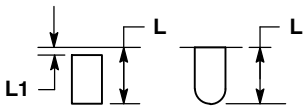
TOP VIEW



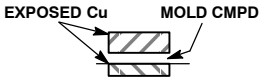
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE
CONSTRUCTIONS

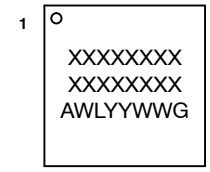


DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

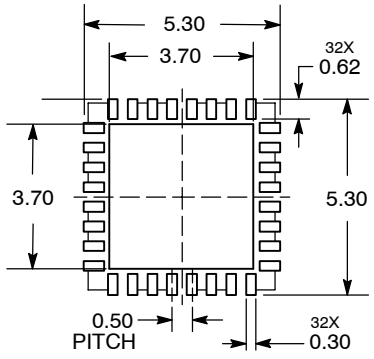
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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