

NCP81236P

Three-Rail Controller with SVID Interface for IMVP8 CPU Applications

The NCP81236P contains a two-phase, and two single-phase buck regulators optimized for Intel IMVP8 compatible CPUs.

The two-phase controller combines true differential voltage sensing, differential inductor DCR current sensing, input voltage feed-forward, and adaptive voltage positioning to provide accurately regulated power for IMVP8 VCCVCGI rails.

Each of the two single-phase controllers can be used for VNN depending on the part configuration. Both make use of ON Semiconductor's patented enhanced RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous frequency scaling operation and continuous mode full power operation. The single-phase rails have an ultralow offset current monitor amplifier with programmable offset compensation for ultra high accuracy current monitoring.

The NCP81236P offers three internal MOSFET drivers with a single external PWM signal.

Two-Phase Rail Features

- Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Digital Soft Start Ramp
- Dynamic Reference Injection® (Patent #US7057381)
- Accurate Total Summing Current Amplifier(Patent #US6683441)
- Dual High Impedance Differential Voltage and Total Current Sense Amplifiers
- Phase-to-Phase Dynamic Current Balancing
- True Differential Current Balancing Sense Amplifiers for Each Phase
- Adaptive Voltage Positioning (AVP)
- Switching Frequency Range of 300 kHz – 750 kHz
- Vin range 4.5 V to 25 V
- Start-Up into Pre-Charged Loads While Avoiding False OVP
- UltraSonic Operation

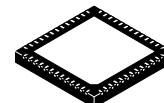
Single-Phase Rail Features

- Enhanced RPM Control System
- Ultra Low Offset IOU Monitor
- Dynamic VID Feed-Forward
- Programmable Droop Gain
- Zero Droop Capable
- Thermal Monitor
- UltraSonic Operation
- Adjustable Vboot
- Digitally Controlled Operating Frequency



ON Semiconductor®

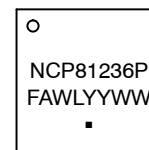
www.onsemi.com



1 52

QFN52
MN SUFFIX
CASE 485BE

MARKING DIAGRAM



NCP81236P = Specific Device Code
F = Wafer Fab
A = Assembly Site
WL = Lot ID
YY = Year
WW = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81236PMNTXG	QFN52 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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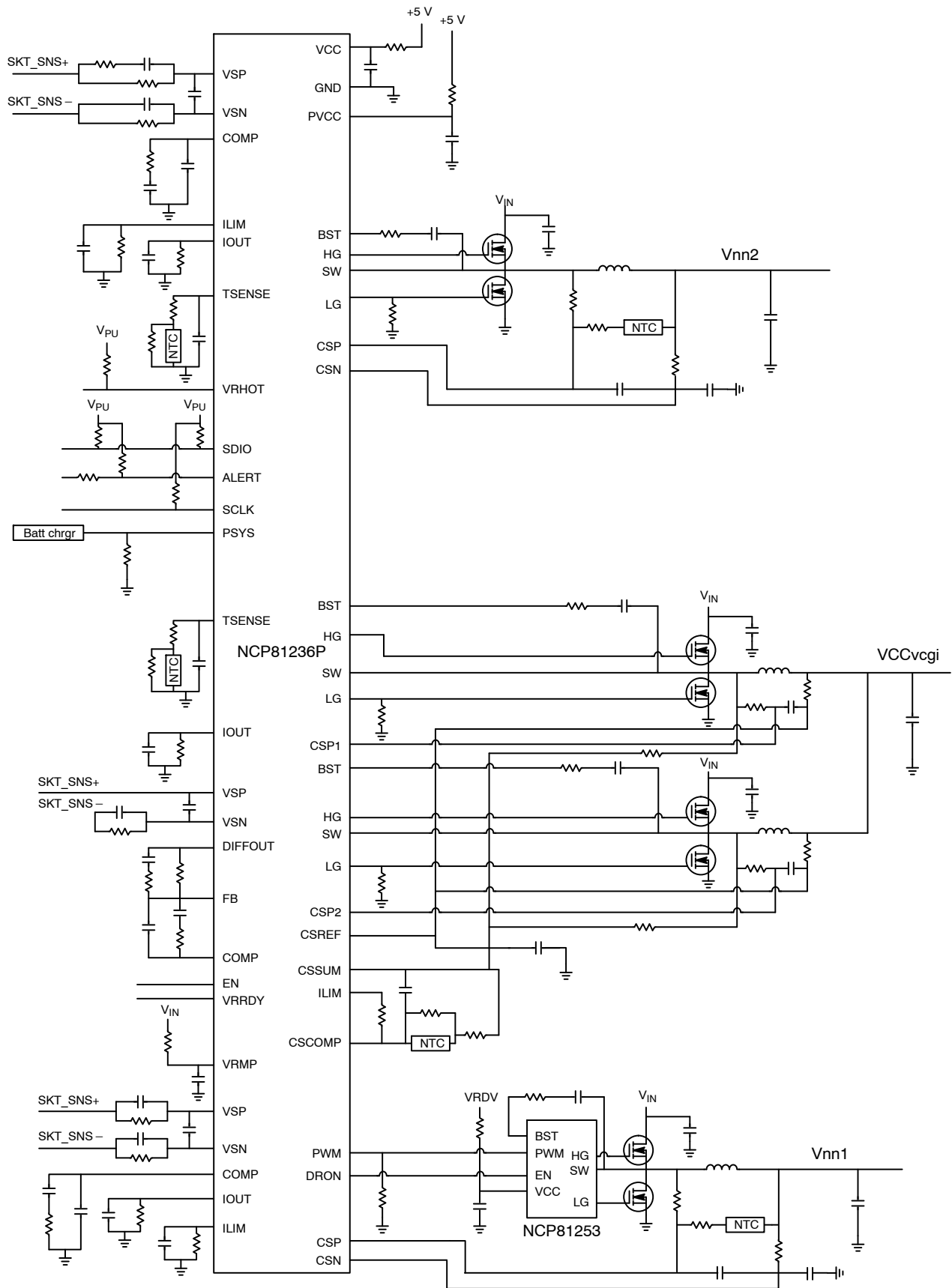


Figure 1. Application Schematic

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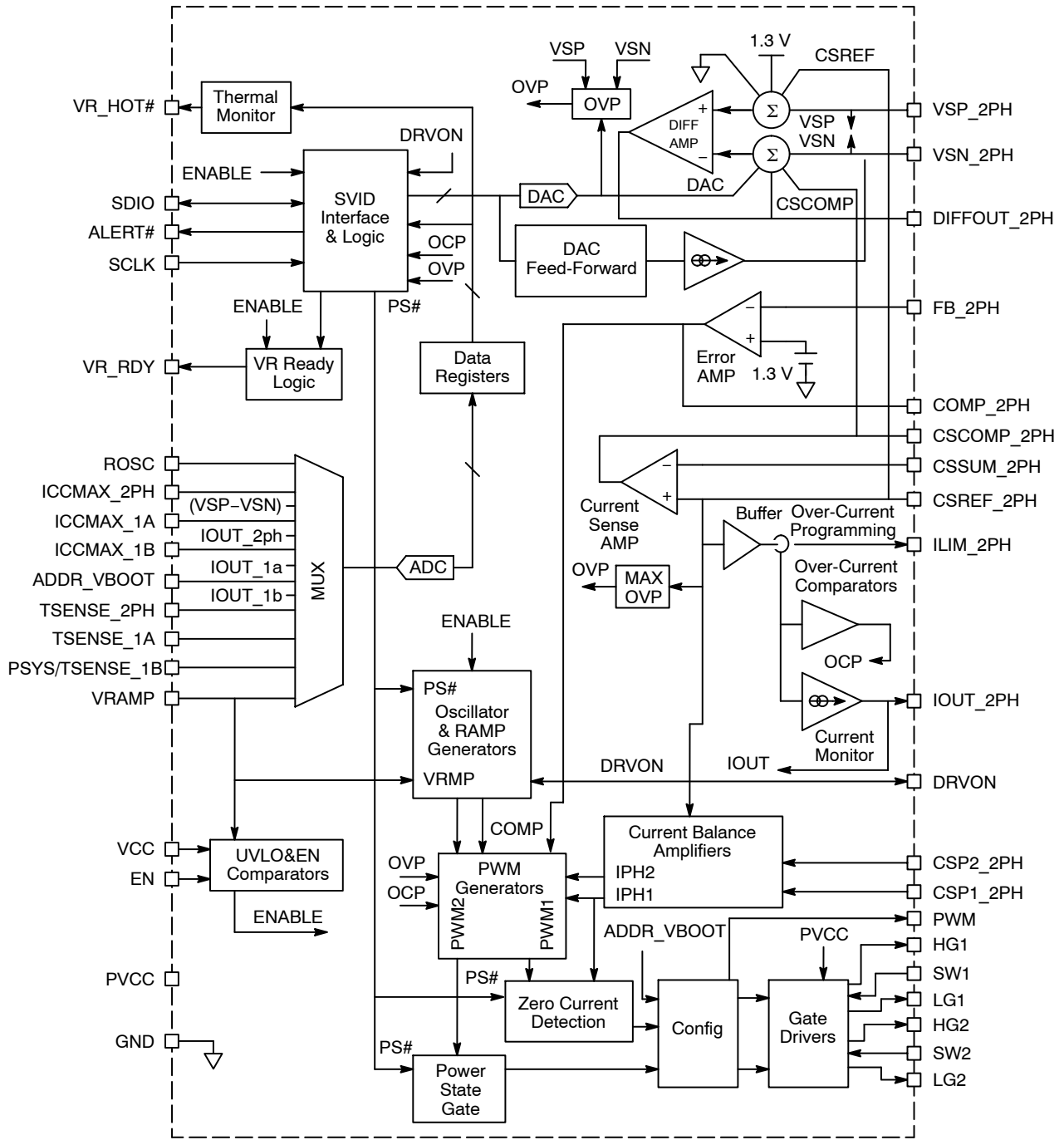


Figure 2. 2-Phase Rail Block Diagram

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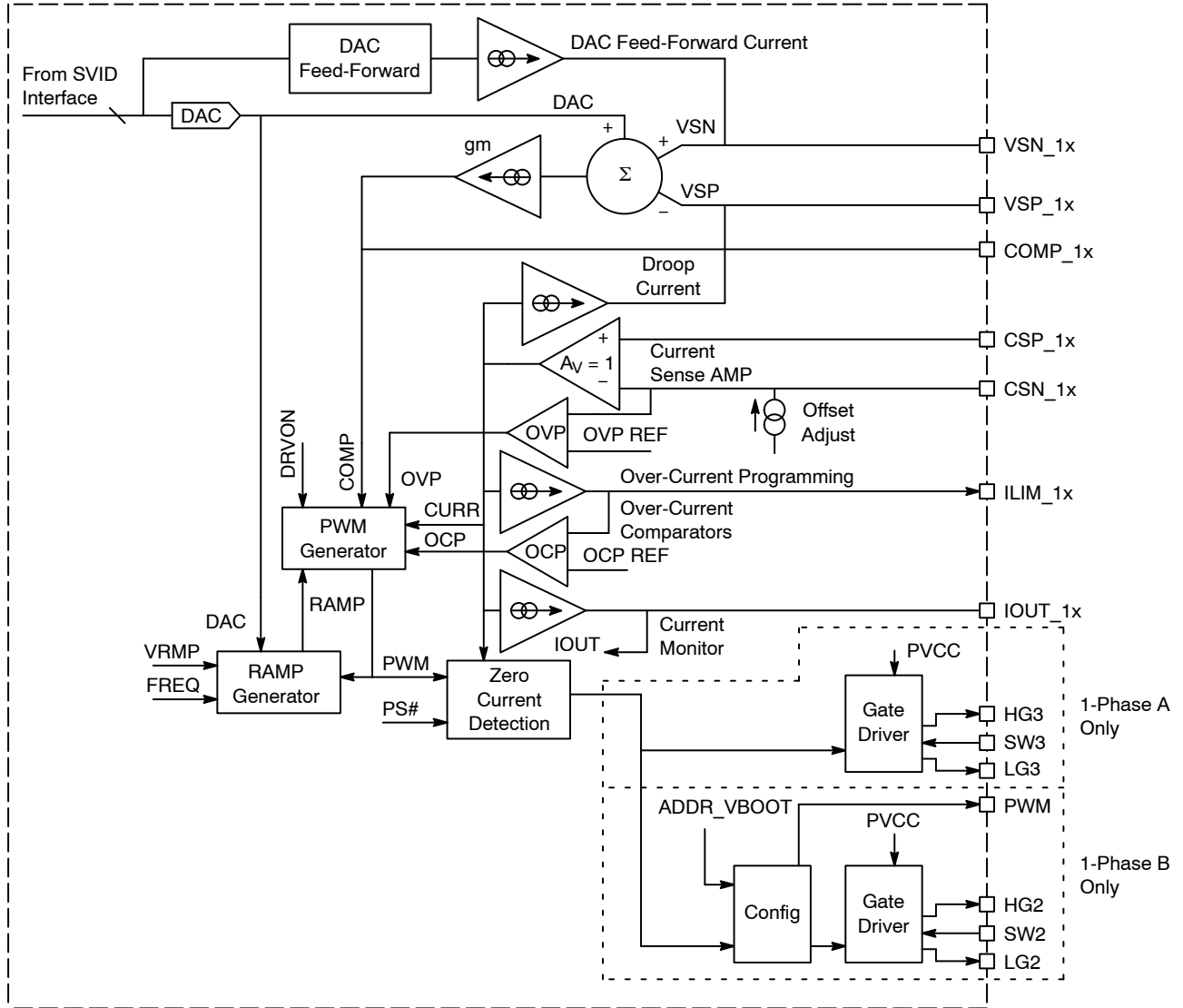


Figure 3. Single-Phase Block Diagram

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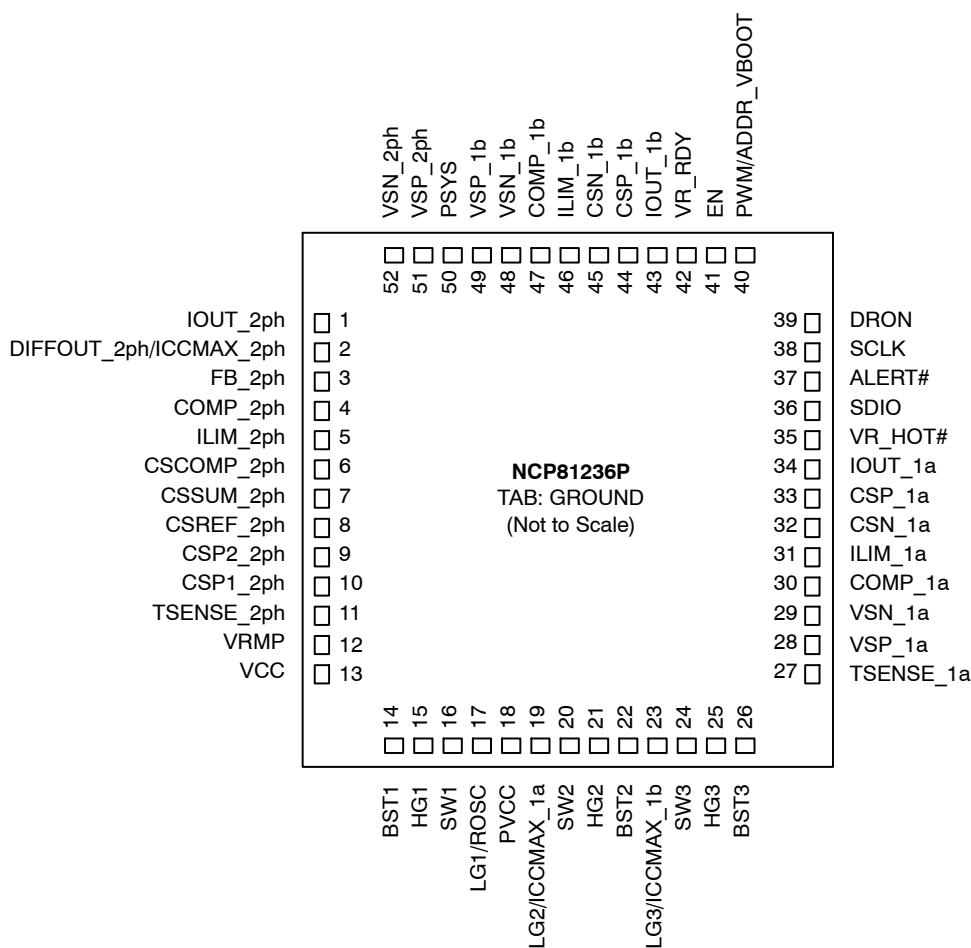


Figure 4. Pin Configuration

Table 1. NCP81236P PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	IOUT_2ph	A resistor to ground programs IOUT gain for the two-phase regulator.
2	DIFFOUT_2ph/ ICCMAX_2ph	Output of the two-phase regulator's differential remote sense amplifier. During start-up, the two-phase regulator's ICCMAX is programmed with a pull-down on this pin.
3	FB_2ph	Error amplifier voltage feedback for two-phase regulator.
4	COMP_2ph	Output of the error amplifier and the non-inverting inputs of the PWM comparators for two-phase regulator.
5	ILIM_2ph	Over-current threshold setting – programmed with a resistor to CSCOMP_2ph for two-phase regulator.
6	CSCOMP_2ph	Output of total-current-sense amplifier for two-phase regulator.
7	CSSUM_2ph	Inverting input of total-current-sense amplifier for two-phase regulator.
8	CSREF_2ph	Total-current-sense amplifier reference voltage input for two-phase regulator.
9	CSP2_2ph	Non-inverting input to current-balance amplifier for Phase 2 of the two-phase regulator.
10	CSP1_2ph	Non-inverting input to current-balance amplifier for Phase 1 of the two-phase regulator.
11	TSENSE_2ph	Temperature sense input for the two-phase regulator.
12	VRMP	Feed-forward input of Vin for the ramp-slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes.
13	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground.
14	BST1	High-side bootstrap supply for Phase 1 of the two-phase regulator.
15	HG1	High-side FET gate driver output for Phase 1 of the two-phase regulator.

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Table 1. NCP81236P PIN DESCRIPTIONS (continued)

Pin No.	Symbol	Description
16	SW1	Current return for high-side FET gate driver for Phase 1 of the two-phase regulator.
17	LG1/ROSC	Low-side FET gate driver output for Phase 1 of the two-phase regulator. During start-up ROSC is programmed with a pull-down resistor on this line.
18	PVCC	Power supply for all three internal FET gate drivers.
19	LG2/ICCMAX_1a	Low-side FET gate driver output for Phase 2 of the two-phase regulator, or output of single-phase regulator 1b. During start-up, regulator 1a's ICCMAX is programmed with a pull-down on this pin.
20	SW2	Current return for high-side FET gate driver for Phase 2 of the two-phase regulator, or for single-phase regulator 1b.
21	HG2	High-side FET gate driver output for Phase 2 of the two-phase regulator, or for single-phase regulator 1b.
22	BST2	High-side bootstrap supply for Phase 2 of the two-phase regulator, or for single-phase regulator 1b.
23	LG3/ICCMAX_1b	Low-side FET gate driver output for single-phase regulator 1a. During start-up, regulator 1b's ICCMAX is programmed with a pull-down on this pin.
24	SW3	Current return for high-side FET gate driver for single-phase regulator 1a.
25	HG3	High-side FET gate driver output for single-phase regulator 1a.
26	BST3	High-side bootstrap supply for single-phase regulator 1a.
27	TSENSE_1a	Temperature sense input for the single-phase regulators.
28	VSP_1a	Differential Output Voltage Sense Positive for single-phase regulator 1a.
29	VSN_1a	Differential Output Voltage Sense Negative for single-phase regulator 1a.
30	COMP_1a	Compensation for single-phase regulator 1a.
31	ILIM_1a	A resistor to ground programs the current-limit for single-phase regulator 1a.
32	CSN_1a	Differential current sense negative for single-phase regulator 1a.
33	CSP_1a	Differential current sense positive for single-phase regulator 1a.
34	IOUT_1a	A resistor to ground programs IOUT gain for single-phase regulator 1a.
35	VR_HOT#	Thermal logic output for over temperature.
36	SDIO	Serial VID data interface
37	ALERT#	Serial VID ALERT#
38	SCLK	Serial VID clock
39	DRON	Bi-directional FET driver enable
40	PWM/ ADDR_VBOOT	PWM output for phase 2 of the two-phase regulator or single-phase regulator 1b. During start-up, a resistor to ground programs SVID address and VBOOT options for all three rails.
41	EN	Enable. High enables all three rails.
42	VR_RDY	VR_RDY indicates all three rails are ready to accept SVID commands.
43	IOUT_1b	A resistor to ground programs IOUT gain for single-phase regulator 1b.
44	CSP_1b	Differential current sense positive for single-phase regulator 1b.
45	CSN_1b	Differential current sense negative for single-phase regulator 1b.
46	ILIM_1b	A resistor to ground programs the current-limit for single-phase regulator 1b.
47	COMP_1b	Compensation for single-phase regulator 1b.
48	VSN_1b	Differential Output Voltage Sense Negative for single-phase regulator 1b.
49	VSP_1b	Differential Output Voltage Sense Positive for single-phase regulator 1b.
50	PSYS/TSENSE_1b	System power signal input. Resistor to ground for scaling / Temperature sense input for the single-phase regulators.
51	VSP_2ph	Differential Output Voltage Sense Positive for the two-phase regulator.
52	VSN-2ph	Differential Output Voltage Sense Negative for the two-phase regulator.

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Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	V _{MAX}	V _{MIN}	I _{SOURCE}	I _{SINK}
COMP_2ph	VCC + 0.3 V	-0.3 V	2 mA	2 mA
CSCOMP_2ph	VCC + 0.3 V	-0.3 V	2 mA	2 mA
VSN_2ph	GND + 0.3 V	GND - 0.3 V	1 mA	1 mA
DIFFOUT_2ph / IccMax_2ph	VCC + 0.3 V	-0.3 V	2 mA	2 mA
VCC	6.5 V	-0.3 V	100 mA	100 mA
PVCC	6.5 V	-0.3 V	100 mA	100 mA
VRMP	25 V	-0.3 V	100 mA	100 mA
SW_x	35 V 40 V ≤ 50 ns	-5 V	100 mA	100 mA
BST_x	35 V wrt / GND 40 V ≤ 50 ns wrt / GND 6.5 V wrt / SW 7.7 V ≤ 50 ns wrt / SW	-0.3 V wrt / SW	100 mA	100 mA
LG_x / ICCMAX_x	VCC + 0.3 V	-0.3 V -2 V ≤ 200 ns	100 mA	100 mA
HG_x	BST + 0.3 V	-0.3 V wrt / SW -2 V ≤ 200 ns wrt /SW	100 mA	100 mA
All Other Pins	VCC + 0.3 V	-0.3 V	100 mA	100 mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*All signals referenced to GND unless noted otherwise.

Table 3. THERMAL INFORMATION

Description	Symbol	Value	Unit
Thermal Characteristic QFN Package (Note 1)	R _{θJA}	68	°C/W
Operating Junction Temperature Range (Note 2)	T _J	-10 to 125	°C
Operating Ambient Temperature Range		-10 to 100	°C
Maximum Storage Temperature Range	T _{STG}	- 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

*The maximum package power dissipation must be observed.

1. JESD 51-5 (1S2P Direct-Attach Method) with 0 LFM
2. JESD 51-7 (1S2P Direct-Attach Method) with 0 LFM

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Table 4. ELECTRICAL CHARACTERISTICS – GENERAL

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit	
BIAS SUPPLY						
VCC Voltage Range		4.75	–	5.25	V	
VCC Quiescent Current	EN = High	PS0, PS1, PS2	–	26	–	mA
		PS3	–	23	–	mA
		PS4	–	145	–	μA
	EN = Low	–	20	–	μA	
VCC UVLO	VCC Rising	–	–	4.5	V	
	VCC Falling	4	–	–	V	
PVCC Voltage Range		4.75	–	5.25	V	
PVCC Quiescent Current	EN = Low (Shutdown)	–	–	1	μA	
	EN = High, No Switching	–	–	1.3	mA	
VRAMP Voltage Range		5	–	20	V	
VRAMP UVLO	VRAMP Rising	–	–	4.25	V	
	VRAMP Falling	3	–	–	V	
ENABLE INPUT						
Upper Threshold		0.8	–	–	V	
Lower Threshold		–	–	0.3	V	
Enable Delay Time		–	–	2.5	ms	
Enable High Input Leakage Current		–	–	0.5	μA	
PHASE DETECTION						
CSP Pin Threshold Voltage		–	–	4.5	V	
Phase Detect Timer		–	1.75	–	ms	
IMVP8 DAC						
System Voltage Accuracy	$0.75\text{ V} \leq \text{DAC} \leq 1.52\text{ V}$	–0.5	–	0.5	%	
	$0.5\text{ V} \leq \text{DAC} \leq 0.745\text{ V}$	–8	–	8	mV	
	$0.25\text{ V} \leq \text{DAC} \leq 0.495\text{ V}$	–10	–	10	mV	
DAC SLEW RATE						
Soft Start Slew Rate		–	15	–	$\text{mV}/\mu\text{s}$	
Slew Rate Slow		–	15	–	$\text{mV}/\mu\text{s}$	
Slew Rate Fast		–	30	–	$\text{mV}/\mu\text{s}$	
DRVON						
Output High Voltage		3	–	–	V	
Output Low Voltage		–	–	0.1	V	
Rise Time	C_L (PCB) = 20 pF $\Delta V_o = 10\%$ to 90%	–	100	–	ns	
Fall Time		–	2.5	–	ns	
Internal Pull-Down Resistance	EN = Low	–	69.5	–	k Ω	
T_{SENSE}						
Bias Current	-10°C to 100°C	115	120	125	μA	
Alert# Assert Threshold		–	485	–	mV	
Alert# De-Assert Threshold		–	513	–	mV	
VR_Hot Assert Threshold		–	466	–	mV	
VR_Hot De-Assert Threshold		–	490	–	mV	

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Table 4. ELECTRICAL CHARACTERISTICS – GENERAL (continued)

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_Rdy OUTPUT					
Output Low Saturation Voltage	IVR_RDY = -4 mA	-	-	0.3	V
Output Leakage Current When High	VR_RDY = 5 V	-1	-	1	μA
Rise Time	1 k Ω Pull-Up to 3.3 V C _{TOT} = 45 pF	-	110	-	ns
Fall Time					
VR_Rdy Delay Rising	EN rising to VR_RDY rising	-	-	2.5	ms
VR_Rdy Delay Falling	Due to OVP	-	0.3	-	μs
	Due to OCP	-	50	-	μs
	EN falling to VR_RDY falling (TD+TE)	-	-	1.5	μs
VR_Hot#					
Output Low Saturation Voltage	IVR_HOT = -4 mA	-	-	0.3	V
Output Leakage Current When High	VR_HOT = 5 V	-1	-	1	μA
ADC					
Linear Input Voltage Range		0	-	2	V
Differential Non-Linearity (DNL)	8-Bits	-	-	1	LSB
Total Unadjusted Error (TUE)		-1	-	1	%
Conversion Time		-	10	-	μs
Conversion Rate		-	33	-	kHz
Power Supply Sensitivity		-	± 1	-	%
Round Robin		-	90	-	μs
IccMax					
Bias Current		9.7	10	10.3	μA
Full scale input voltage		-	2.0	-	V
SCLK, SDIO					
VIL		-	-	0.45	V
VIH		0.65	-	-	V
VOH		-	1.05	-	V
Output Leakage Current When High		-0.5	-	0.5	μA
Pin Capacitance	@ 25°C Only	-	9	-	pF
Clock to Data Delay (Tco) (Note 3)		-	-	12	ns
Setup Time (Tsu) (Note 3)		7	-	-	ns
Hold Time (Thld) (Note 3)		14	-	-	ns
Alert#					
VOL		-	-	0.3	V
VOH		-	1.05	-	V
Output Leakage Current When High		-1	-	1	μA
Pin Capacitance	@ 25°C Only	-	9	-	pF
OVP and UVP					
Absolute Over Voltage Threshold	During Soft Start	-	2.0	-	V
Over Voltage Threshold Above DAC	VSP-VSN-VID Rising	360	400	440	mV
Over Voltage Delay	VSP-VSN Rising to PWM Low	-	25	-	ns
Under Voltage Threshold Below DAC	VSP-VSN-VID Falling	-	300	-	mV
Under Voltage Delay		-	5	-	μs

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Table 4. ELECTRICAL CHARACTERISTICS – GENERAL (continued)

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR					
Switching Frequency Range		300	–	750	kHz
Switching Frequency Accuracy		–	± 10	–	%
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	$V_{CC} - 0.2$	–	–	V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	V
Rise Time	C_L (PCB) = 50 pF	$\Delta V_o = 10\% \text{ to } 90\%$	–	5	ns
Fall Time		$\Delta V_o = 90\% \text{ to } 10\%$	–	5	ns
HIGH-SIDE MOSFET DRIVER					
Pull-Up Resistance, Sourcing Current	BST = PVCC	–	1.4	2.5	Ω
Pull-Down Resistance, Sinking Current	BST = PVCC	–	0.9	2	Ω
HG Rise Time	PVCC = 5 V, $C_L = 3\text{ nF}$, BST-SW = 5 V	6	12	27	ns
HG Fall Time	PVCC = 5 V, $C_L = 3\text{ nF}$, BST-SW = 5 V	6	11	15	ns
HG Turn ON Propagation Delay t _{pdhDRVH}	$C_L = 3\text{ nF}$	9	13	17	ns
SW Pull-Down Resistance	SW to GND	–	2	–	k Ω
HG Pull-Down Resistance	HG to SW, BST – SW = 0 V	–	292	–	k Ω
LOW-SIDE MOSFET DRIVER					
Pull-Up Resistance, Sourcing Current		–	1.6	3.5	Ω
Pull-Down Resistance, Sinking Current		–	0.5	1.5	Ω
LGx Rise Time	3 nF Load	6	18	27	ns
LGx Fall Time	3 nF Load	6	12	25	ns
LGx Turn-On Propagation Delay t _{pdhDRVL}	$C_{LOAD} = 3\text{ nF}$	–	14	20	ns
BOOST RECTIFIER					
RON	EN = Low or EN = High and DRVL = HIGH	5	13	22	Ω
Psys					
Input Current	$R_{SYS} = 20\text{ k}\Omega$	–	–	100	μA
ADC Resolution	8-Bit	–	0.39	–	$\mu\text{A}/\text{LSB}$
		–	7.81	–	mV/L SB
Register Update Rate		–	500	–	μs
Disable Threshold	$V_{CC} = 5\text{ V}$	–	–	4.5	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Based on design or characterisation data, not in production test.

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Table 5. ELECTRICAL CHARACTERISTICS – 2-PHASE RAIL SPECIFIC

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
DIFFERENTIAL SUMMING AMP					
Input Bias Current	VSP = VSN = 1.3 V	-25	-	25	nA
VSP Input Voltage Range		-0.3	-	3	V
VSN Input Voltage Range		-0.3	-	0.3	V
-3dB Bandwidth	$C_L = 20\ \text{pF}$, $R_L = 10\ \text{k}\Omega$	-	22.5	-	MHz
Closed Loop DC Gain	VSP - VSN = 0.5 V to 1.3 V	-	1	-	V/V
ERROR AMPLIFIER					
Input Bias Current	@1.3 V	-400	-	400	nA
Open Loop DC Gain	$C_L = 20\ \text{pF}$, $R_L = 10\ \text{k}\Omega$	-	80	-	dB
Open Loop Unity Gain Bandwidth	$C_L = 20\ \text{pF}$, $R_L = 10\ \text{k}\Omega$	-	20	-	MHz
Slew Rate	$\Delta V_{IN} = 100\ \text{mV}$, $G = -10\ \text{V/V}$ $\Delta V_{OUT} = 1.5\ \text{V}$ to $2.5\ \text{V}$, $C_L = 20\ \text{pF}$, $R_L = 10\ \text{k}\Omega$	-	5	-	V/ μs
Maximum Output Voltage	$I_{SOURCE} = 2.0\ \text{mA}$	4	-	-	V
Minimum Output Voltage	$I_{SINK} = 2.0\ \text{mA}$	-	-	0.9	V
CURRENT SUMMING AMPLIFIER					
Input Bias Current	CSSUM = CSREF = 1.0 V	-8	-	8	μA
Offset Voltage (Vos) (Note 4)		-2.5	-	2.5	mV
Open Loop Gain		-	80	-	dB
Open Loop Unity Gain Bandwidth	$C_L = 20\ \text{pF}$, $R_L = 10\ \text{k}\Omega$	-	10	-	MHz
Maximum Output Voltage	$I_{SOURCE} = 2.0\ \text{mA}$	3.5	-	-	V
Minimum Output Voltage	$I_{SINK} = 0.5\ \text{mA}$	-	-	0.1	V
CURRENT BALANCE AMPLIFIERS					
Input Bias Current	CSP1/2 = CSREF = 1.2 V	-50	-	50	nA
Common Mode Input Voltage Range	CSP1/2 = CSREF	0	-	2.3	V
Differential Mode Input Voltage Range	CSREF = 1.2 V	-100	-	100	mV
Input Offset Voltage Matching	CSP1/2 = CSREF = 1.2 V Measured from Average.	-1.5	-	1.5	mV
Current Sense Amplifier Gain	$0\ \text{V} < \text{CSP1/2} - \text{CSREF} < 0.1\ \text{V}$	5.7	6	6.3	V/V
Multiphase Current Sense Gain Matching	CSP1/2 = CSREF = 10 mV to 30 mV	-3	-	3	%
-3dB Bandwidth		-	6	-	MHz
OVER-CURRENT PROTECTION					
I_{LIM} Threshold Current (Delayed OCP Shutdown)	PS0	9	10	11	μA
	PS1, PS2, PS3	-	6.67	-	μA
I_{LIM} Threshold Current (Immediate OCP Shutdown)	PS0	13.5	15	16.5	μA
	PS1, PS2, PS3	-	10	-	μA
Shutdown Delay	Immediate	-	300	-	ns
Shutdown Delay	Delayed	-	50	-	μs
I_{LIM} Output Voltage Offset	I_{LIM} sourcing 15 μA	-1.5	-	1.5	mV

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Table 5. ELECTRICAL CHARACTERISTICS – 2-PHASE RAIL SPECIFIC (continued)

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OUT} OUTPUT					
Output Offset Current	$V_{ILIM} = 5\text{ V}$	–	–	0.25	μA
Output Source Current	I_{LIM} Source Current = $20\ \mu\text{A}$	–	200	–	μA
Current Gain	I_{IOUT} / I_{ILIM} , $R_{ILIM} = 20\ \text{k}\Omega$, $R_{IOUT} = 5\ \text{k}\Omega$ DAC = 0.8 V , 1.25 V , 1.52 V	9.5	10	10.5	A/A

MODULATORS

0% Duty Cycle	Comp Voltage for PWM Held Low	–	1.3	–	V
100% Duty Cycle	Comp Voltage for PWM Held High $VRAMP = 12\text{ V}$	–	2.6	–	V
PWM Ramp Duty Cycle Matching	Comp = 2 V , PWM T_{ON} Matching	–	± 3	–	%
PWM Phase Angle Error		–	± 15	–	$^{\circ}$
Ramp Feed Forward Voltage Range		5	–	20	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Based on design or characterisation data, not in production test.

Table 6. ELECTRICAL CHARACTERISTICS – SINGLE PHASE RAIL SPECIFIC

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current		–25	–	25	nA
VSP Input Voltage Range		–0.3	–	3	V
VSN Input Voltage Range		–0.3	–	0.3	V
gm		1.3	1.6	1.9	mS
Output Offset		–15	–	15	μA
Open Loop Gain	$Z_L = (1\ \text{nF} + 1\ \text{k}\Omega) \parallel 10\ \text{pF}$	–	73	–	dB
Source Current	$\Delta V_{IN} = -200\ \text{mV}$	–	200	–	μA
Sink Current	$\Delta V_{IN} = 200\ \text{mV}$	–	200	–	μA
–3dB Bandwidth	$Z_L = (1\ \text{nF} + 1\ \text{k}\Omega) \parallel 10\ \text{pF}$	–	20	–	MHz

CURRENT SENSE AMPLIFIER

Input Bias Current	$CSP = CSN = 1.2\text{ V}$	–50	–	50	nA
Common Mode Input Voltage Range	$CSP = CSN$	0	–	2.3	V
Common Mode Rejection	$CSP = CSN = 0.5\text{ V to }1.2\text{ V}$	60	80	–	dB
Differential Mode Input Voltage Range	$CSN = 1.2\text{ V}$	–100	–	100	mV
Gain I_{OUT} Output	$0\text{ V} \leq CSP - CSN \leq 0.1\text{ V}$	0.96	1	1.04	mS
Gain VSP and I_{LIM} Outputs	$0\text{ V} \leq CSP - CSN \leq 0.1\text{ V}$	0.96	1	1.04	mS
–3dB Bandwidth		–	6	–	MHz

OVER-CURRENT PROTECTION

Output Offset Current	$V_{ILIM} = 1.3\text{ V}$	–1.5	–	1.5	μA
Maximum Output Current	$0\text{ V} \leq V_{ILIM} \leq 1.3\text{ V}$	–	130	–	μA
Maximum Output Voltage	$I_{LIM} = 100\ \mu\text{A}$	1.4	–	–	V
Activation Threshold Voltage		1.287	1.3	1.313	V
Activation Delay		–	250	–	ns

I_{OUT}

Output Offset Current	$0\text{ V} \leq V_{IOUT} \leq 2.0\text{ V}$	–250	–	250	nA
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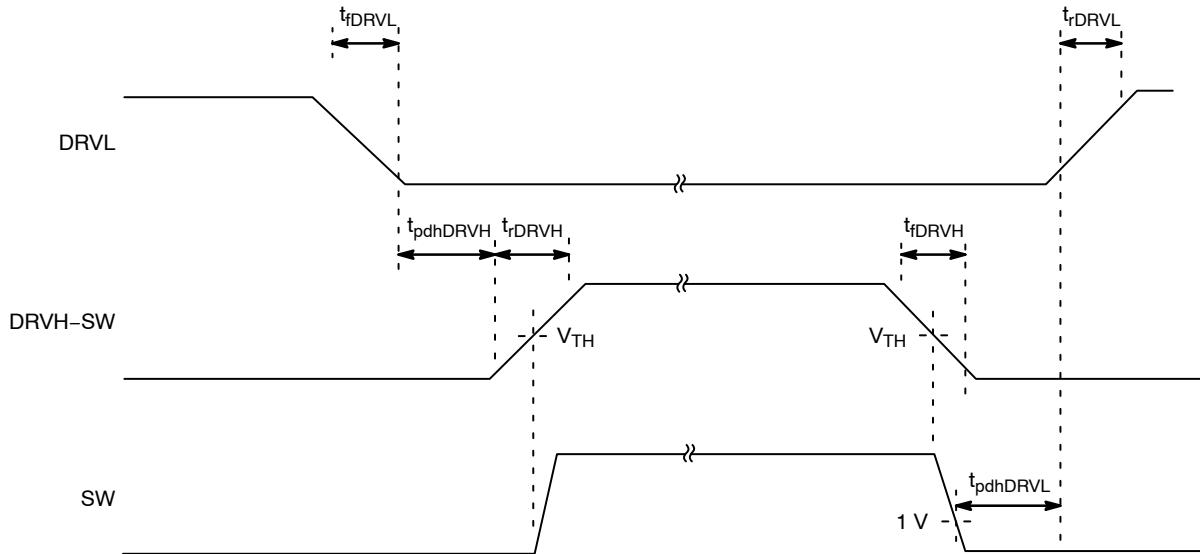
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Table 6. ELECTRICAL CHARACTERISTICS – SINGLE PHASE RAIL SPECIFIC (continued)

(Unless otherwise stated: $-10^{\circ}\text{C} < T_A < 100^{\circ}\text{C}$; $4.75\text{ V} < V_{CC} < 5.25\text{ V}$; $C_{VCC} = 0.1\ \mu\text{F}$)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OUT}					
Maximum Output Current	$0\text{ V} \leq V_{IOUT} \leq 2.0\text{ V}$	–	130	–	μA
Maximum Output Voltage	$I_{IOUT} = 100\ \mu\text{A}$	2.1	–	–	V
DROOP					
Output Offset Current	$0\text{ V} \leq V_{DROOP} \leq 1.8\text{ V}$	–900	–	900	nA
Maximum Output Current	$0\text{ V} \leq V_{DROOP} \leq 1.8\text{ V}$	–	130	–	μA
Maximum Output Voltage	$I_{DROOP} = 100\ \mu\text{A}$	1.8	–	–	V
ZCD COMPARATOR					
Offset Accuracy	Referred to CSP – CSN	–	± 1.5	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



NOTE: Timing is referenced to the 10% and the 90% points, unless otherwise stated.

Figure 5. Driver Timing Diagram

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Table 7. IMVP8 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	0	0	0	0	0	0	0	Off	00
0	0	0	0	0	0	0	1	0.25	01
0	0	0	0	0	0	1	0	0.255	02
0	0	0	0	0	0	1	1	0.26	03
0	0	0	0	0	1	0	0	0.265	04
0	0	0	0	0	1	0	1	0.27	05
0	0	0	0	0	1	1	0	0.275	06
0	0	0	0	0	1	1	1	0.28	07
0	0	0	0	1	0	0	0	0.285	08
0	0	0	0	1	0	0	1	0.29	09
0	0	0	0	1	0	1	0	0.295	0A
0	0	0	0	1	0	1	1	0.3	0B
0	0	0	0	1	1	0	0	0.305	0C
0	0	0	0	1	1	0	1	0.31	0D
0	0	0	0	1	1	1	0	0.315	0E
0	0	0	0	1	1	1	1	0.32	0F
0	0	0	1	0	0	0	0	0.325	10
0	0	0	1	0	0	0	1	0.33	11
0	0	0	1	0	0	1	0	0.335	12
0	0	0	1	0	0	1	1	0.34	13
0	0	0	1	0	1	0	0	0.345	14
0	0	0	1	0	1	0	1	0.35	15
0	0	0	1	0	1	1	0	0.355	16
0	0	0	1	0	1	1	1	0.36	17
0	0	0	1	1	0	0	0	0.365	18
0	0	0	1	1	0	0	1	0.37	19
0	0	0	1	1	0	1	0	0.375	1A
0	0	0	1	1	0	1	1	0.38	1B
0	0	0	1	1	1	0	0	0.385	1C
0	0	0	1	1	1	0	1	0.39	1D
0	0	0	1	1	1	1	0	0.395	1E
0	0	0	1	1	1	1	1	0.4	1F
0	0	1	0	0	0	0	0	0.405	20
0	0	1	0	0	0	0	1	0.41	21
0	0	1	0	0	0	1	0	0.415	22
0	0	1	0	0	0	1	1	0.42	23
0	0	1	0	0	1	0	0	0.425	24
0	0	1	0	0	1	0	1	0.43	25
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	1	0.44	27
0	0	1	0	1	0	0	0	0.445	28
0	0	1	0	1	0	0	1	0.45	29
0	0	1	0	1	0	1	0	0.455	2A
0	0	1	0	1	0	1	1	0.46	2B
0	0	1	0	1	1	0	0	0.465	2C
0	0	1	0	1	1	0	1	0.47	2D
0	0	1	0	1	1	1	0	0.475	2E
0	0	1	0	1	1	1	1	0.48	2F
0	0	1	1	0	0	0	0	0.485	30
0	0	1	1	0	0	0	1	0.49	31
0	0	1	1	0	0	1	0	0.495	32
0	0	1	1	0	0	1	1	0.5	33

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Table 7. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	0	1	1	0	1	0	0	0.505	34
0	0	1	1	0	1	0	1	0.51	35
0	0	1	1	0	1	1	0	0.515	36
0	0	1	1	0	1	1	1	0.52	37
0	0	1	1	1	0	0	0	0.525	38
0	0	1	1	1	0	0	1	0.53	39
0	0	1	1	1	0	1	0	0.535	3A
0	0	1	1	1	0	1	1	0.54	3B
0	0	1	1	1	1	0	0	0.545	3C
0	0	1	1	1	1	0	1	0.55	3D
0	0	1	1	1	1	1	0	0.555	3E
0	0	1	1	1	1	1	1	0.56	3F
0	1	0	0	0	0	0	0	0.565	40
0	1	0	0	0	0	0	1	0.57	41
0	1	0	0	0	0	1	0	0.575	42
0	1	0	0	0	0	1	1	0.58	43
0	1	0	0	0	1	0	0	0.585	44
0	1	0	0	0	1	0	1	0.59	45
0	1	0	0	0	1	1	0	0.595	46
0	1	0	0	0	1	1	1	0.6	47
0	1	0	0	1	0	0	0	0.605	48
0	1	0	0	1	0	0	1	0.61	49
0	1	0	0	1	0	1	0	0.615	4A
0	1	0	0	1	0	1	1	0.62	4B
0	1	0	0	1	1	0	0	0.625	4C
0	1	0	0	1	1	0	1	0.63	4D
0	1	0	0	1	1	1	0	0.635	4E
0	1	0	0	1	1	1	1	0.64	4F
0	1	0	1	0	0	0	0	0.645	50
0	1	0	1	0	0	0	1	0.65	51
0	1	0	1	0	0	1	0	0.655	52
0	1	0	1	0	0	1	1	0.66	53
0	1	0	1	0	1	0	0	0.665	54
0	1	0	1	0	1	0	1	0.67	55
0	1	0	1	0	1	1	0	0.675	56
0	1	0	1	0	1	1	1	0.68	57
0	1	0	1	1	0	0	0	0.685	58
0	1	0	1	1	0	0	1	0.69	59
0	1	0	1	1	0	1	0	0.695	5A
0	1	0	1	1	0	1	1	0.7	5B
0	1	0	1	1	1	0	0	0.705	5C
0	1	0	1	1	1	0	1	0.71	5D
0	1	0	1	1	1	1	0	0.715	5E
0	1	0	1	1	1	1	1	0.72	5F
0	1	1	0	0	0	0	0	0.725	60
0	1	1	0	0	0	0	1	0.73	61
0	1	1	0	0	0	1	0	0.735	62
0	1	1	0	0	0	1	1	0.74	63
0	1	1	0	0	1	0	0	0.745	64
0	1	1	0	0	1	0	1	0.75	65
0	1	1	0	0	1	1	0	0.755	66
0	1	1	0	0	1	1	1	0.76	67

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Table 7. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
0	1	1	0	1	0	0	0	0.765	68
0	1	1	0	1	0	0	1	0.77	69
0	1	1	0	1	0	1	0	0.775	6A
0	1	1	0	1	0	1	1	0.78	6B
0	1	1	0	1	1	0	0	0.785	6C
0	1	1	0	1	1	0	1	0.79	6D
0	1	1	0	1	1	1	0	0.795	6E
0	1	1	0	1	1	1	1	0.8	6F
0	1	1	1	0	0	0	0	0.805	70
0	1	1	1	0	0	0	1	0.81	71
0	1	1	1	0	0	1	0	0.815	72
0	1	1	1	0	0	1	1	0.82	73
0	1	1	1	0	1	0	0	0.825	74
0	1	1	1	0	1	0	1	0.83	75
0	1	1	1	0	1	1	0	0.835	76
0	1	1	1	0	1	1	1	0.84	77
0	1	1	1	1	0	0	0	0.845	78
0	1	1	1	1	0	0	1	0.85	79
0	1	1	1	1	0	1	0	0.855	7A
0	1	1	1	1	0	1	1	0.86	7B
0	1	1	1	1	1	0	0	0.865	7C
0	1	1	1	1	1	0	1	0.87	7D
0	1	1	1	1	1	1	0	0.875	7E
0	1	1	1	1	1	1	1	0.88	7F
1	0	0	0	0	0	0	0	0.885	80
1	0	0	0	0	0	0	1	0.89	81
1	0	0	0	0	0	1	0	0.895	82
1	0	0	0	0	0	1	1	0.9	83
1	0	0	0	0	1	0	0	0.905	84
1	0	0	0	0	1	0	1	0.91	85
1	0	0	0	0	1	1	0	0.915	86
1	0	0	0	0	1	1	1	0.92	87
1	0	0	0	1	0	0	0	0.925	88
1	0	0	0	1	0	0	1	0.93	89
1	0	0	0	1	0	1	0	0.935	8A
1	0	0	0	1	0	1	1	0.94	8B
1	0	0	0	1	1	0	0	0.945	8C
1	0	0	0	1	1	0	1	0.95	8D
1	0	0	0	1	1	1	0	0.955	8E
1	0	0	0	1	1	1	1	0.96	8F
1	0	0	1	0	0	0	0	0.965	90
1	0	0	1	0	0	0	1	0.97	91
1	0	0	1	0	0	1	0	0.975	92
1	0	0	1	0	0	1	1	0.98	93
1	0	0	1	0	1	0	0	0.985	94
1	0	0	1	0	1	0	1	0.99	95
1	0	0	1	0	1	1	0	0.995	96
1	0	0	1	0	1	1	1	1	97
1	0	0	1	1	0	0	0	1.005	98
1	0	0	1	1	0	0	1	1.01	99
1	0	0	1	1	0	1	0	1.015	9A
1	0	0	1	1	0	1	1	1.02	9B

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Table 7. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
1	0	0	1	1	1	0	0	1.025	9C
1	0	0	1	1	1	0	1	1.03	9D
1	0	0	1	1	1	1	0	1.035	9E
1	0	0	1	1	1	1	1	1.04	9F
1	0	1	0	0	0	0	0	1.045	A0
1	0	1	0	0	0	0	1	1.05	A1
1	0	1	0	0	0	1	0	1.055	A2
1	0	1	0	0	0	1	1	1.06	A3
1	0	1	0	0	1	0	0	1.065	A4
1	0	1	0	0	1	0	1	1.07	A5
1	0	1	0	0	1	1	0	1.075	A6
1	0	1	0	0	1	1	1	1.08	A7
1	0	1	0	1	0	0	0	1.085	A8
1	0	1	0	1	0	0	1	1.09	A9
1	0	1	0	1	0	1	0	1.095	AA
1	0	1	0	1	0	1	1	1.1	AB
1	0	1	0	1	1	0	0	1.105	AC
1	0	1	0	1	1	0	1	1.11	AD
1	0	1	0	1	1	1	0	1.115	AE
1	0	1	0	1	1	1	1	1.12	AF
1	0	1	1	0	0	0	0	1.125	B0
1	0	1	1	0	0	0	1	1.13	B1
1	0	1	1	0	0	1	0	1.135	B2
1	0	1	1	0	0	1	1	1.14	B3
1	0	1	1	0	1	0	0	1.145	B4
1	0	1	1	0	1	0	1	1.15	B5
1	0	1	1	0	1	1	0	1.155	B6
1	0	1	1	0	1	1	1	1.16	B7
1	0	1	1	1	0	0	0	1.165	B8
1	0	1	1	1	0	0	1	1.17	B9
1	0	1	1	1	0	1	0	1.175	BA
1	0	1	1	1	0	1	1	1.18	BB
1	0	1	1	1	1	0	0	1.185	BC
1	0	1	1	1	1	0	1	1.19	BD
1	0	1	1	1	1	1	0	1.195	BE
1	0	1	1	1	1	1	1	1.2	BF
1	1	0	0	0	0	0	0	1.205	C0
1	1	0	0	0	0	0	1	1.21	C1
1	1	0	0	0	0	1	0	1.215	C2
1	1	0	0	0	0	1	1	1.22	C3
1	1	0	0	0	1	0	0	1.225	C4
1	1	0	0	0	1	0	1	1.23	C5
1	1	0	0	0	1	1	0	1.235	C6
1	1	0	0	0	1	1	1	1.24	C7
1	1	0	0	1	0	0	0	1.245	C8
1	1	0	0	1	0	0	1	1.25	C9
1	1	0	0	1	0	1	0	1.255	CA
1	1	0	0	1	0	1	1	1.26	CB
1	1	0	0	1	1	0	0	1.265	CC
1	1	0	0	1	1	0	1	1.27	CD
1	1	0	0	1	1	1	0	1.275	CE
1	1	0	0	1	1	1	1	1.28	CF

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Table 7. IMVP8 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	Hex
1	1	0	1	0	0	0	0	1.285	D0
1	1	0	1	0	0	0	1	1.29	D1
1	1	0	1	0	0	1	0	1.295	D2
1	1	0	1	0	0	1	1	1.3	D3
1	1	0	1	0	1	0	0	1.305	D4
1	1	0	1	0	1	0	1	1.31	D5
1	1	0	1	0	1	1	0	1.315	D6
1	1	0	1	0	1	1	1	1.32	D7
1	1	0	1	1	0	0	0	1.325	D8
1	1	0	1	1	0	0	1	1.33	D9
1	1	0	1	1	0	1	0	1.335	DA
1	1	0	1	1	0	1	1	1.34	DB
1	1	0	1	1	1	0	0	1.345	DC
1	1	0	1	1	1	0	1	1.35	DD
1	1	0	1	1	1	1	0	1.355	DE
1	1	0	1	1	1	1	1	1.36	DF
1	1	1	0	0	0	0	0	1.365	E0
1	1	1	0	0	0	0	1	1.37	E1
1	1	1	0	0	0	1	0	1.375	E2
1	1	1	0	0	0	1	1	1.38	E3
1	1	1	0	0	1	0	0	1.385	E4
1	1	1	0	0	1	0	1	1.39	E5
1	1	1	0	0	1	1	0	1.395	E6
1	1	1	0	0	1	1	1	1.4	E7
1	1	1	0	1	0	0	0	1.405	E8
1	1	1	0	1	0	0	1	1.41	E9
1	1	1	0	1	0	1	0	1.415	EA
1	1	1	0	1	0	1	1	1.42	EB
1	1	1	0	1	1	0	0	1.425	EC
1	1	1	0	1	1	0	1	1.43	ED
1	1	1	0	1	1	1	0	1.435	EE
1	1	1	0	1	1	1	1	1.44	EF
1	1	1	1	0	0	0	0	1.445	F0
1	1	1	1	0	0	0	1	1.45	F1
1	1	1	1	0	0	1	0	1.455	F2
1	1	1	1	0	0	1	1	1.46	F3
1	1	1	1	0	1	0	0	1.465	F4
1	1	1	1	0	1	0	1	1.47	F5
1	1	1	1	0	1	1	0	1.475	F6
1	1	1	1	0	1	1	1	1.48	F7
1	1	1	1	1	0	0	0	1.485	F8
1	1	1	1	1	0	0	1	1.49	F9
1	1	1	1	1	0	1	0	1.495	FA
1	1	1	1	1	0	1	1	1.5	FB
1	1	1	1	1	1	0	0	1.505	FC
1	1	1	1	1	1	0	1	1.51	FD
1	1	1	1	1	1	1	0	1.515	FE
1	1	1	1	1	1	1	1	1.52	FF

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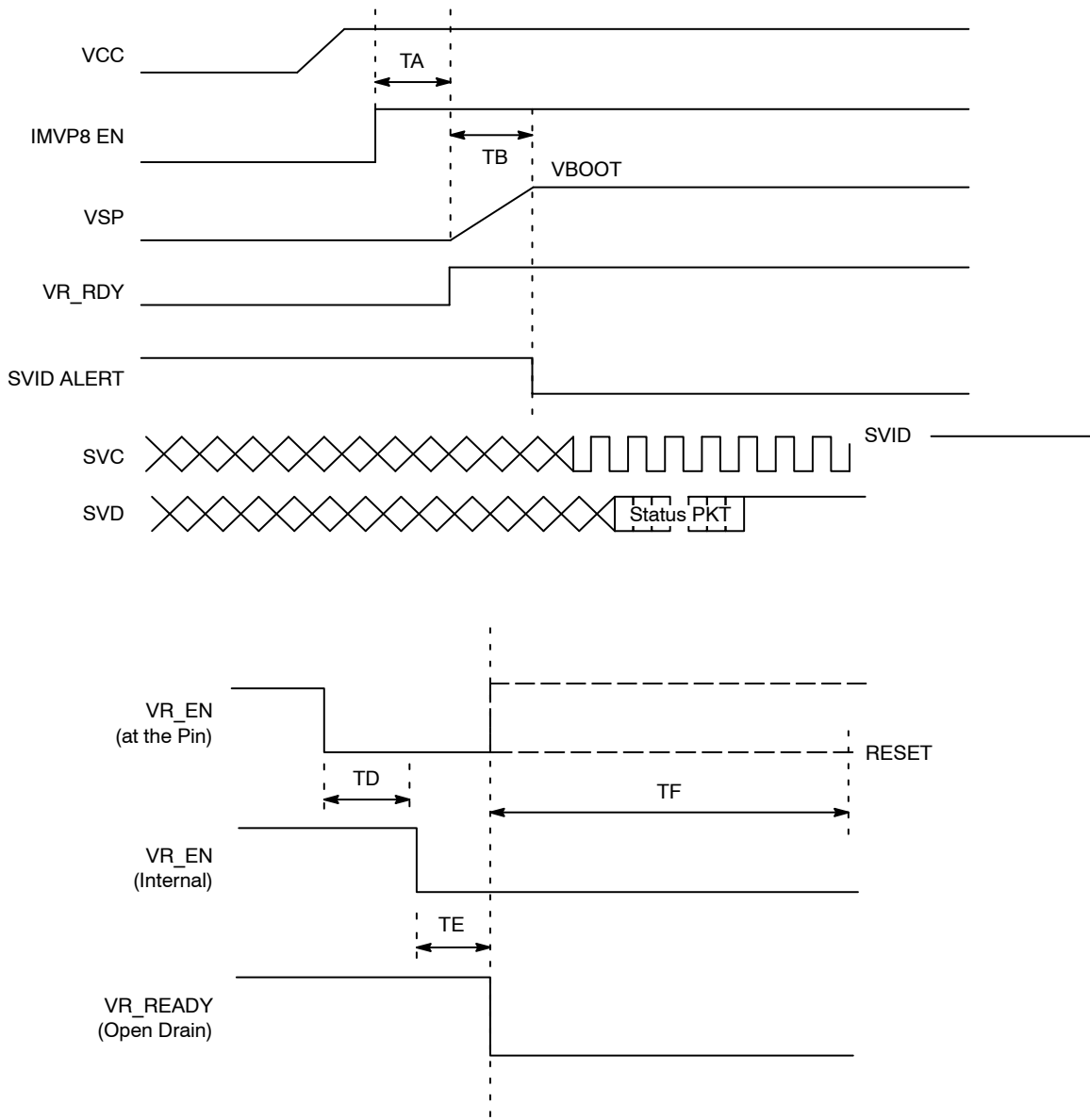


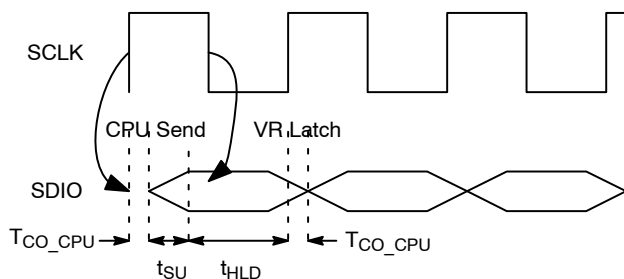
Figure 6. Start-Up Timing

Table 8. START-UP TIMING

	Minimum	Typical	Maximum
TA	-	-	2.5 ms
TB	-	-	VID/Slow
TD	0 μ s	-	1 μ s
TE	-	-	500 ns

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CPU Driving, Single Data Rate

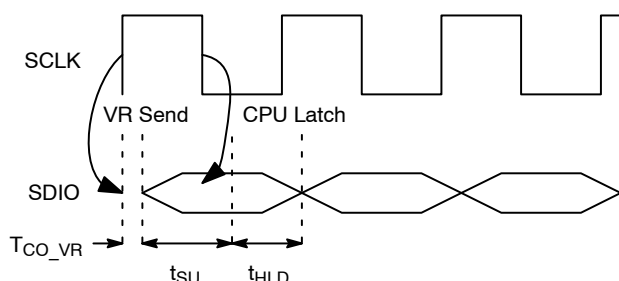


$$T_{CO_CPU} = \text{Clock to Data Delay in CPU}$$

$$t_{SU} = 0.5 \cdot T - T_{CO_CPU}$$

$$t_{HLD} = 0.5 \cdot T + T_{CO_CPU}$$

VR Driving, Single Data Rate



$$T_{CO_VR} = \text{Clock to Data Delay in VR}$$

$$t_{SU} = T - 2 \cdot T_{FLY} - T_{CO_VR}$$

$$t_{HLD} = 2 \cdot T_{FLY} + T_{CO_VR}$$

$$T_{FLY} = \text{Propagation Time on Serial VID Bus}$$

Figure 7. SVID Timing Diagram

Table 9. STATE TRUTH TABLE

State	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	DRON Pin	Method of Reset
POR 0 < VCC < UVLO	N/A	N/A	N/A	Resistive Pull Down	
Disabled EN < Threshold UVLO > Threshold	Low	Low	Disabled	Low	
Start-Up Delay & Calibration EN > Threshold UVLO > Threshold	Low	Low	Disabled	Low	
DRON Fault EN > Threshold UVLO > Threshold DRON < Threshold	Low	Low	Disabled	Resistive Pull Up	Driver Must Release DRON to High
Soft Start EN > Threshold UVLO > Threshold DRON > High	High	Operational	Active/No Latch	High	
Normal Operation EN > Threshold UVLO > Threshold DRON > High	High	Operational	Active/Latching	High	N/A
Over Voltage	Low	N/A	DAC+OVP	High	
Over Current	Low	Operational	Last DAC Code	Low	
VID Code = 00h	Low: if Reg34h: bit 0 = 0; High: if Reg34h: bit 0 = 1;	Clamped at 0.9 V	Disabled	High, PWM Outputs in Low State	

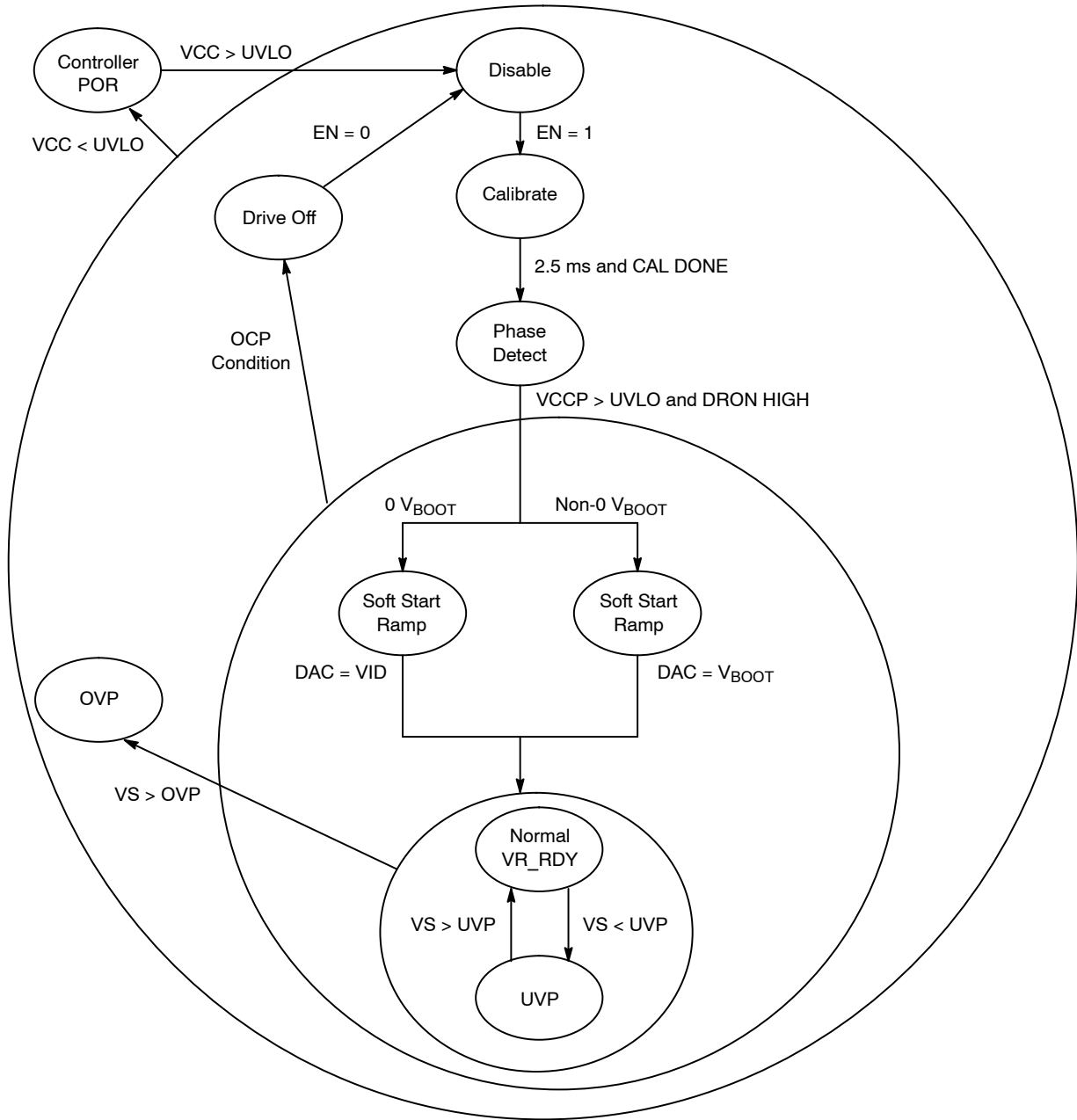


Figure 8. State Diagram

NCP81236P

GENERAL

Configuration

The NCP81236P is a three-rail IMVP8 controller, with three internal drivers, intended to provide VCCVCGI (Address 00h) and VNN (Address 02h). The NCP81236P is configured with the two-phase, dualedge controller providing VCCVCGI.

Table 10 shows the available configurations, and the pull-down resistor required on Pin 40 (PWM/ ADDR_VBOOT) to configure them.

Table 10. CONFIGURATIONS

R (kΩ)	2ph		Ph1	Ph2		T _{SENSE}	1ph A				1ph B				
	Addr	V _{BOOT} (V)	D _{RV1}	D _{RV2}	PWM		Addr	V _{BOOT} (V)	D _{RV3}	T _{SENSE}	Addr	V _{BOOT} (V)	D _{RV2}	PWM	T _{SENSE}
10	0	0	x		x	2ph	1	0	x	1a	2	1	x		N/A (P _{sys})
16.2	0	1.2	x		x	2ph	1	1.2	x	1a	2	1	x		N/A (P _{sys})
22.1	0	0	x		x	2ph	1	0	x	1a	2	1.05	x		N/A (P _{sys})
28.7	0	0	x		x	2ph	1	0	x	1a	2	0.95	x		N/A (P _{sys})
35.7	0	0	x	x		2ph	1	0	x	1a	2	1		x	N/A (P _{sys})
43.2	0	1.2	x	x		2ph	1	1.2	x	1a	2	1		x	N/A (P _{sys})
51.1	0	0	x	x		2ph	1	0	x	1a	2	1.05		x	N/A (P _{sys})
61.9	0	0	x	x		2ph	1	0	x	1a	2	0.95		x	N/A (P _{sys})
71.5	0	0	x	x		2ph	2	1	x	N/A (P _{sys})	1	0		x	1a
82.5	0	1.2	x	x		2ph	2	1	x	N/A (P _{sys})	1	1.2		x	1a
95.3	0	0	x	x		2ph	2	1.05	x	N/A (P _{sys})	1	0		x	1a
110	0	0	x	x		2ph	2	0.95	x	N/A (P _{sys})	1	0		x	1a

Switching Frequency F_{sw}

F_{sw} is programmed on start-up with a pull-down on the LG1 pin.

Table 11. SWITCHING FREQUENCY

Resistor	Core/GT	SA
6.81 kΩ	750 kHz	750 kHz
14 kΩ	600 kHz	600 kHz
21.5 kΩ	450 kHz	600 kHz
28.7 kΩ	300 kHz	450 kHz

Serial VID interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the NCP81236P (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the master. The SDIO is bidirectional, used for transferring data from the CPU to the NCP81236P and from the NCP81236P

to the CPU. The ALERT# is an open drain output from the NCP81236P to signal to the master that the Status Register should be read.

Refer to the relevant Intel document for SVID routing and pull-up topologies.

The SVID bus will operate at a max frequency of 43 MHz.

VID code change is supported by SVID interface with three options as below:

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Table 12. VID CODE CHANGE

Option	SVID Command Code	Feature Description	Register Address (Indicating the Slew Rate of VID Code Change)
SetVID_Fast	01h	30 mV/ μ s VID Code Change Slew Rate	24h
SetVID_Slow	02h	=1/2 of SetVID_Fast VID Code Change Slew Rate	25h
SetVID_Decay	03h	No Control, VID Code Down	N/A

Serial VID

The NCP81236P supports the Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#). The table of supported

registers for Domains 00h, 01h, and 02/03h is shown below. The SVID register set for Domain 0Dh is smaller and contains the following registers: 00h, 01h, 02h, 05h, 10h, 11h, and 1Bh.

Table 13. SERIAL VID

Index	Name	Description	Access	IA/GT/SA	PSYS 0Dh
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah.	R	1Ah	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	36h	36h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R		
03h	Product Date Code ID		R		
05h	Protocol ID	Identifies the SVID Protocol the controller supports.	R	05h	05h
06h	Capability	<p>Informs the Master of the controller's Capabilities, 1 = Supported, 0 = Not Supported</p> <p>Bit 7: I_{out} format 0: I_{out} reported as 1A/LSB of Reg 15h 1: I_{out} reported relative to I_{ccMax}, where FFh = I_{ccMax}</p> <p>Bit 6: ADC Measurement of Temp Supported Bit 5: ADC Measurement of Pin Supported Bit 4: ADC Measurement of V_{in} Supported Bit 3: ADC Measurement of I_{in} Supported Bit 2: ADC Measurement of P_{out} Supported Bit 1: ADC Measurement of V_{out} Supported Bit 0: ADC Measurement of I_{out} Supported</p>	R	D1h	N/A
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h	00h
12h	Temp Zone	Data register showing temperature zones the system is operating in.	R	00h	N/A
15h	I _{out}	8 bit binary word ADC of current. This register reads 0xFF when the output current is at I _{cc_Max} .	R		N/A
16h	V _{out}	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8 mV.	R		N/A
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C = 64h. A value of 00h indicates this function is not supported.	R		N/A
18h	P _{out}	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported.	R	01h	N/A
1Ch	Status2_Last Read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h	

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Table 13. SERIAL VID (continued)

Index	Name	Description	Access	IA/GT/SA	PSYS 0Dh
1Bh	Input Power	Required for Input Power Domain Address 0Dh.	R		
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register.	R	00h	N/A
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_hot asserts. This value defaults to 100°C and programmable over the SVID Interface.	R/W	64h	N/A
24h	SR_Fast	Slew Rate for SetVID_fast commands. Binary format in mV/μs.	R	1Eh	N/A
25h	SR_Slow	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/μs. FAST/2 is default for IMVP8	R	02h	N/A
26h	Vboot	Vboot is resistor programmed at startup. The controller will ramp to Vboot and hold at Vboot until it receives a new SetVID command to move to a different voltage.	R	00h	N/A
2Ah	SR_Slow Selector	Fast_SR/2 – Default Fast_SR/4 Fast_SR/8 Fast_SR/16	R/W	01h	N/A
2Bh	PS4 Exit Latency	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp	R	8Ch	N/A
2Ch	PS3 Exit Latency	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h	N/A
2Dh	EN to Ready for SVID Command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh	N/A
2Eh	PWR_IN_MAX	Input power sensor scaling for input power (1Bh) register programmed by platform designer to the rating of the input power sensor. Programming as 2W/LSB	RW	N/A	FFh
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format.	RW	FBh	N/A
31h	VID Setting	Data register containing currently programmed VID voltage. VID data format.	RW	00h	N/A
32h	Pwr State	Register containing the current programmed power state.	RW	00h	N/A
33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 BITS are # VID steps for margin 2's complement. 00h = No Margin 01h = +1 VID Step 02h = +2 VID Steps FFh = -1 VID Step FEh = -2 VID Steps	RW	00h	N/A
34h	MultiVR Config			01h	N/A
42h	IVID1-VID		RW	00h	N/A
43h	IVID1-I	Maximum instantaneous current for single phase operation.	RW		N/A
44h	IVID2-VID		RW	00h	N/A
45h	IVID2-I	Maximum instantaneous current for IVID 2 state.	RW		N/A
46h	IVID3-VID		RW	00h	N/A
47h	IVID3-I	Maximum instantaneous current for DCM/CCM decision threshold.	RW		N/A

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The NCP81236P is optimized to meet Intel’s IMVP8 specifications and implements PS0, PS1, PS2, PS3 and PS4 power-states.

Table 14. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Two-Phase Dual Edge One-Phase CCM RPM (1-Phase A/B Only)
PS1	One-Phase CCM RPM
PS2	One-Phase DCM RPM
PS3	One-Phase DCM RPM
PS4	Standby

Ultra-Sonic Mode

Ultra-Sonic Mode forces a minimum switching frequency above audible range when a rail is in DCM mode.

$$V_{DIFFOUT} = (V_{VSP} - V_{VSN}) + (1.3\text{ V} - V_{DAC}) + (V_{DROOP} - V_{CSREF}) \quad (\text{eq. 1})$$

Two-Phase Rail Voltage Compensation

The remote Sense Amplifier output is applied to a Type III compensation network formed by the error amplifier and external tuning components. The non-inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote sense amplifier output.

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to the same 1.3 V reference used for the differential sense amplifier output bias.

Two-Phase Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator’s output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage to

Two-Phase Rail High Performance Voltage Error Amplifier

A high performance error amplifier is provided for high bandwidth transient performance. A standard type III compensation circuit is normally used to compensate the system.

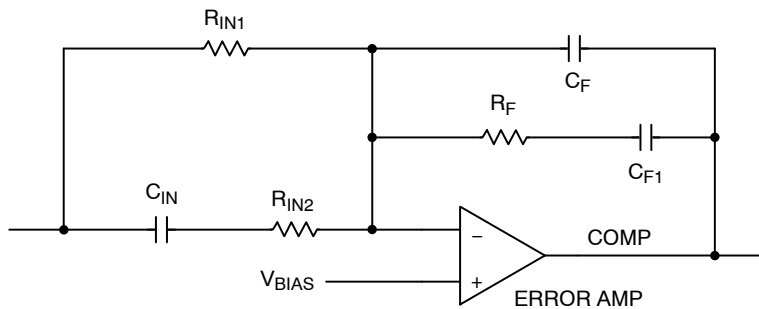


Figure 9. Standard Type III Compensation Circuit

Differential Current Feedback Amplifiers

Each phase of the two-phase rail has a low offset differential amplifier to sense that phase current for current balance and per phase OCP protection during soft-start. The inputs to the CSNx and CSPx pins are high impedance inputs. It is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset issues with leakage current. It is also recommended that the voltage

sense element be no less than 0.5 mΩ for accurate current balance. Fine tuning of this time constant is generally not required. The individual phase current is summed into the PWM comparator feedback this way current is balanced via a current mode control approach.

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \cdot DCR} \tag{eq. 2}$$

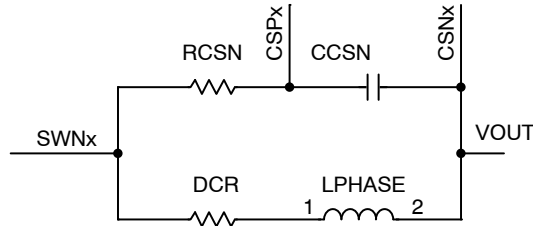


Figure 10.

Two-Phase Rail Total Current Sense Amplifier

The NCP81236P uses a patented approach to sum the phase currents into a single temperature compensated total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The total current signal is floating with respect to CSREF. The current signal is the difference between CSCOMP and CSREF. The Rref(n) resistors sum the signals from the output side of the inductors to create a

low impedance virtual ground. The amplifier actively filters and gains up the voltage applied across the inductors to recover the voltage drop across the inductor series resistance (DCR). Rth is placed near an inductor to sense the temperature of the inductor. This allows the filter time constant and gain to be a function of the Rth NTC resistor and compensate for the change in the DCR with temperature.

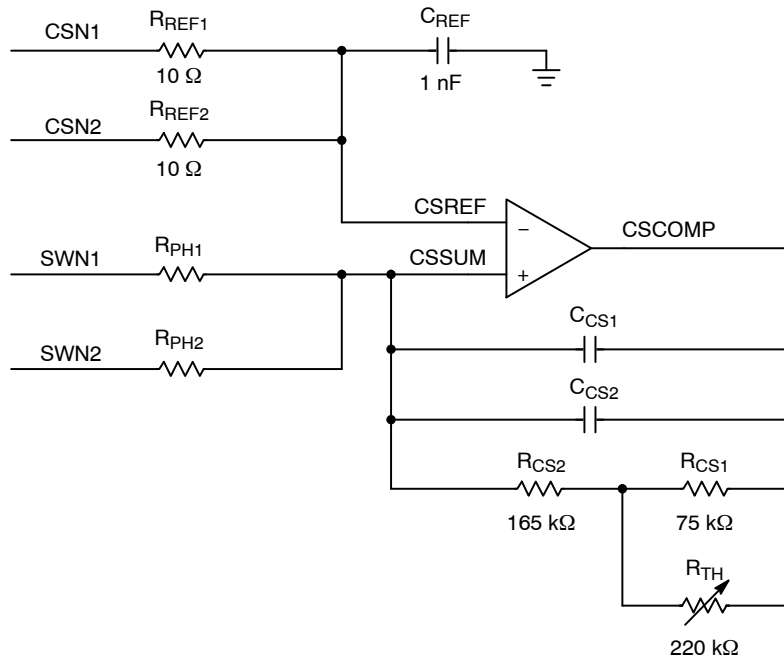


Figure 11.

The DC gain equation for the current sensing:

$$V_{CSCOMP - CSREF} = - \frac{R_{CS2} + \frac{R_{CS1} \cdot R_{TH}}{R_{CS1} + R_{TH}}}{R_{PH}} \cdot (I_{OUT_{Total}} \cdot DCR) \tag{eq. 3}$$

Set the gain by adjusting the value of the R_{PH} resistors. The DC gain should be set to the output voltage droop. If the voltage from CSCOMP to CSREF is less than 100 mV at ICCMAX then it is recommend increasing the gain of the CSCOMP amp. This is required to provide a good current signal to offset voltage ratio for the ILIMIT pin. When no droop is needed, the gain of the amplifier should be set to provide ~100 mV across the current limit programming resistor at full load. The NTC should be placed near the closest inductor. The output voltage droop should be set with the droop filter divider.

The pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor. This allows the circuit to recover the inductor DCR voltage drop current signal. C_{CS1} and C_{CS2} are in parallel to allow for fine tuning of the time constant using commonly available values. It is best to fine tune this filter during transient testing.

$$F_Z = \frac{DCR @ 25^\circ C}{2 \cdot \pi \cdot L_{Phase}} \quad (eq. 4)$$

Two-Phase Rail Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIMIT and CSCOMP pins. The ILIMIT pin mirrors the voltage at the CSREF pin and mirrors the sink current internally to IOUT (reduced by the IOUT Current Gain) and the current limit comparators. The 100% current limit trips if the ILIMIT sink current exceeds 10 μA for 50 μs. The 150% current limit trips with minimal delay if the ILIMIT sink current exceeds 15 μA. Set the value of the current limit resistor based on the CSCOMP-CSREF voltage as shown below.

If the 2-phase rail is configured in 2-phase mode, the ILIMIT sink current thresholds are reduced when the rail transitions to single-phase operation (PS1/2/3). In these lower power states, the trip currents are 2/3 of the thresholds in PS0. This helps to prevent power stage damage should an over current event occur during single-phase operation. If the multi-phase rail is configured in 1-phase mode, the ILIMIT threshold current remain the same (10 μA delayed, 15 μA immediate) regardless of the power state.

$$R_{LIMIT} = \frac{R_{CS2} + \frac{R_{CS1} \cdot R_{TH}}{R_{CS1} + R_{TH}}}{R_{PH}} \cdot \left(I_{OUT_Total} \cdot DCR \right) \quad (eq. 5)$$

or

$$R_{LIMIT} = \frac{V_{CSCOMP-CSREF @ ILIMIT}}{10 \mu} \quad (eq. 6)$$

Two-Phase Rail Programming DAC Feed-Forward Filter

The DAC feed-forward implementation is realized by having a filter on the VSN pin. Programming R_{VSN} sets the

gain of the DAC feed-forward and C_{VSN} provides the time constant to cancel the time constant of the system per the following equations. C_{OUT} is the total output capacitance and R_{OUT} is the output impedance of the system.

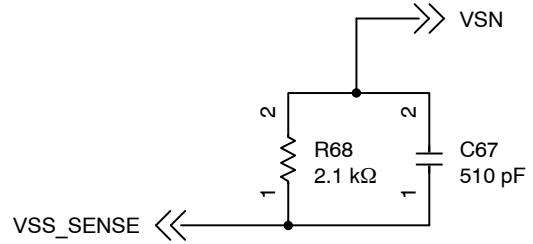


Figure 12.

$$R_{VSN} = C_{OUT} \cdot R_{OUT} \cdot 453.6 \cdot 10^6 \quad (eq. 7)$$

$$C_{VSN} = \frac{R_{OUT} \cdot C_{OUT}}{R_{VSN}} \quad (eq. 8)$$

Two-Phase Rail Programming DROOP

The signals CSCOMP and CSREF are differentially summed with the output voltage feedback to add precision voltage droop to the output voltage.

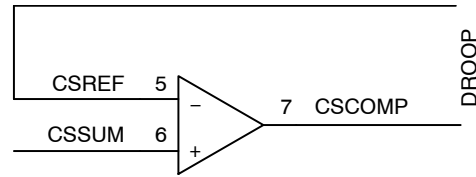


Figure 13.

$$Droop = DCR \cdot \frac{R_{CS}}{R_{PH}} \quad (eq. 9)$$

Two-Phase Rail Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICC_MAX generates a 2 V signal on IOUT. A pull-up resistor from 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2.0 V \cdot R_{LIMIT}}{10 \cdot \frac{R_{CS2} + \frac{R_{CS1} \cdot R_{TH}}{R_{CS1} + R_{TH}}}{R_{PH}} \cdot \left(I_{OUT_ICC_MAX} \cdot DCR \right)} \quad (eq. 10)$$

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Programming ICC_MAX

The SVID interface provides the platform ICC_MAX value at register 21h. A resistor to ground on the IMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set according to the table/equation below. The resistor value should be no less than 2 kΩ.

Design Note: Since ICC_MAX is multi-functioned with LG, it is crucial that the LS FET is not turned on during

ICC_MAX programming. Source current and maximum resistor value must not produce a voltage at the FET gate that will turn it on. Keeping the voltage less than 400 mV should be safe.

IccMax_2ph:

$$R_{IccMax2ph} = \frac{IccMax_{2ph} + 32}{127} \cdot 200 \text{ k}\Omega \quad (\text{eq. 11})$$

IccMax_1ph: See Table 15 below.

Table 15. ICCMAX_1PH

Resistor	01h	Resistor	02h
6.8 kΩ	23	5 kΩ	3
11 kΩ	24	7.8 kΩ	4
14.1 kΩ	25	11 kΩ	5
17.2 kΩ	28	14.1 kΩ	6
22.6 kΩ	29	17.2 kΩ	7
26.5 kΩ	30	20.3 kΩ	8
29.5 kΩ	34	23.4 kΩ	9
32.8 kΩ	35		
36 kΩ	36		

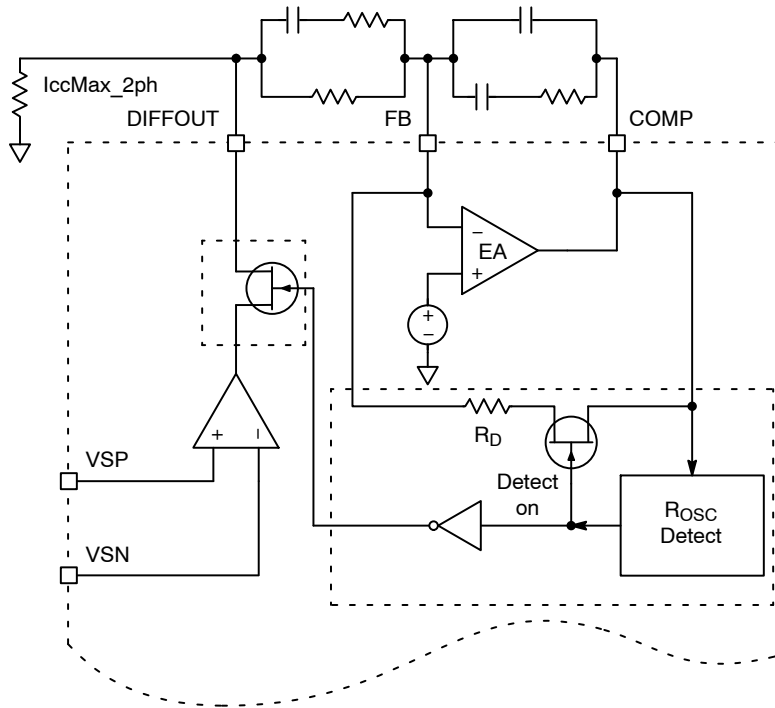


Figure 14.

Programming TSENSE

Temperature sense inputs are provided. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the

internal A/D converter. A 100 k NTC similar to the VISHAY ERT-J1VS104JA should be used. See the specification table for the thermal sensing voltage thresholds and source current.

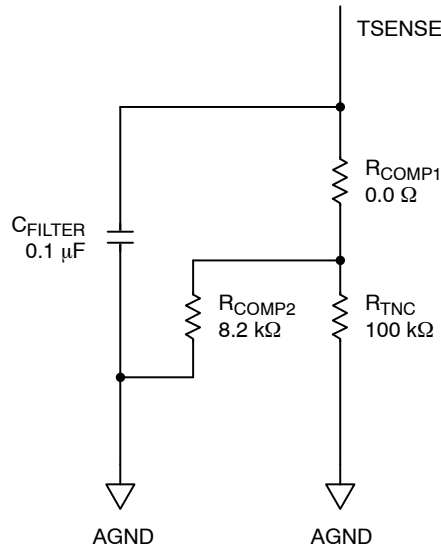


Figure 15.

Precision Oscillator

A programmable precision oscillator is provided. The clock oscillator serves as the master clock to the ramp generator circuit. This oscillator is programmed during start-up by a resistor to ground on the LG1/ROSC pin.

The oscillator generates triangle ramps that are 0.5~2.5 V in amplitude depending on the VRMP pin voltage to provide input voltage feed forward compensation.

feed-forward control by varying the ramp magnitude with respect to the VRMP pin voltage. The VRMP pin also has a UVLO function. The VRMP UVLO is only active after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled.

The PWM ramp is changed according to the following,

$$V_{RAMPpk=pkpp} = 0.1 \cdot V_{VRMP} \quad (\text{eq. 12})$$

Programming the Ramp Feed-Forward Circuit

The ramp generator circuit provides the ramp used by the PWM comparators. The ramp generator provides voltage

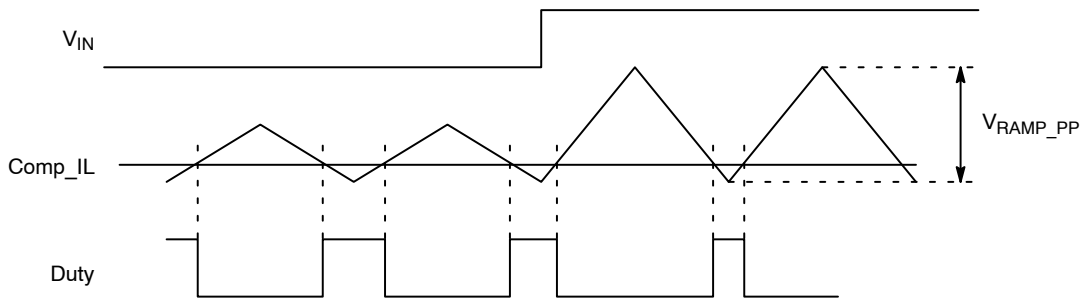


Figure 16.

Two-Phase Rail PWM Comparators

The non-inverting input of the comparator for each phase is connected to the summed output of the error amplifier (COMP) and each phase current ($I_L \cdot DCR \cdot \text{Phase Balance}$

Gain Factor). The inverting input is connected to the oscillator ramp voltage with a 1.3 V offset. The operating input voltage range of the comparators is from 0 V to 3.0 V and the output of the comparator generates the PWM output.

During steady state operation, the duty cycle is centered on the valley of the sawtooth ramp waveform. The steady state duty cycle is still calculated by approximately V_{OUT}/V_{IN} .

Two-Phase Rail Phase Detection Sequence

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry monitoring the CSP outputs. Normally, this rail operates as a two-phase VCC_{VCGI} PWM controller. If CSP2_2ph is pulled high to VCC, the two-phase rail operates as a single-phase rail.

Disable Single-Phase Rail

If the NCP81236P is to provide fewer than three rails, one or both of the single-phase rails can be disabled by pulling up their respective CSP pin. The main rail cannot be disabled.

Single-Phase Rails

The architecture of the two single-phase rails makes use of a digitally enhanced, high performance, current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove

frequency drift under all continuous mode operating conditions. At light load the single-phase rails automatically transition into DCM operation to save power.

Single-Phase Rail Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator’s output voltage sense points through filter networks describe in the Droop Compensation and DAC Feedforward Compensation sections. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm \cdot (V_{DAC} - (V_{VSP} - V_{VSN})) \quad (eq. 13)$$

This current is applied to a standard Type II compensation network.

Single-Phase Rail Voltage Compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF.

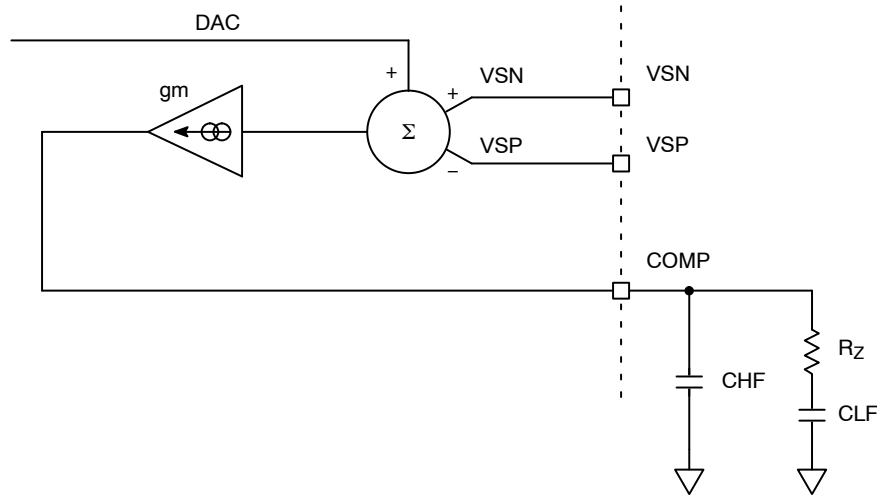


Figure 17.

Single-Phase Rail – Differential Current Feedback Amplifier

Each single-phase controller has a low offset, differential amplifier to sense output inductor current. An external lowpass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The lowpass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_Z = \frac{DCR @ 25^{\circ}C}{2 \cdot \pi \cdot L_{Phase}} \quad (eq. 14)$$

$$F_P = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}} \right) \cdot C_{CSSP}} \quad (eq. 15)$$

Forming the lowpass filter with an NTC thermistor (R_{TH}) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of R_{PHSP} and R_{CSSP} are set

based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the lowpass filter resistance not exceed 10 kΩ in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 mΩ for sufficient current accuracy. Recommended values for the external filter components are:

$$R_{PHSP} = 7.68 \text{ k}\Omega$$

$$R_{CSSP} = 14.3 \text{ k}\Omega$$

$$R_{TH} = 100 \text{ k}\Omega, \text{ Beta} = 4300$$

$$C_{CSSP} = \frac{L_{PHASE}}{\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot DCR} \quad (\text{eq. 16})$$

Using 2 parallel capacitors in the lowpass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT} \cdot DCR \quad (\text{eq. 17})$$

To improve the noise immunity of the current feedback amplifier, it is recommended to use an RC low pass filter (R_F and C_F in Figure 18) on the CSN pin of the amplifier placed as close as possible to the controller. The bandwidth of this filter should be ~5 MHz with $R_F < 20 \Omega$. To mitigate against noise due to excessive ringing that may be present on the inductor side of R_{PHSP} , it is recommended to use a capacitor in parallel with the inductor. The value of the capacitor should be chosen such that:

$$\sqrt{L \times C} < < \frac{1}{2 \times \pi \times \text{Ringing Frequency}} \quad (\text{eq. 18})$$

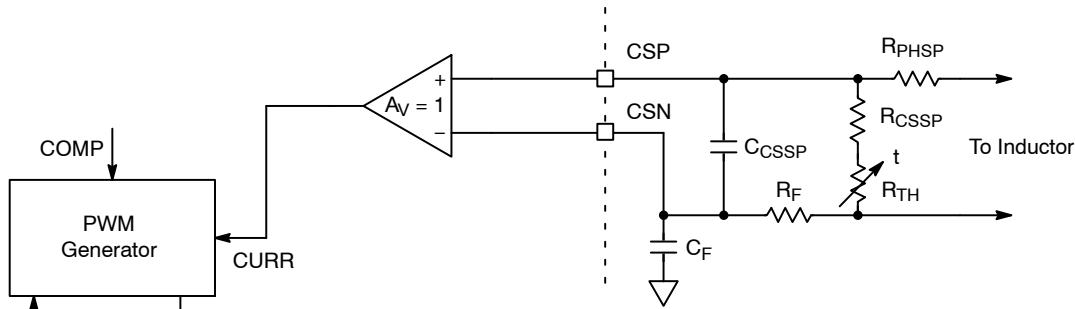


Figure 18.

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

Single-Phase Rail – Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP} proportional to load current. This characteristic can reduce the output capacitance required to

maintain output voltage within limits during load transients faster than those to which the regulation loop can respond. In the NCP81236P, a loadline is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.

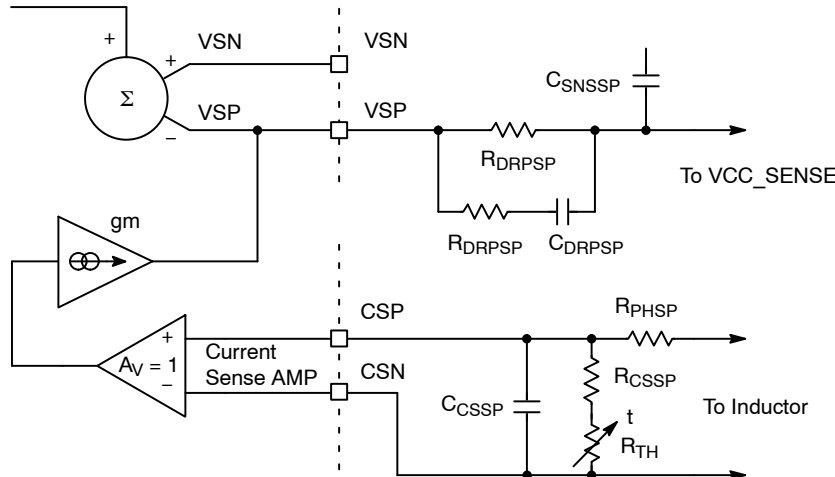


Figure 19.

$$V_{\text{DROOP}} = R_{\text{DRPSP}} \cdot g_m \cdot \frac{R_{\text{TH}} + R_{\text{CSSP}}}{R_{\text{PHSP}} + R_{\text{TH}} + R_{\text{CSSP}}} \cdot I_{\text{OUT}} \cdot \text{DCR} \quad (\text{eq. 19})$$

The loadline is programmed by choosing R_{DRPSP} such that the ratio of voltage produced across R_{DRPSP} to output current is equal to the desired loadline.

$$R_{\text{DRPSP}} = \frac{\text{Loadline}}{g_m \cdot \text{DCR}} \cdot \frac{R_{\text{PHSP}} + R_{\text{TH}} + R_{\text{CSSP}}}{R_{\text{TH}} + R_{\text{CSSP}}} \quad (\text{eq. 20})$$

Single-Phase Rail – Programming the DAC Feed-Forward Filter

The DAC feed-forward implementation for the single-phase rail is the same as for the 2-phase rail. The NCP81236P outputs a pulse of current from the VSN

pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. R_{FFSP} sets the gain of the DAC feed-forward and C_{FFSP} provides the time constant to cancel the time constant of the system per the following equations. C_{OUT} is the total output capacitance of the system.

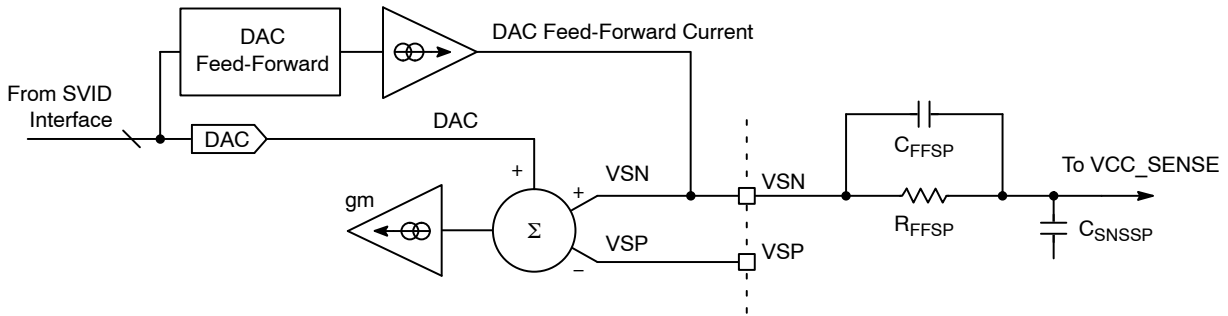


Figure 20.

$$R_{\text{FFSP}} = \frac{\text{Loadline} \cdot C_{\text{OUT}}}{1.35 \cdot 10^{-9}} \quad (\Omega) \quad C_{\text{FFSP}} = \frac{200}{R_{\text{FFSP}}} \quad (\text{nF}) \quad (\text{eq. 21})$$

Single-Phase Rail – Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIMSP}) from the ILIM pin to ground. The current limit latches the single-phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the

current limit resistor based on the equation shown below. A capacitor must be placed in parallel with the programming resistor to avoid false trips due to the effect of the output ripple current.

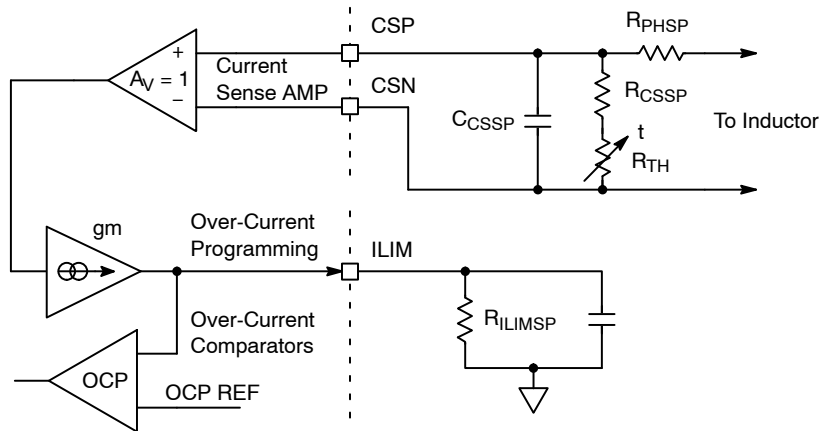


Figure 21.

$$R_{\text{ILIMSP}} = \frac{1.3 \text{ V}}{g_m \cdot \frac{R_{\text{TH}} + R_{\text{CSSP}}}{R_{\text{PHSP}} + R_{\text{TH}} + R_{\text{CSSP}}} \cdot I_{\text{OUT_LIMIT}} \cdot \text{DCR}} \quad (\text{eq. 22})$$

Single-Phase Rail – Programming IOU

The IOU pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOU pin is monitored by the internal A/D converter and should be

scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2 V signal on IOU. A pull-up resistor from 5 V VCC can be used to offset the IOU signal positive if needed.

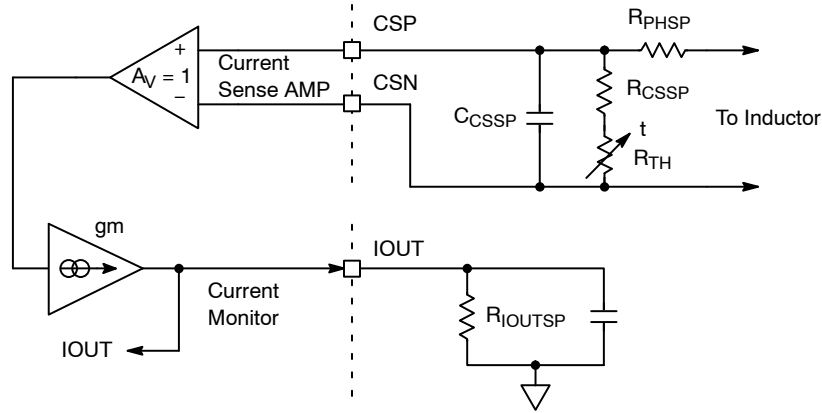


Figure 22.

$$R_{IOUASP} = \frac{2\text{ V}}{gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{ccMax} \cdot DCR} \tag{eq. 23}$$

Single-Phase Rail PWM Comparators

The non-inverting input of each comparator (one for each phase) is connected to the summation of the output of the error amplifier (COMP) and each phase current ($I_L \cdot DCR \cdot \text{Phase Current Gain Factor}$). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output.

A PWM pulse starts when the error amp signal (COMP voltage) rises above the trigger threshold plus gained-up

inductor current, and stops when the artificial ramp plus gained-up inductor current crosses the COMP voltage. Both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the COMP voltage increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

PROTECTION FEATURES

Under Voltage Lockouts

There are several under voltage monitors in the system. Hysteresis is incorporated within the comparators. The NCP81236P monitors the 5 V VCC supply as well as the VRMP pin. The gate drivers monitor both the gate driver VCC and the BST voltage. When the voltage on the gate

driver is insufficient it will pull DRON low and prevents the controller from being enabled. The gate driver will hold DRON low for a minimum period of time to allow the controller to hold off it's start-up sequence. In this case the PWM is set to the MID state to begin soft start.

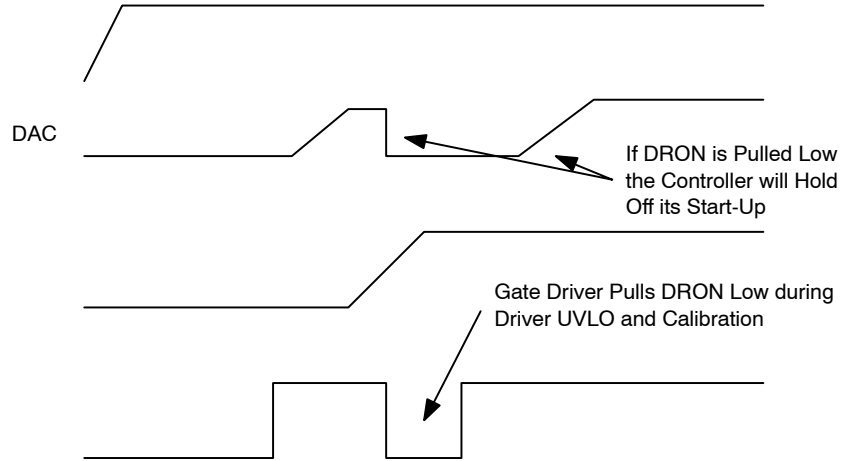


Figure 23. Gate Driver UVLO Restart

Soft Start

Soft start is implemented internally. A digital counter steps the DAC up from zero to the target voltage based on the predetermined SetVID_SLOW rate in the spec table. The PWM signal will start out open with a test current to collect data on SVID address and V_{BOOT} . After the configuration data is collected, if the controller is enabled,

the internal and external PWMs will be set to 2.0 V MID state to indicate that the drivers should be in diode mode. DRON will then be asserted. As the DAC ramps the PWM outputs will begin to fire. Each phase will move out of the MID state when the first PWM pulse is produced. When a controller is disabled the PWM signal will return to the MID state.

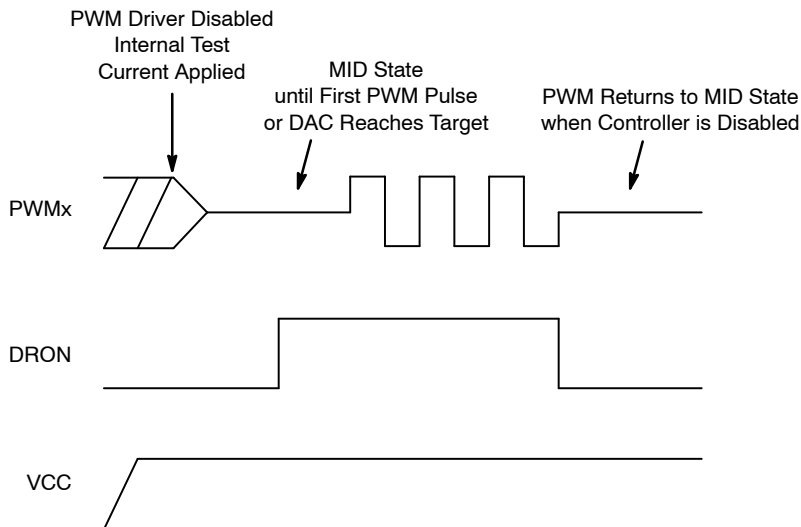


Figure 24. Soft Start

Over Current Latch-Off Protection

Each of the NCP81236P rails compares a programmable current-limit set point to the voltage from the output of its current-summing amplifier. The level of current limit is set with the resistor from the ILIM pin to CSCOMP (two-phase) or to ground (single-phase rails).

Two-Phase Rail Over Current

The current through the external resistor connected between ILIM and CSCOMP is then compared to the internal current-limit threshold. If the current generated through this resistor into the ILIM pin (I_{ILIM}) exceeds the internal current-limit threshold, an internal latch-off counter starts, and the controller shuts down if the fault is not removed after 50 μ s (immediately shut down for 150% of current-limit threshold) after which the outputs will remain disabled until the V_{CC} voltage or EN is toggled.

The voltage swing of CSCOMP cannot go below ground. This limits the voltage drop across the DCR through the current balance circuitry. An inherent per-phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. The over-current limit is programmed by a resistor on the ILIM pin. The resistor value can be calculated by the following equations.

Equation related to the NCP81236P:

$$R_{ILIM} = \frac{I_{LIM} \cdot DCR \cdot \frac{R_{CS}}{R_{PH}}}{I_{CL}} \quad (\text{eq. 24})$$

Where $I_{CL} = 10 \mu\text{A}$

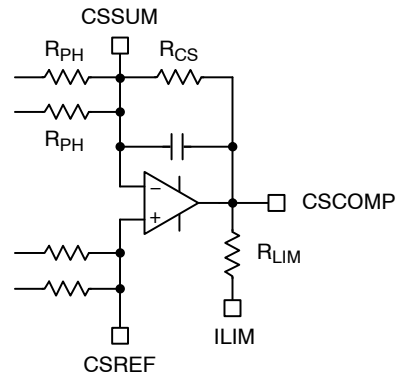


Figure 25.

Under Voltage Monitor

The output voltage is monitored at the output of the differential amplifier for UVLO. If the output falls more than 300 mV below the DAC-DROOP voltage the UVLO comparator will trip sending the VR_RDY signal low.

Over Voltage Protection

The output voltage is also monitored at the output of the differential amplifier for OVP. During normal operation, if the output voltage exceeds the DAC voltage by 400 mV, the VR_RDY flag goes low, and the output voltage will be ramped down to 0 V. At the same time, the high side gate drivers are all turned off and the low side gate drivers are all turned on. The part will stay in this mode until the V_{CC} voltage or EN is toggled.

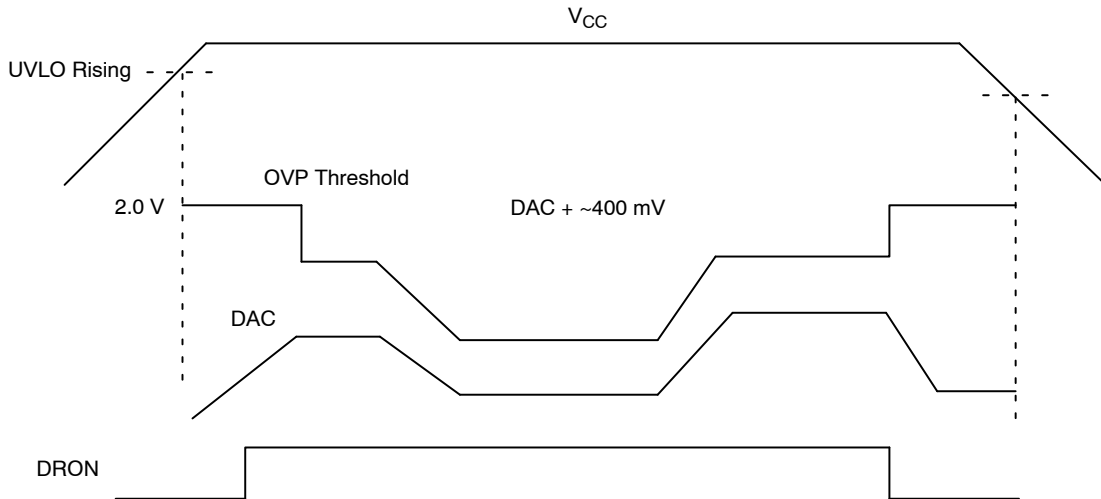


Figure 26. OVP Threshold Behavior

NCP81236P

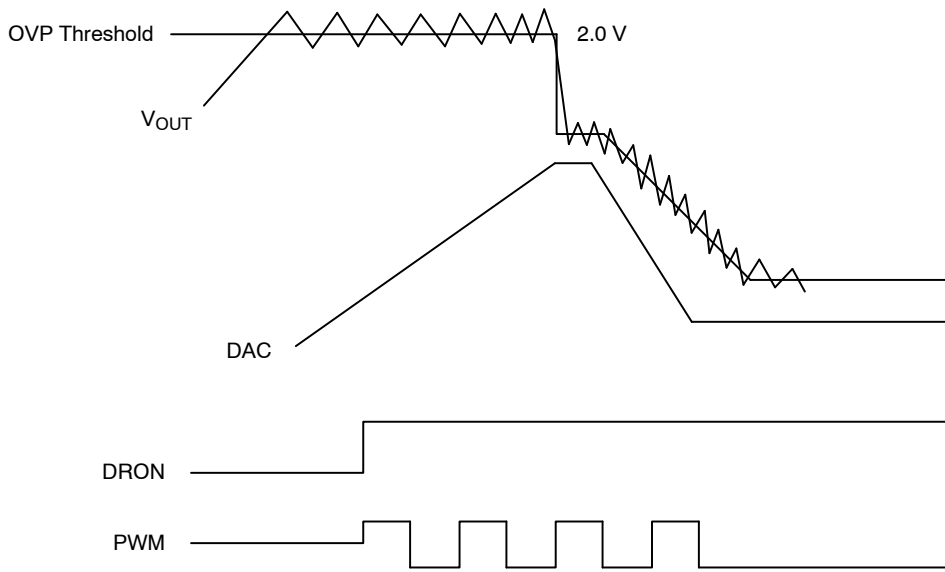


Figure 27. OVP Behavior at Start-Up

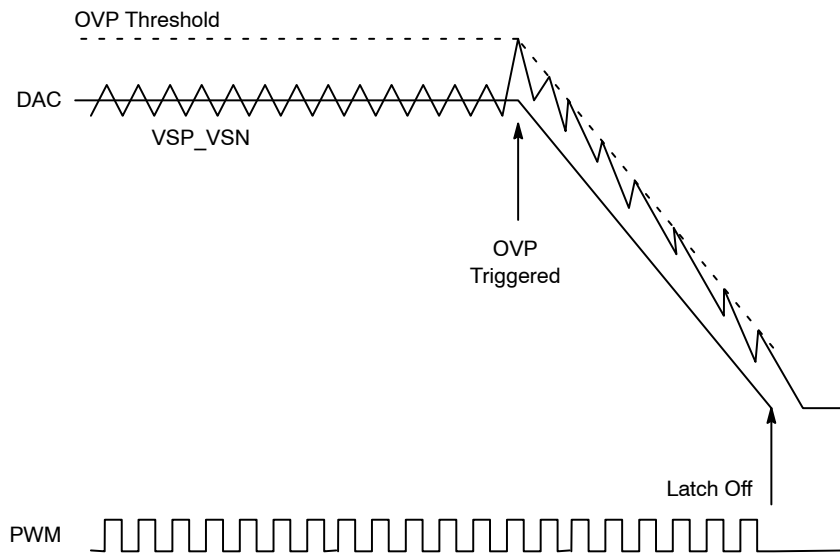


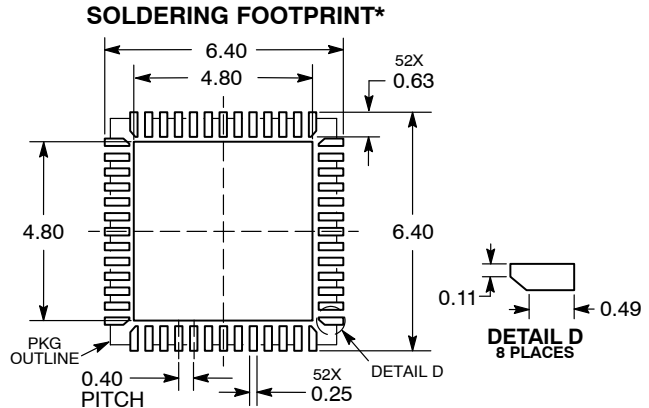
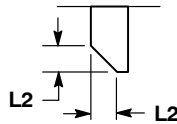
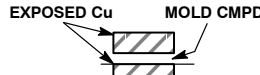
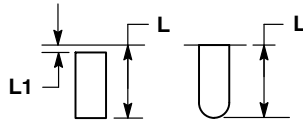
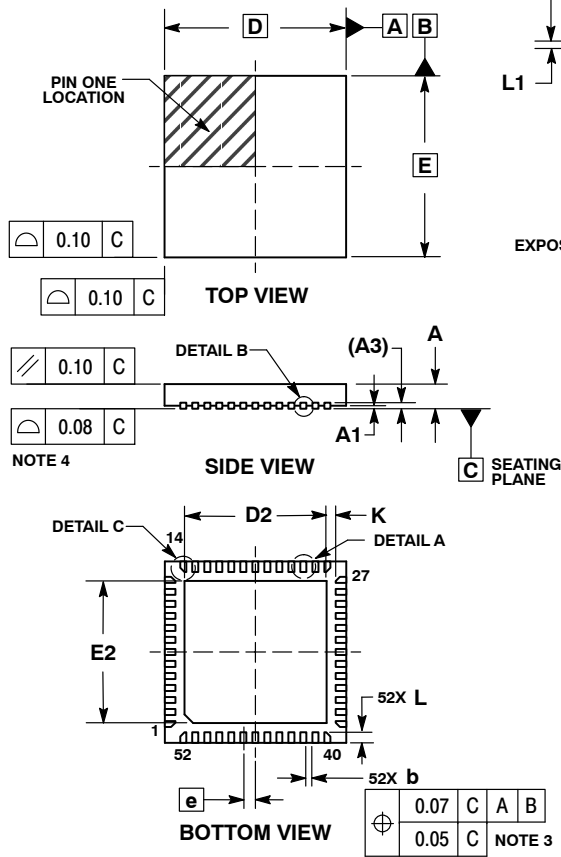
Figure 28. OVP during Normal Operation Mode

During start-up, the OVP threshold is set to 2.0 V. This allows the controller to start up without false triggering the OVP.

NCP81236P

PACKAGE DIMENSIONS

QFN52 6x6, 0.4P CASE 485BE ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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