NCP81273

2-Phase Synchronous Buck Controller with Integrated 12 V Gate Drivers and PWM VID Interface

The NCP81273, a general−purpose 2−phase synchronous buck controller, integrates 12 V gate drivers and PWM VID interface in a QFN−24 package and provides a compact−footprint power management solution for new generation computing processors. It receives power save command (PSI) from processors and operates in 1−phase diode emulation mode to obtain high efficiency in light−load condition. Operating in high switching frequency up to 800 kHz allows employing small size inductor and capacitors. The part is able to support all−ceramic−capacitor applications.

Features

- 4.5 V to 13.2 V Single Supply Voltage
- Integrated 12 V Gate Drivers Powered by PVCC
- Integrated 5 V LDO VCC
- Output Voltage up to 2.0 V with PWM VID Interface
- Differential Output Voltage Sense
- 200 kHz ~ 800 kHz Switching Frequency
- Power Saving Interface (PSI)
- Support both 3.3 V and 1.8 V VID
- Power Good Output
- UVLO on VCC
- Programmable VIN Supply UVLO using EN
- Programmable Over Current Protection
- Over Voltage Protection
- Under Voltage Protection
- Temperature Sense and Alert Output
- Thermal Shutdown Protection
- QFN−24, 4x4 mm, 0.5 mm Pitch Package
- These are Pb−Free Devices

Typical Applications

- GPU and CPU Power
- Graphics Card Applications
- Desktop and Notebook Applications

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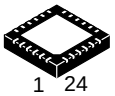
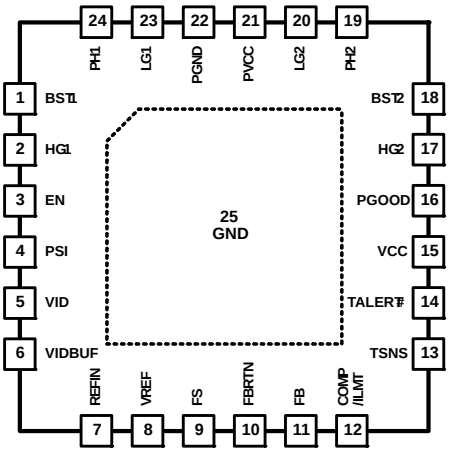


QFN24
MN SUFFIX
CASE 485L

MARKING DIAGRAM

81273	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PINOUT



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81273MNTXG	QFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

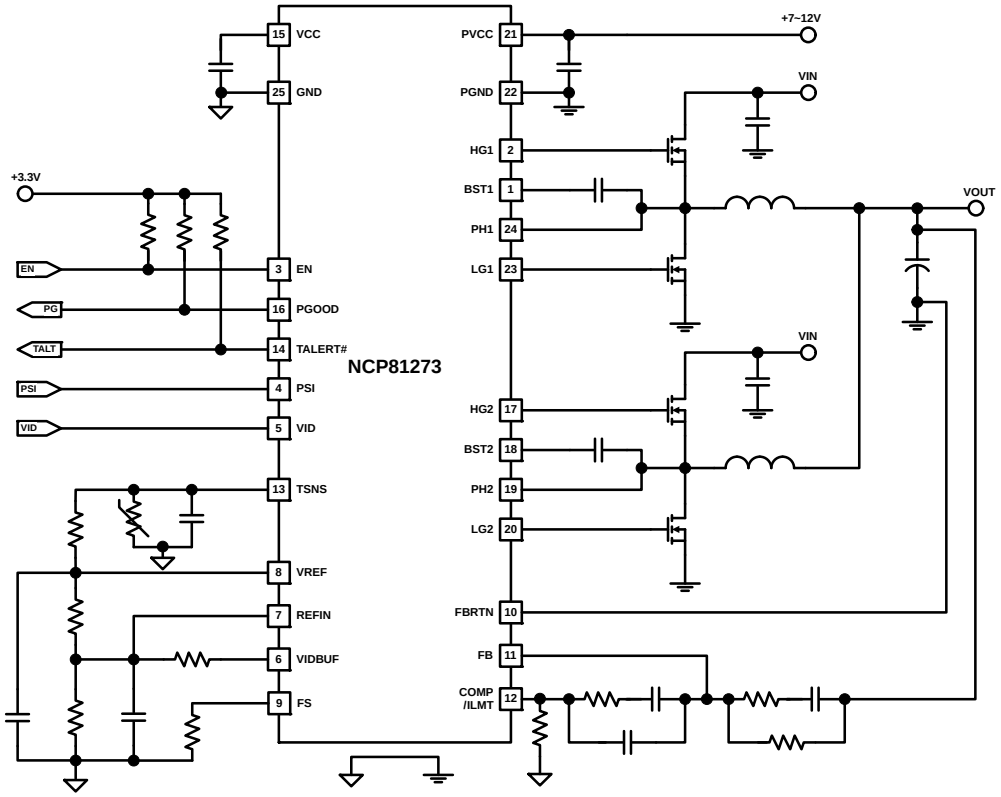


Figure 1. Typical Application Circuit with PWM−VID Interface

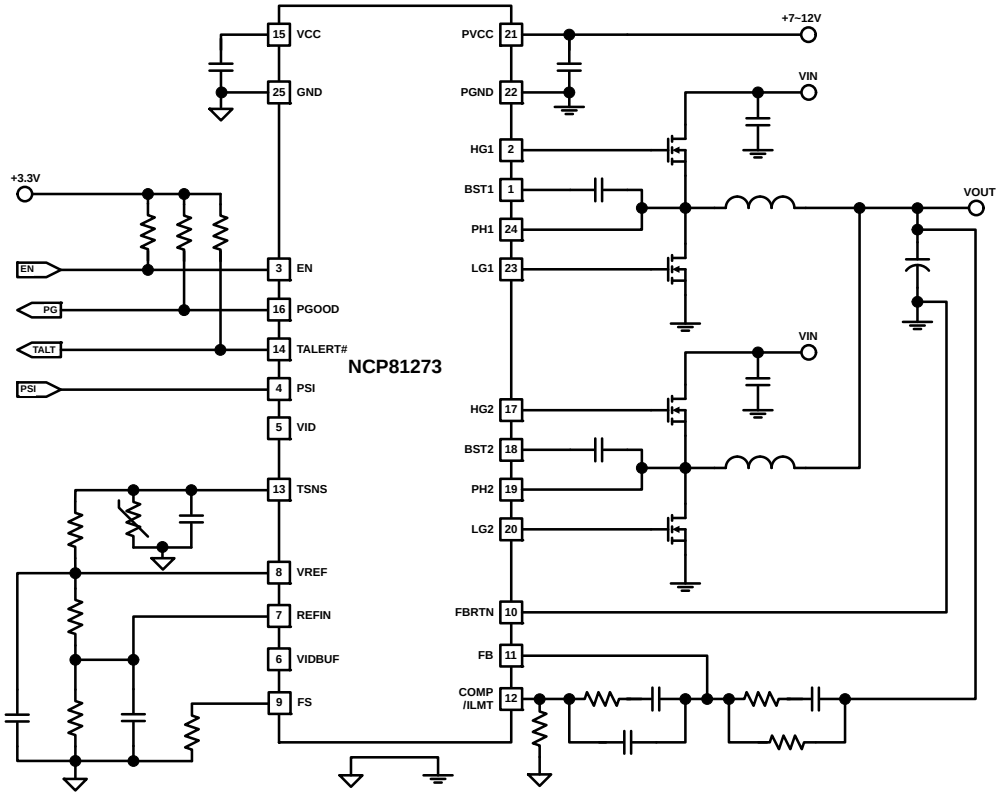


Figure 2. Typical Application Circuit without PWM−VID Interface

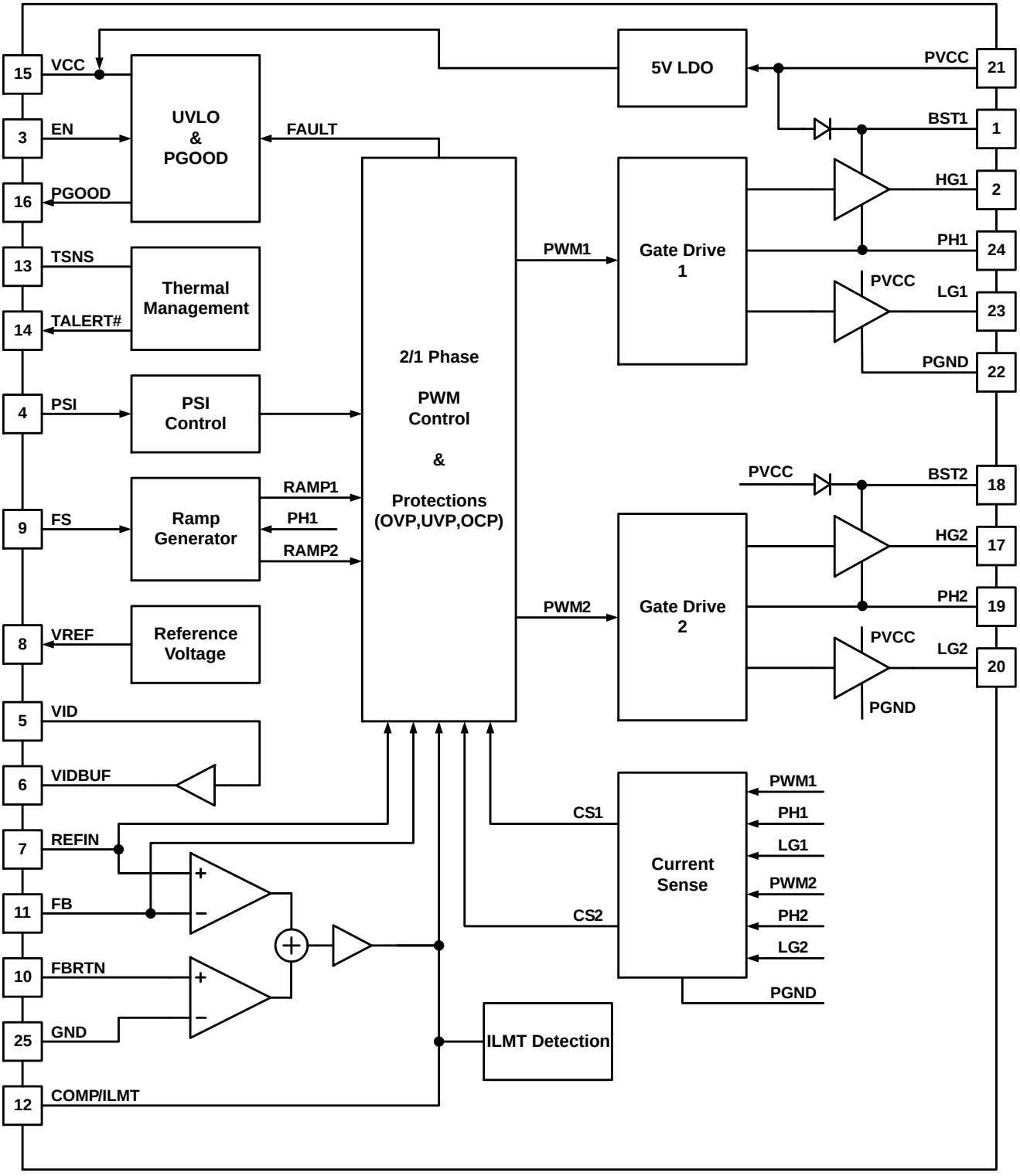


Figure 3. Functional Block Diagram

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	BST1	Analog Power	**Bootstrap 1.** Provides bootstrap voltage for the high−side gate drive of phase 1. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to PH1 (pin 24).
2	HG1	Analog Output	**High−Side Gate 1.** Connected with the gate of the high−side power MOSFET of phase 1.
3	EN	Logic Input	**Enable.** Logic high enables the device and logic low makes the device in standby mode.
4	PSI	Logic Input	**Power Saving Interface.** Logic high enables 2−phase CCM operation, mid−level enables 1−phase CCM operation, and logic low enables 1−phase auto CCM/DCM operation.
5	VID	Logic Input	**Voltage ID.** Voltage ID input from processor.
6	VIDBUF	Analog Output	**Voltage ID Buffer.** VID PWM pulse output from an internal buffer.
7	REFIN	Analog Input	**Reference Input.** Reference voltage input for output voltage regulation. The pin is connected to a non−inverting input of internal error amplifier.
8	VREF	Analog Output	**Output Reference Voltage.** Precise 2 V reference voltage output. A 10 nF ceramic capacitor is required from this pin to GND.
9	FS	Analog Input	**Frequency Selection.** A resistor from this pin to ground programs switching frequency.
10	FBRTN	Analog Input	**Voltage Feedback Return Input.** An inverting input of internal error amplifier.
11	FB	Analog Input	**Feedback.** An inverting input of internal error amplifier.
12	COMP/ILMT	Analog Output	**Compensation / ILMT.** Output pin of error amplifier. A resistor may be applied between this pin and GND to program OCP threshold.
13	TSNS	Analog Input	**Temperature Sensing.** Temperature sensing input.
14	TALERT#	Logic Output	**Thermal Alert.** Open drain output and active low indicates over temperature.
15	VCC	Analog Power	**5 V LDO Output and Voltage Supply of Controller.** Output pin of integrated 5 V LDO and power supply of control circuits. A 4.7 μF or larger ceramic capacitor bypasses this input to GND. This capacitor should be placed as close as possible to this pin.
16	PGOOD	Logic Output	**Power GOOD.** Open−drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
17	HG2	Analog Output	**High−Side Gate 2.** Connected with the gate of the high−side power MOSFET in phase 2.
18	BST2	Analog Power	**Bootstrap 2.** Provides bootstrap voltage for the high−side gate drive of phase 2. A 0.1 μF ~ 1 μF ceramic capacitor is required from this pin to PH2 (pin 19).
19	PH2	Analog Input	**Phase Node 2.** Connected to interconnection between high−side MOSFET and low−side MOSFET in phase 2.
20	LG2	Analog Output	**Low−Side Gate 2.** Connected with the gate of the low−side power MOSFET in phase 2.
21	PVCC	Analog Power	**Voltage Supply of LDO and Gate Drivers.** Power supply input pin of internal 5 V LDO and gate drivers. A 4.7 μF or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
22	PGND	Analog Ground	**Power Ground.** Power ground of internal gate drivers. Must be connected to the system ground.
23	LG1	Analog Output	**Low−Side Gate 1.** Connected with the gate of the low−side power MOSFET in phase 1.
24	PH1	Analog Input	**Phase Node 1.** Connected to interconnection between high−side MOSFET and low−side MOSFET in phase 1.
25	THERM/GND	Analog Ground	**Thermal Pad and Analog Ground.** Ground of internal control circuits. Must be connected to the system ground.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
PH to PGND	V_{PH}	−0.3 −5.5 (<500 ns) −8 (<100 ns)	30	V
Gate Driver Supply Voltage PVCC to GND	V_{PVCC}	−0.3	15	V
BST to PH BST to GND	V_{BST_PH} V_{BST_GND}	−0.3 −0.3	15 30	V
HG to PH	V_{HG}	−0.3 −2 (<200 ns)	BST−PH+0.3	V
LG to GND	V_{LG}	−0.3 −2 (<200 ns)	PVCC+0.3	V
PGND to GND	V_{PGND}	−0.3	0.3	V
FBRTN to GND	V_{FBRTN}	−0.3	0.3	V
Other Input Pins to GND		−0.3	VCC+0.3	V
Latch up Current: (Note 2) All pins, except digital pins Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range (Note 3 and 4)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C
Storage Temperature Range	T_{STG}	−40	150	°C
Thermal Resistance Junction to Top Case(Note 5)	$R_{\Psi JC}$	7.0		°C/W
Thermal Resistance Junction to Board (Note 5)	$R_{\Psi JB}$	6.0		°C/W
Thermal Resistance Junction to Ambient (Note 4)	$R_{\theta JA}$	44.5		°C/W
Power Dissipation (Note 6)	P_D	2.25		W
Moisture Sensitivity Level (Note 7)	MSL	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is ESD sensitive. Handling precautions are needed to avoid damage or performance degradation.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. JEDEC standard JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM.
5. JEDEC standard JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM. It is for checking junction temperature using external measurement.
6. The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected. Tambient = 25°C, Tjunc_max = 125°C, PD = (Tjunc_max−T_amb)/Theta JA.
7. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Table 3. ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{VCC} = 5 V, V_{PVCC} = 12 V, V_{REFIN} = 1.0 V, typical values are referenced to $T_A = T_J$ = 25°C, Min and Max values are referenced to $T_A = T_J$ = −40°C to 100°C. unless other noted.)

Characteristics	Test Conditions		Symbol	Min	Typ	Max	Units
SUPPLY VOLTAGE							
VCC Under−Voltage (UVLO) Threshold	VCC falling		V_{CCUV-}	4.3	4.43	4.5	V
VCC OK Threshold	VCC rising		V_{CCOK}	4.55	4.65	4.75	V
SUPPLY CURRENT							
PVCC Quiescent Supply Current	EN high, no switching		I_{PCC}	−	4.64	7.0	mA
PVCC Shutdown Current	EN low		I_{sdPCC}	−	−	550	μA
5 V LDO VCC							
VCC Output Voltage	PVCC = 7 V to 12 V; IVCC < 100 mA		V_{CC}	4.8	5	5.5	V
Maximum LDO Current	VCC > 4.5 V		I_{PCC}	100			mA
SWITCHING FREQUENCY SETTING							
PS0 Switching Frequency Range	(Note 8)		F_{SW}	200		800	kHz
FS Voltage	RFS = 39.2 kΩ		V_{FS}		2.0		V
VOLTAGE REFERENCE							
VREF Reference Voltage	I_{REF} = 1 mA		V_{VREF}	1.98	2.0	2.02	V
PWM MODULATION							
Minimum On Time	(Note 8)		T_{on_min}		50		ns
Minimum Off Time	(Note 8)		T_{off_min}		250		ns
Maximum Duty Cycle	(Note 8)		D_{max}	−	100	−	%
VOLTAGE ERROR AMPLIFIER							
Open−Loop DC Gain	(Note 8)		$GAIN_{EA}$		80		dB
Unity Gain Bandwidth	(Note 8)		GBW_{EA}		20		MHz
Slew Rate	(Note 8)		SR_{COMP}		20		V/μs
COMP Voltage Swing	I_{COMP}(source) = 2 mA		$V_{maxCOMP}$	3.0	3.3	−	V
	I_{COMP}(sink) = 2 mA		$V_{minCOMP}$	−	0.86	1.1	V
FB, REFIN Bias Current	$V_{FB} = V_{REFIN}$ = 1.0 V		I_{FB}	−400		400	nA
Input Offset Voltage	$V_{osEA} = V_{REFIN} - V_{FB}$ (Note 8)	T_J = 25°C	V_{osEA}	−0.6		0.6	mV
		T_J from −40°C to 100°C		−8.0		8.0	
REFIN Discharge Switch ON−Resistance	I_{REFIN} (sink) = 2 mA				6.06		Ω
CURRENT−SENSE AMPLIFIER							
Closed−Loop DC Gain			$GAIN_{CA}$		−4.85		V/V
−3 dB Gain Bandwidth	(Note 8)		BW_{CA}		10		MHz
Input Offset Voltage	$V_{osCS} = V_{PH} - V_{GND}$ (Note 8)		V_{osCS}	−500	−	500	uV
ENABLE							
EN High Threshold			V_{EN_TH}		1.2		V
EN Internal Resistance			R_{EN_INT}		42		kΩ
EN Hysteresis Current	External 1 K pull−up to 1.8 V		I_{EN_HYS}	4.3	6.0	7.4	μA
POWER SAVE INPUT							
High Threshold	PS0: 2−Phase CCM Mode		$V_{highPSI}$	1.5			V
Mid Voltage level	PS1: 1−Phase CCM Mode		V_{midPSI}	0.6		1.2	V
Low Threshold	PS2: 1−Phase Auto CCM/DCM Mode		V_{lowPSI}			0.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design, not tested in production.

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Characteristics	Test Conditions		Symbol	Min	Typ	Max	Units
POWER SAVE INPUT							
Internal Pull High Resistance	PSI to internal 1.8 V				100		kΩ
Internal Pull Low Resistance	PSI to GND				100		kΩ
SOFT START and PGOOD							
Vout Startup Delay	From EN to Vout Start up (Note 8)				303		μs
Vout Startup Slew Rate	(Note 8)				0.643		V/ms
PGOOD Startup Delay	Measured from EN to PGOOD assertion					2.0	ms
PGOOD Shutdown Delay	Measured from EN to PGOOD de−assertion				256		ns
PGOOD Low Voltage	I_{PGOOD}= 4 mA (sink)		V_{IPGOOD}	−	−	0.3	V
PGOOD Leakage Current	PGOOD = 5 V		$I_{lkgPGOOD}$	−	−	1.0	μA
PROTECTION							
Current Limit Threshold	Measured from GND to PHx (R_{ILMT} (1%) is connected from COMP to GND)	R_{ILMT} = open	V_{OCTH}	80	90	102	mV
		R_{ILMT} = 75.0 k		99	110	123	
		R_{ILMT} = 56.2 k		121	135	151	
		R_{ILMT} = 33.2 k		162	180	196	
		R_{ILMT} = 11 k		OCP is disabled			−
Source Current of OCP Programming	Source out COMP pin		I_{ILMT}	9.5	10	10.5	μA
Fast Under Voltage Protection (FUVP) Threshold	Voltage from FB to GND			0.15	0.2	0.25	V
Fast Under Voltage Protection (FUVP) Delay	(Note 8)				1.0		μs
Slow Under Voltage Protection (SUVP) Threshold	Voltage from COMP to GND				2.95		V
Slow Under Voltage Protection (SUVP) Delay	(Note 8)				50		μs
Over Voltage Protection (OVP) Threshold	Voltage from FB to GND			1.85	2.0	2.15	V
Over Voltage Protection (OVP) Delay	(Note 8)				1.0		μs
Over Temperature Protection (OTP) Threshold	(Note 8)		T_{sd}	140	150		°C
Recovery Temperature Threshold	(Note 8)		T_{rec}		125		°C
Over Temperature Protection (OTP) Delay	(Note 8)				125		ns
OUTPUT DISCHARGE							
Output Discharge Resistance per Phase	Measured from PHx to GND when EN is low (Note 8)		$R_{dischrg}$		2.5		kΩ
TSENSE and ALERT							
TALERT# Assert Threshold	Measured at TSNS (Temperature Rising)		$V_{lowTSNS}$	0.99	1.00	1.01	V
TALERT# De−Assert Threshold	Measured at TSNS (Temperature Falling)		$V_{highTSNS}$	−	1.05	−	V
TALERT# Low Voltage	I_{ALERT}= 4 mA (sink)		$V_{lowALERT}$	−	-	0.3	V
TALERT# Leakage Current	TALERT# = 5 V		$I_{lkgALERT}$	−	−	1.0	μA
PWM−VID BUFFER							
Input High Threshold			$V_{highVID}$	1.5			V
Input Low Threshold			V_{lowVID}			0.3	V

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Units
PWM−VID BUFFER						
Internal Pull High Resistance in VID Pin	VID to internal 1.8 V			100		kΩ
Internal Pull Low Resistance in VID Pin	VID to GND			100		kΩ
3−State Shut−Off Time		$T_{D\_HOLD-OFF}$		325		ns
Buffer Output Rise Time		T_r		3		ns
Buffer Output Fall Time		T_f		3		ns
Propagation Delay	$T_{pd} = T_{pHL} = T_{pLH}$	T_{pd}		8		ns
INTERNAL HIGH−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{BST} - V_{PH}$ = 12 V, I_{HG} = 2 mA (source)	R_{DRV_HH}	−	3.5	-	Ω
Pull−Low Drive ON Resistance	$V_{BST} - V_{PH}$ = 12 V, I_{HG} = 2 mA (sink)	R_{DRV_HL}	−	1.6	-	Ω
HG Propagation Delay Time	From LG off to HG on	T_{pdHG}		52		ns
INTERNAL LOW−SIDE GATE DRIVE						
Pull−High Drive ON Resistance	$V_{PVCC} - V_{PGND}$ = 12 V, I_{LG} = 2 mA (source)	R_{DRV_LH}	−	2.0	-	Ω
Pull−Low Drive ON Resistance	$V_{PVCC} - V_{PGND}$ = 12 V, I_{LG} = 2 mA (sink)	R_{DRV_LL}	−	1.0	-	Ω
LG Propagation Delay Time	From HG off to LG on	T_{pdLG}		48		ns
BOOTSTRAP						
On Resistance of Rectifier Switch	V_{PVCC} = 12 V, Id = 2 mA, T_A = 25°C	R_{BST}	-	12	25	Ω
Rectifier Switch Leakage Current	V_{PVCC} = 12 V, EN = 0 V	I_{lkgBST}	-	-	110	μA
Rectifier Forward Voltage	Ifw = 100 μA			0.3		V

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DETAILED DESCRIPTION

General

The NCP81273, a 2−phase synchronous buck controller, integrates 12 V gate drivers and PWM VID interface in a QFN−24 package and provides a compact−footprint power management solution for new generation computing processors. It receives power save input (PSI) from processors and operates in 1−phase diode emulation mode to obtain high efficiency in light−load condition. Operating in high switching frequency up to 800 kHz allows employing small size inductors and capacitors. The part is able to support all−ceramic−capacitor applications.

Operation Modes

The NCP81273 has total 3 power operation modes responding to PSI levels as shown in Table 4. The three operation modes can be changed on the fly. In 1−phase operation, no switching in phase 2.

Table 4.
POWER SAVING INTERFACE (PSI) Configurations

PSI Level	Power Mode	Phase Configuration
High	PS0	2−Phase, CCM
Middle	PS1	1−Phase, CCM
Low	PS2	1−Phase, Auto CCM/DCM

The NCP81273 is also able to support pure 1−phase applications without a need to stuff components for phase 2. In this configuration, the four pins including BST2, HG2, LG2, and PH2 can be float, but make sure the voltage at PSI pin is never in high level.

Enable and Input UVLO

The NCP81273 is enabled when the voltage at EN pin is higher than an internal threshold V_{EN_TH} = 1.2 V. A hysteresis can be programmed by an external resistor R_{EN} connected to EN pin as shown in Figure 4. The high threshold V_{EN_H} in ENABLE signal is

$$V_{EN\_H} = V_{EN\_TH} \quad \text{(eq. 1)}$$

The low threshold V_{EN_L} in ENABLE signal is

$$V_{EN\_L} = V_{EN\_TH} - V_{EN\_HYS} \quad \text{(eq. 2)}$$

The hysteresis V_{EN_HYS} is

$$V_{EN\_HYS} = I_{EN\_HYS} \cdot \left(R_{EN\_INT} + R_{EN}\right) \quad \text{(eq. 3)}$$

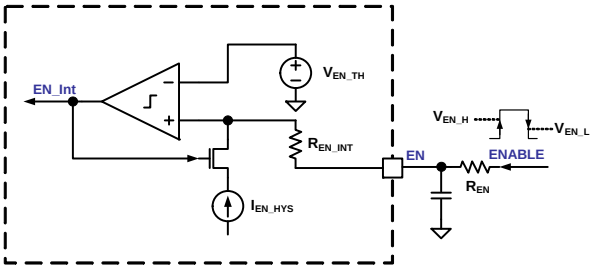


Figure 4. Enable and Hysteresis Programming

A UVLO function for input power supply can be implemented at EN pin. As shown in Figure 5, the UVLO thresholds can be programmed by two external resistors. The high threshold V_{IN_H} in VIN signal is

$$V_{IN\_H} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \cdot V_{EN\_TH}, \quad \text{(eq. 4)}$$

The low threshold V_{IN_L} in VIN signal is

$$V_{IN\_L} = V_{IN\_H} - V_{IN\_HYS} \quad \text{(eq. 5)}$$

The hysteresis V_{IN_HYS} is

$$V_{IN\_HYS} = I_{EN\_HYS} \cdot \left(R_{EN\_INT} + R_{EN1}\right) \quad \text{(eq. 6)}$$

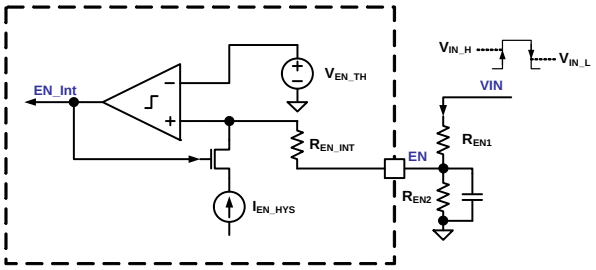


Figure 5. Enable and Input Supply UVLO Circuit

To avoid undefined operation, EN pin cannot be left float in applications.

Remote Voltage Sense

A high performance and high input impedance differential error amplifier, as shown in Figure 6, provides an accurate sense for the output voltage of the regulator. The output voltage and FBRTN inputs should be connected to the regulator's output voltage sense points via a Kelvin−sense pair. The output voltage sense signal goes through a compensation network and into the inverting input (FB pin) of the error amplifier. The non−inverting input of the error amplifier is connected to the reference input (REFIN pin).

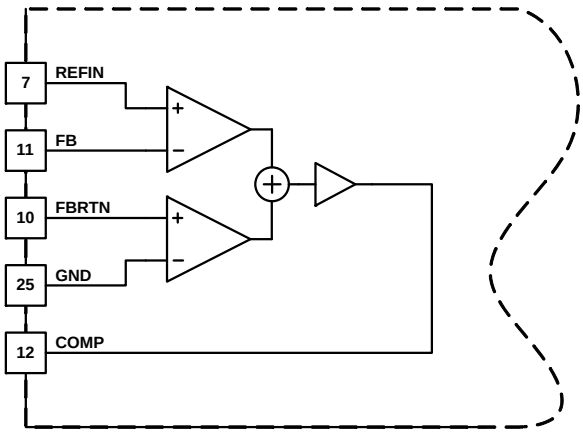


Figure 6. Differential Error Amplifier

PWM VID

The NCP81273 receives a PWMVID signal at VID pin for the output voltage regulation. Figure 7 shows the PWMVID dynamic voltage control circuit diagram. The duty cycle modulated PWM VID signal, independent from its signal level of 3.3 V or 1.8 V, is converted into a fixed−amplitude 2 V PWM−VID signal and passed to the VIDBUF output. If VID input is left floating or driven by z−state signal for more than ~100 ns, VIDBUF enters into z−state. The VIDBUF signal is filtered through an external low−pass filter constructed by R_VIDBUF and C_REFIN. The filtered output is connected to REFIN pin. REFIN is the voltage reference of the output voltage regulator. The dynamic range of the circuit is determined by the external resistor network. The resistor network and capacitor C_REFIN function as a filter for the PWMVID signal, and will affect ripple voltage and transition slew rate in REFIN signal.

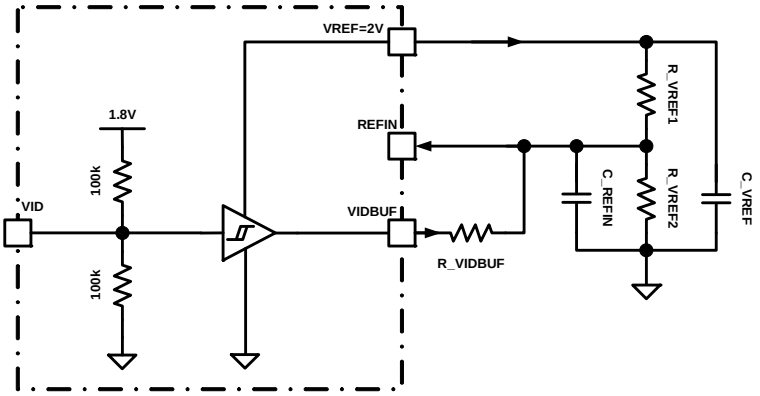


Figure 7. PWM VID Interface

Switching Frequency

Switching frequency is programmed by a resistor R_{FS} applied from the FS pin to ground. The typical frequency range is from 200 KHz to 800 kHz. The FS pin provides approximately 2 V out and the source current is mirrored into the internal ramp generator. The switching frequency in 2−phase operation (PS0 mode) can be estimated by

$$F_{SW(kHz)} = 16486 \cdot R_{FS(k\Omega)}^{-0.961}. \qquad \text{(eq. 7)}$$

To reduce output ripple in 1−phase operation, the switching frequency in PS1 and PS2 modes is set to be higher than PS0 mode, which can be estimated by

$$F_{SW(kHz)} = 15783 \cdot R_{FS(k\Omega)}^{-0.873}. \qquad \text{(eq. 8)}$$

Figure 8 shows a measurement based on a typical application under condition of Vin = 12 V, Vout = 0.9 V, Iout = 10 A for PS1 mode operation and Iout = 20 A for PS0 mode operation. It can also be found that the lower Rdson of the low−side MOSFETs the smaller frequency difference between PS0 mode and PS1 mode.

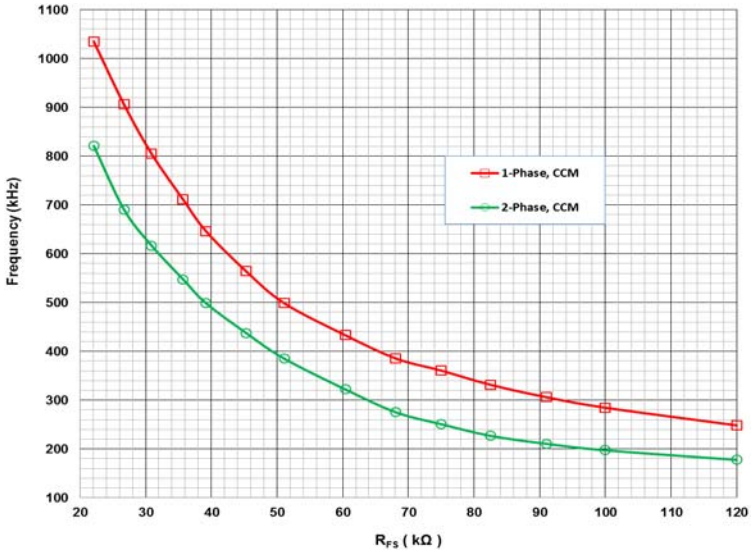


Figure 8. Switching Frequency Programmed by Resistor R_{FS} at FS Pin

Soft Start

The NCP81273 has a soft start function. The output starts to ramp up following a system reset period after the device is enabled. The device is able to start up smoothly under an output pre−biased condition without discharging the output before ramping up.

REFIN Discharge

An internal switch in REFIN pin starts to short REFIN to GND just after EN is pulled high and it turns off just before the beginning of the soft start. The typical on resistance of the switch is 6.25 Ω.

Output Discharge in Shut Down

The NCP81273 has an output discharge function when the device is in shutdown mode. The resistors from PH node to PGND in both phases are active to discharge the output capacitors.

Over Current Protection

The NCP81273 protects converters from over current. The current through each phase is monitored by voltage sensing from phase node PHx to GND pin. The sense signal is compared to an internal voltage threshold. Once over load happens, the inductor current is limited to an average current per phase, which can be estimated by

$$I_{LMT(phase)} = \frac{V_{thOC}}{R_{DS(phase)}}, \qquad \text{(eq. 9)}$$

where RDS(phase) is a total on conduction resistance of low−side MOSFETs per phase. Normally, a continuous over load event leads to a voltage drop in the output voltage and possible to eventually trip under voltage protection.

The over−current threshold can be externally programmed by adding a 1% tolerance resistor between COMP pin and GND. The selectable thresholds can be found in the electrical table. To assure accurate resistance detection, the total capacitance from COMP pin to FB pin should be less than 330 pF.

Under Voltage Protection

There are two under voltage protections implemented in the NCP81273, which are fast under voltage protection and slow under voltage protection.

Fast under voltage protection (FUVP) protects converters in case of an extreme short circuit in output by monitoring FB voltage. Once FB voltage drops below 0.2 V for more than 1 μs, the NCP81273 latches off, both the high−side MOSFETs and the low−side MOSFETs in all phases are turned off. The fault remains set until the system has either VCC or EN toggled state. The FUVP function is disabled in soft start.

Slow under voltage protection (SUVP) of the NCP81273 is based on voltage detection at COMP pin. In normal operation, COMP level is below 2.5 V. When the output voltage drops below REFIN voltage for long time and COMP rises to be over 2.95 V, an internal UV fault timer will be triggered. If the fault still exists after 50us, the NCP81273 latches off, both the high−side MOSFETs and the low−side MOSFETs in all phases are turned off. The fault remains set until the system has either VCC or EN toggled state.

Over Voltage Protection

Over voltage protection of the NCP81273 is based on voltage detection at FB pin. Once FB voltage is over 2 V for more than 1 μs, all the high−side MOSFETs are turned off and all the low−side MOSFETs are latched on. The NCP81273 latches off until the system has either VCC or EN has toggled state.

Temperature Sense and Thermal Alert

The NCP81273 provides external temperature sense and thermal alert in the normal operation mode, and disables the function in the standby mode. The temperature sense and thermal alert circuit diagram is shown in Figure 9. An external voltage divider, consisting of a NTC thermistor R_NTC and a resistor R_TSNS, is employed to sense temperature and program alert level. Usually the thermistor is placed close to a hot spot like a power MOSFET. The NCP81273 monitors the voltage at TSNS pin and compares the voltage to an internal 1 V threshold by an internal comparator. Once the TSNS voltage drops below 1 V, the comparator turns on an open−drain switch at TALERT# pin and thus indicates a high temperature alert. The thermal alert can be de−asserted when TSNS voltage raises back to be higher than 1.05 V. In an exemplary application where a 100 kΩ (B = 4250 at 25°C) NTC thermistor is applied together with a 5.62 kΩ resistor, an low−valid thermal alert signal is asserted when the temperature of the NTC thermistor reaches 100°C and de−asserted when the temperature drops down to 97°C.

Thermal Shutdown

The NCP81273 has a thermal shutdown protection to protect the device from overheating when the die temperature exceeds 150°C. Once the thermal protection is triggered, the fault state can be ended by re−applying VCC and/or EN if the temperature drops down below 125°C.

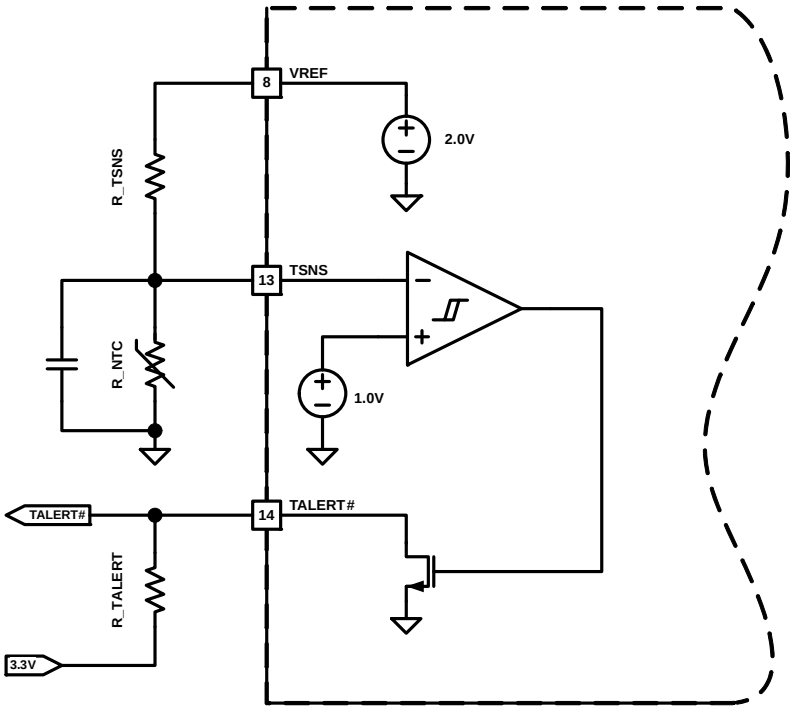


Figure 9. Temperature Sense and Thermal Alert Circuit Diagram

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction.

- **Power Paths:** Use wide and short traces for power paths to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling:** The power MOSFET bridges should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Place decoupling caps as close as possible to the controller VCC and VCCP pins.
- **Output Decoupling:** The output capacitors should be as close as possible to the load like a GPU. If the load is distributed, the capacitors should also be distributed and generally placed in greater proportion where the load is more dynamic.
- **Switching Nodes:** Switching nodes between HS and LS MOSFETs should be copper pours to carry high current and dissipate heat, but compact because they are also noise sources.
- **Gate Drive:** All the gate drive traces such as HGx, LGx, PHx, and BSTx should be short, straight as possible, and not too thin. The bootstrap cap and an option resistor need to be very close and directly connected between BSTx pin and PHx pin.
- **Ground:** It would be good to have separated ground planes for PGND and GND and connect the two planes at one point. PGND plane is an isolation plane between noisy power traces and all the sensitive control circuits. Directly connect the exposed pad (GND pin) to GND ground plane through vias. The analog control circuits should be surrounded by GND ground plane. GND ground plane is connected to PGND plane by single joint with low impedance.
- **Voltage Sense:** Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- **Current Sense:** The NCP81273 senses phase currents by monitoring voltages from phase nodes PHx to the common ground PGND pin. PGND ground plane should be well underneath PHx trances. To get better current balance between the two phases, try to make a layout as symmetrical as possible and balance the current flow in PGND plane for the two phases.
- **Temperature Sense:** A NTC thermistor is placed close to a hot spot like a power MOSFET, and a filter capacitor is placed close to TSNS pin of the controller. To avoid the traces from/to the NTC thermistor to cross over other sensitive control circuits.
- **Compensation Network:** The compensation network should be close to the controller. Keep FB trace short to minimize their capacitance to GND.
- **PWM VID Circuit:** The PWM VID is a high slew−rate digital signal from GPU to the controller. The trace routing of it should be done to avoid noise coupling from the switching node and to avoid coupling to other sensitive analog circuit as well. The RC network of the PWM VID circuit needs to be close to the controller. A 10 nF ceramic cap is connected from VREF pin to GND plane, and another small ceramic cap is connected from REFIN pin to GND plane.

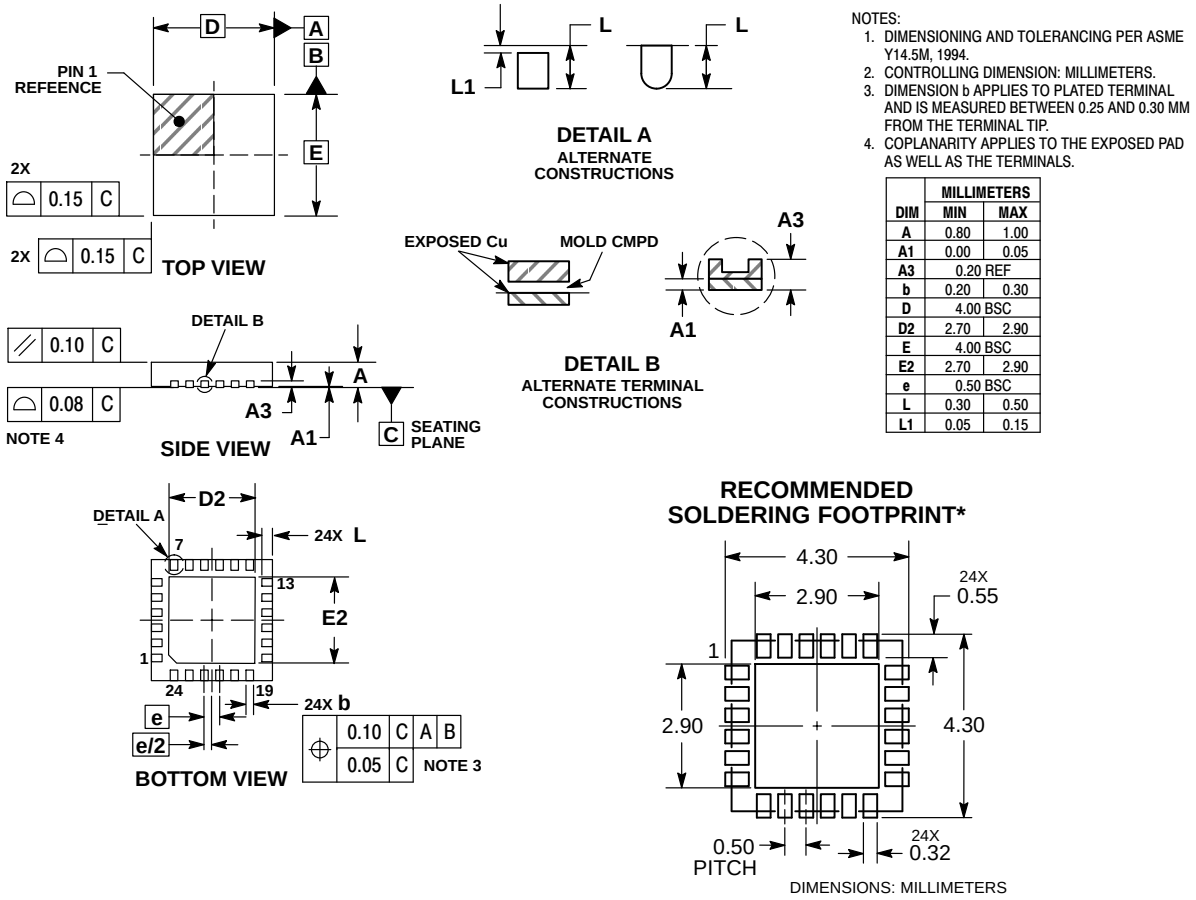
Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small−form factor VR with reduced temperature rise.

- The exposed pads of the controller and power MOSFETs must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More vias are welcome to be underneath the exposed pads and surrounding the power devices to connect the inner ground layers to reduce thermal resistances.
- Use large area copper pour to help thermal conduction and radiation.
- Try distributing multiple heat sources to reduce temperature rise in hot spots.

PACKAGE DIMENSIONS

QFN24, 4x4, 0.5P
CASE 485L
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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