NCS20561, NCV20561, NCS20562, NCV20562, NCS20564, NCV20564

Product Preview

Precision Operational Amplifier, Low Offset, Wide Bandwidth, Rail-to-Rail Input/Output

The NCS2056x family of high precision op amps feature rail−to−rail input and output, and wide bandwidth. These low quiescent current, low noise amplifiers are trimmed to provide a low initial input offset voltage. These op amps operate over a supply range from 2.2 V to 5.5 V. The NCS2056x and NCV2056x each come in several different pinout configurations and packages. All versions are specified for operation from −40°C to +125°C.

Features

- Gain Bandwidth: 10 MHz Typical
- Trimmed Offset Voltage: 65 μV Max (V_S = 5.5 V)
- Supply Voltage: 2.2 V to 5.5 V
- Quiescent Current: 1.2 mA Max
- Voltage Noise Density: 10 nV/$\sqrt{Hz}$ Typical
- Rail−to−Rail Input and Output
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Current Sensing
- Current Sensing in Motor Control Circuits
- Current Monitor for Power Supplies
- Battery Powered Instrumentation
- Transducer or Sensor Interface
- Medical Instrumentation

End Products

- Industrial
- Power Supplies
- Computers and Servers
- Automotive
- Medical Instrumentation

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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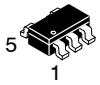
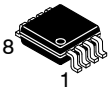


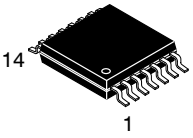
SC−74A
CASE 318BQ

SC−88A
CASE 419A

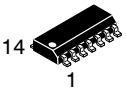


Micro8
CASE 846A

SOIC−8 NB
CASE 751



TSSOP−14 WB
CASE 948G



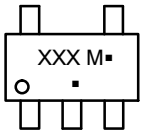
SOIC−14 NB
CASE 751A

ORDERING INFORMATION

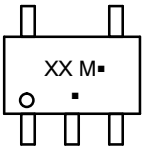
See detailed ordering and shipping information on page 3 of this data sheet.

DEVICE MARKING INFORMATION

Single Channel Configuration
NCS20561, NCV20561

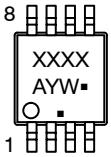


SC−74A
CASE 318BQ

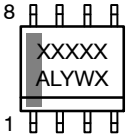


SC70−5
CASE 419A

Dual Channel Configuration
NCS20562, NCV20562

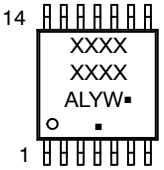


Micro8
CASE 846A

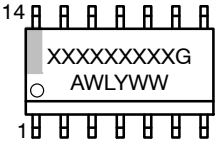


SOIC−8
CASE 751

Quad Channel Configuration
NCS20564, NCV20564



TSSOP−14
CASE 948G



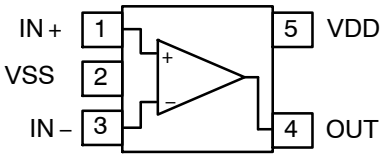
SOIC−14
CASE 751A

XXX = Specific Device Code
M = Date Code
A or AL = Assembly Location
WL = Wafer Lot
Y = Year
W or WW = Work Week
G or ▪ = Pb−Free Package

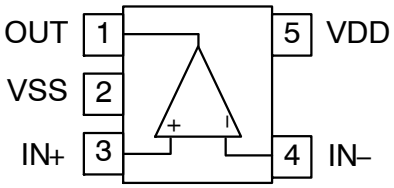
(Note: Microdot may be in either location)

PIN CONNECTIONS

Single Channel Configuration
NCS20561, NCV20561

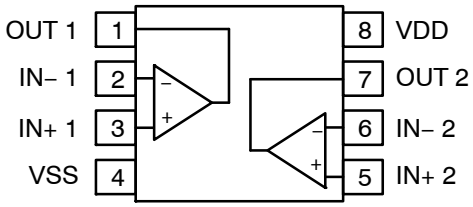


SC–74A and SC88A / SC70–5
SN3/SQ3 Pinout



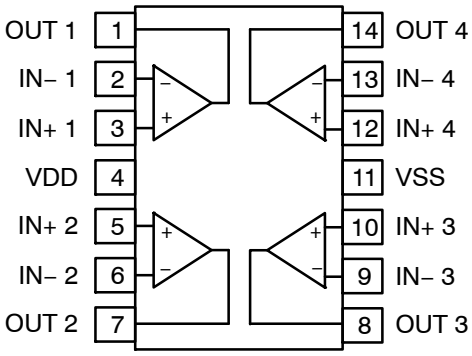
SC–74A and SC88A / SC70–5
SN2/SQ2 Pinout

Dual Channel Configuration
NCS20562, NCV20562



MICRO8 / SOIC8

Quad Channel Configuration
NCS20564, NCV20564



TSSOP14 / SOIC14

ORDERING INFORMATION

Device	Configuration	Marking	Package	Shipping†
INDUSTRIAL				
NCS20561SN2T1G (In Development)**	Single	TBD	SC–74A	3000 / Tape and Reel
NCS20561SN3T1G (In Development)**		TBD		
NCS20561SQ2T1G (In Development)**		TBD	SC88A / SC70–5	
NCS20561SQ3T1G (In Development)**		TBD		
NCS20562DMR2G (In Development)**	Dual	TBD	MICRO–8	
NCS20562DR2G (In Development)**		TBD	SOIC–8	
NCS20564DB0R2G (In Development)**	Quad	TBD	TSSOP–14	
NCS20564DR2G (In Development)**		TBD	SOIC–14	
AUTOMOTIVE				
NCV20561SN2T1G* (In Development)**	Single	TBD	SC–74A	3000 / Tape and Reel
NCV20561SN3T1G* (In Development)**		TBD		
NCV20561SQ2T1G* (In Development)**		TBD	SC88A / SC70–5	
NCV20561SQ3T1G* (In Development)**		TBD		
NCV20562DMR2G* (In Development)**	Dual	TBD	MICRO–8	
NCV20562DR2G* (In Development)**		TBD	SOIC–8	
NCV20564DB0R2G* (In Development)**	Quad	TBD	TSSOP–14	
NCV20564DR2G* (In Development)**		TBD	SOIC–14	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV prefix for automotive and other applications requiring unique site and control change requirements; AEC–Q100 qualified and PPAP capable
** Contact local sales office for more information

Table 1. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature, unless otherwise stated.

Parameter	Rating	Unit
Supply Voltage (V_{DD} − V_{SS})	6	V
INPUT AND OUTPUT PINS		
Input Voltage (Note 1)	V_{SS} − 0.3 to V_{DD} + 0.3	V
Differential Input Voltage (Note 1)	$\pm V_s$	V
Input Current (Note 1)	±10	mA
Output Short Circuit Current (Note 2)	Continuous	
TEMPERATURE		
Operating Temperature	−40 to +125	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	+150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions	+260	°C
ESD RATINGS (Note 3)		
Human Body Model (HBM)	2000	V
Charged Device Model (CDM)	2000	V
OTHER RATINGS		
Latch−up Current (Note 4)	100	mA
Moisture Sensitivity Level (MSL)	1	
Continuous Total Power Dissipation	200	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Input terminals are diode clamped to the power supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less
2. Short−circuit to ground up to T_A = 125°C.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JEDEC standard JS−001−2017 (AEC−Q100−002)
   ESD Charged Device Model tested per JEDEC standard JS−002−2014 (AEC−Q100−011)
4. Latch−up Current tested per JEDEC standard JESD78E (AEC−Q100−004)

Table 2. THERMAL INFORMATION (Note 5)

Parameter	Symbol	Package	Value	Unit
Junction to Ambient	θ_{JA}	SC−74A	198	°C/W
		SC88A / SC70−5	247	
		Micro8	TBD	
		SOIC−8	TBD	
		TSSOP−14	TBD	
		SOIC−14	TBD	

5. As mounted on an 80x80x1.5 mm FR4 PCB with 600 mm^2 and 2 oz (0.034 mm) thick copper heat spreader. Following JEDEC JESD/EIA 51.1, 51.2, 51.3 test guidelines

Table 3. OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply Voltage (V_{DD} − V_{SS})	V_S	2.2	5.5	V
Specified Operating Temperature Range	T_A	−40	125	°C
Input Common Mode Voltage Range	V_{ICMR}	V_{SS}	V_{DD}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS V_S = 2.2 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	V_S = 5.5 V		±10	±65	μV
		V_S = 2.2 V		±70	±400	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			**±0.4**	**±2.4**	μV/°C
Input Bias Current (Note 6)	I_{IB}			±0.2		pA
					±600	pA
Input Offset Current (Note 6)	I_{OS}			±0.2		pA
					±600	pA
Common Mode Rejection Ratio @ Vs = 5.5 V	CMRR	V_{CM} = V_{SS} to V_{DD}	**75**	100		dB
Common Mode Rejection Ratio @ Vs = 2.2 V			**70**	90		
Input Resistance	R_{IN}	Differential		111		GΩ
		Common Mode		111		
Input Capacitance	C_{IN}	Differential		6		pF
		Common Mode		12		
OUTPUT CHARACTERISTICS						
Open Loop Voltage Gain	A_{VOL}	V_O = V_{SS} + 0.05 V to V_{DD} − 0.05 V		120		dB
Open Loop Output Impedance	Z_{OUT_OL}			See Figure 33		Ω
Output Voltage High, Referenced to Rail (Note 6)	V_{OH}	I_L = 1 mA			**30**	mV
		I_L = 10 mA			**100**	
Output Voltage Low, Referenced to Rail (Note 6)	V_{OL}	I_L = 1 mA			**30**	mV
		I_L = 10 mA			**100**	
Short Circuit Current	I_{SC}	Sinking Current		22		mA
		Sourcing Current		23		
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBWP	Load = 10 kΩ || 100 pF		10		MHz
Gain Margin	A_M	Load = 10 kΩ || 100 pF		10		dB
Phase Margin	ϕ_M	Load = 10 kΩ || 100 pF		60		°
Slew Rate	SR	Rising Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 100 pF		6		V/μs
		Falling Edge, V_S = 5.5 V A_v = 1, Load = 10 kΩ || 100 pF		4		
Settling Time	t_S	0.1 % V_o = 2 V step		2.5		μs
		0.0 1% V_o = 2 V step		6.5		μs
Turn On Time	t_{ON}			3		μs
Overload Recovery Time	t_{OR}	V_{IN} = <100 mV Step, A_V = −100		2		μs
Capacitive Load Drive	C_L	See Figure 34		1		nF
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	V_S = 5.5 V, f_{IN} = 1 kHz, AV = 1, V_{out} = 2 V_{pp}, R_L = 10 kΩ		0.0007		%
Voltage Noise Density	e_N	f_{IN} = 1 kHz		10		nV/√Hz

Table 4. ELECTRICAL CHARACTERISTICS V_S = 2.2 V to 5.5 V
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, $V_{CM} = V_S/2$, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = −40°C to 125°C, guaranteed by characterization and/or design.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NOISE PERFORMANCE						
Current Noise Density	i_N	f_{IN} = 1 kHz		7		fA/√Hz
Voltage Noise, Peak−to−Peak	e_{PP}	f_{IN} = 0.1 Hz to 10 Hz		1		μV_{PP}
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.2 V to 5.5 V	**77**	95		dB
Quiescent Current	I_Q	No load		1	1.2	mA
					1.3	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization.

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

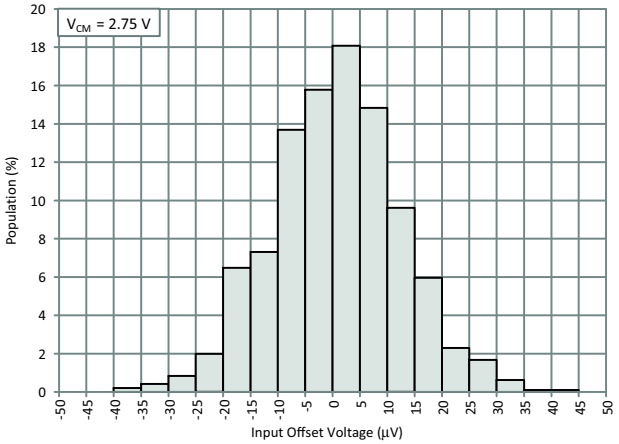


Figure 1. Input Offset Voltage Distribution
V_S = 5.5 V

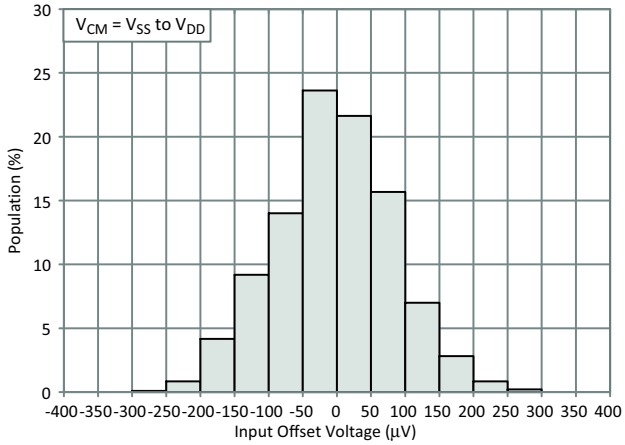


Figure 2. Input Offset Voltage Distribution vs.
V_{CM}, V_S = 2.2 V

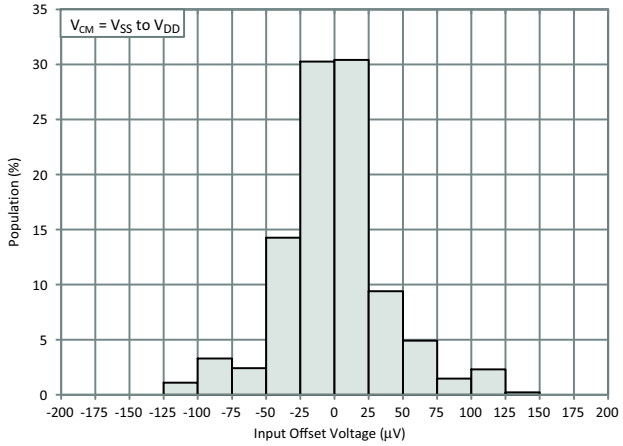


Figure 3. Input Offset Voltage Distribution vs.
V_{CM}, V_S = 5.5 V

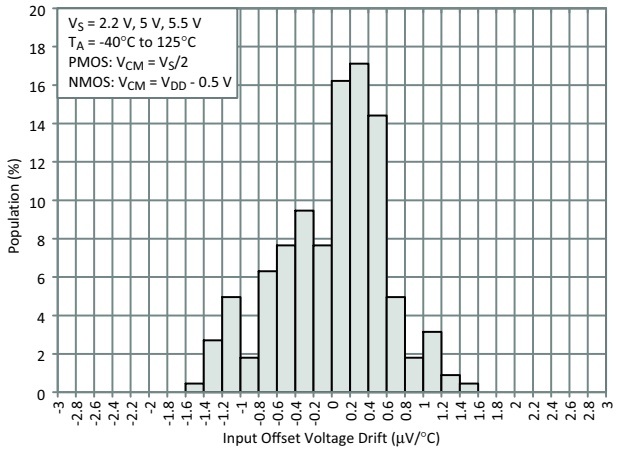


Figure 4. Input Offset Voltage vs. Temperature Distribution

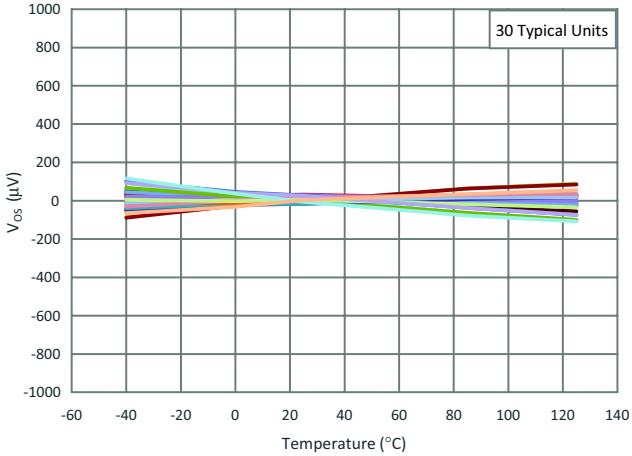


Figure 5. Input Offset Voltage vs. Temperature,
V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

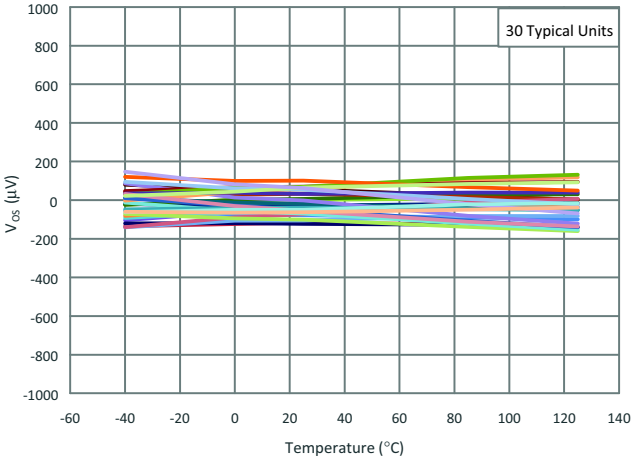


Figure 6. Input Offset Voltage vs. Temperature, V_S = 2.2 V

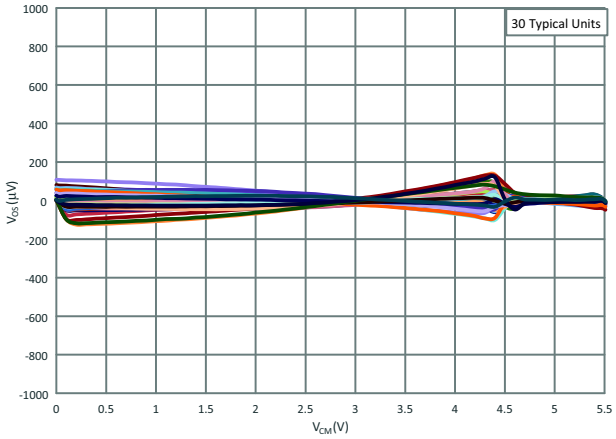


Figure 7. Input Offset Voltage vs. Input Common Mode Voltage, V_S = 5.5 V

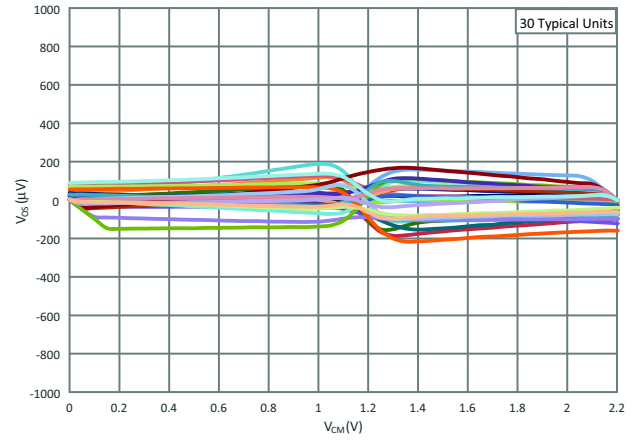


Figure 8. Input Offset Voltage vs. Input Common Mode Voltage, V_S = 2.2 V

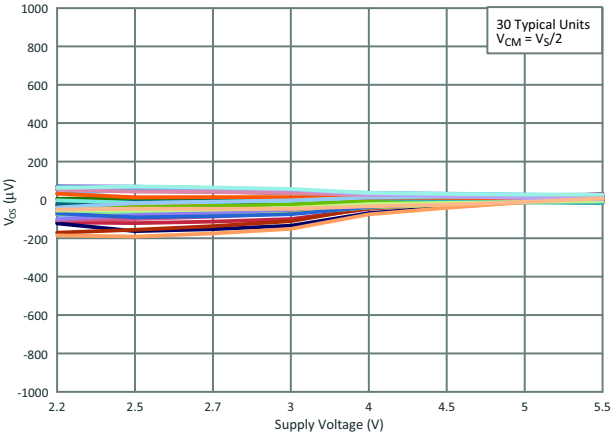


Figure 9. Input Offset Voltage vs. Supply Voltage

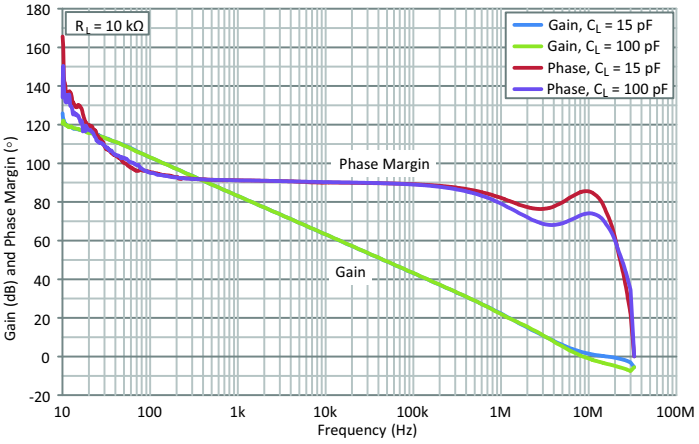


Figure 10. Open Loop Gain and Phase vs. Frequency, V_S = 5.5 V

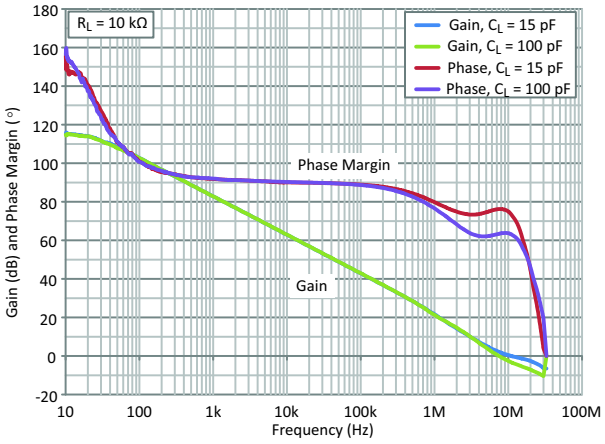


Figure 11. Open Loop Gain and Phase vs. Frequency, V_S = 2.2 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

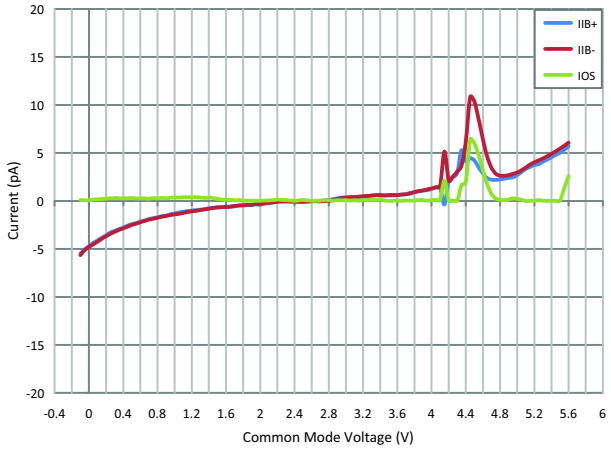


Figure 12. Input Bias Current and Input Offset Current vs. Common Mode Voltage, V_S = 5.5 V

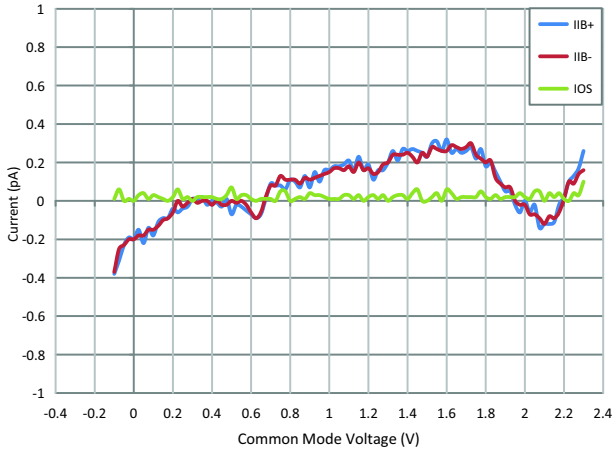


Figure 13. Input Bias Current and Input Offset Current vs. Common Mode Voltage, V_S = 2.2 V

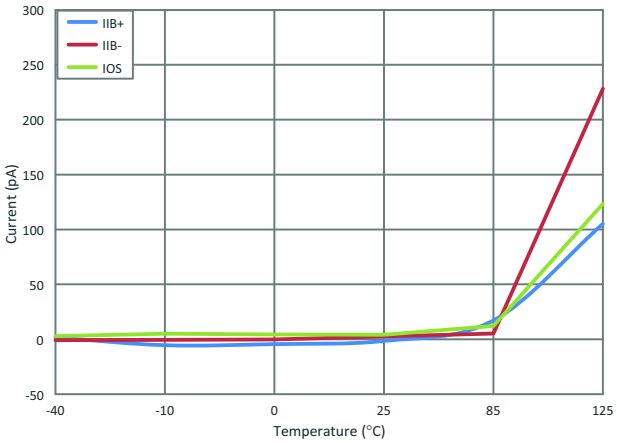


Figure 14. Input Bias Current and Input Offset Current vs. Temperature, V_S = 5.5 V

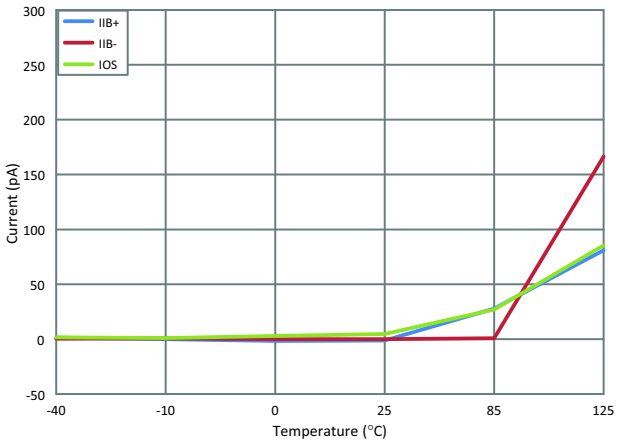


Figure 15. Input Bias Current and Input Offset Current vs. Temperature, V_S = 2.2 V

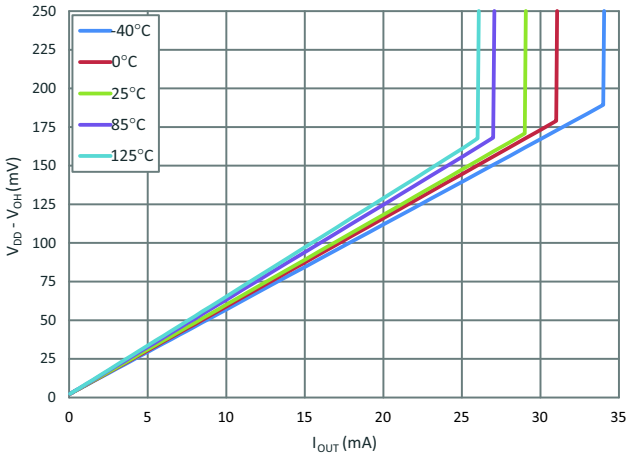


Figure 16. V_{OH} vs. Output Current vs. Temperature, V_S = 5.5 V

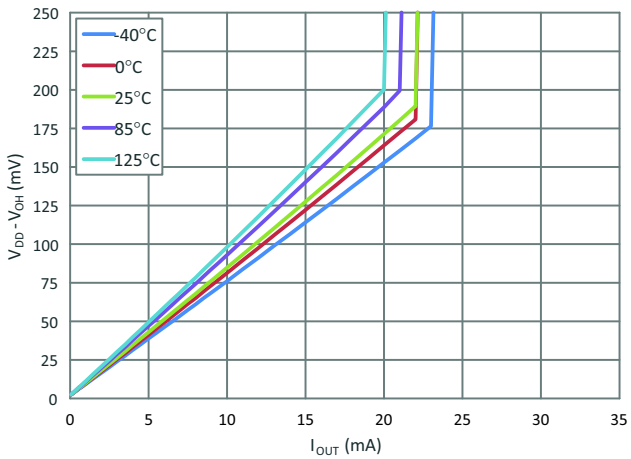


Figure 17. V_{OH} vs. Output Current vs. Temperature, V_S = 2.2 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

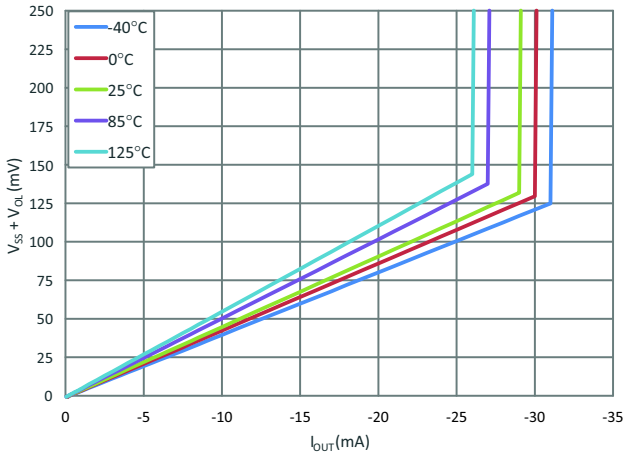


Figure 18. V_{OL} vs. Output Current vs. Temperature, V_S = 5.5 V

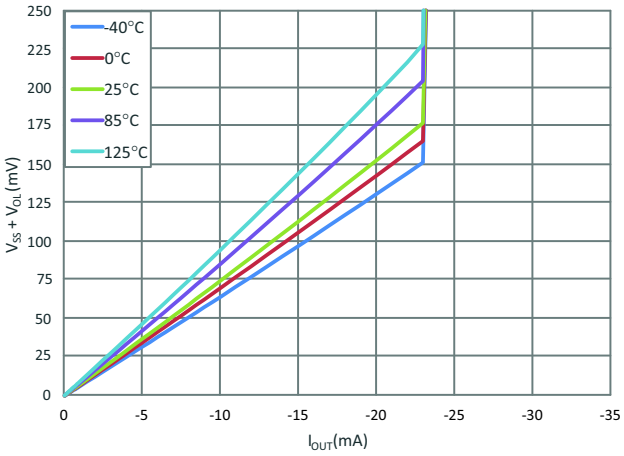


Figure 19. V_{OL} vs. Output Current vs. Temperature, V_S = 2.2 V

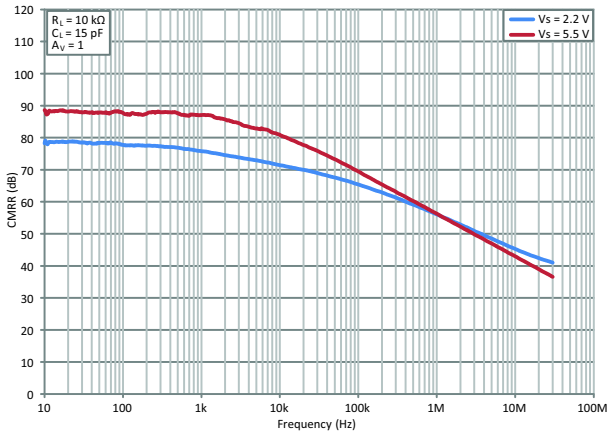


Figure 20. Common Mode Rejection Ratio vs. Frequency

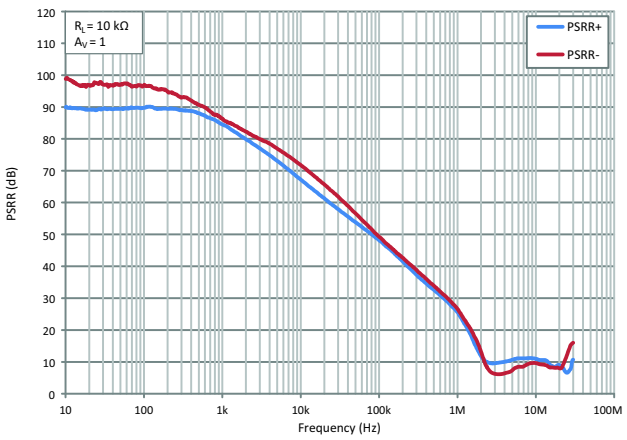


Figure 21. Power Supply Rejection Ratio vs. Frequency ; V_S = 5.5 V

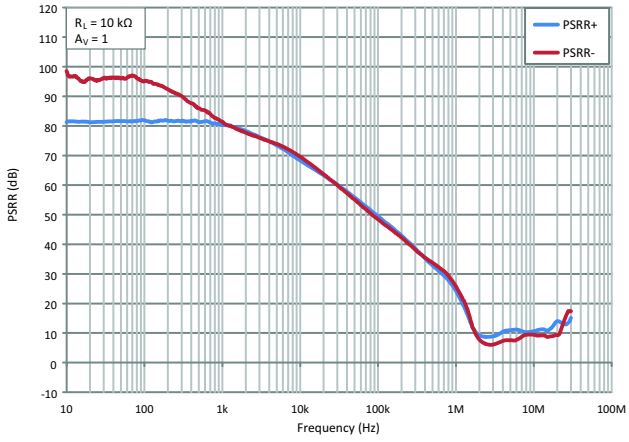


Figure 22. Power Supply Rejection Ratio vs. Frequency; V_S = 2.2 V

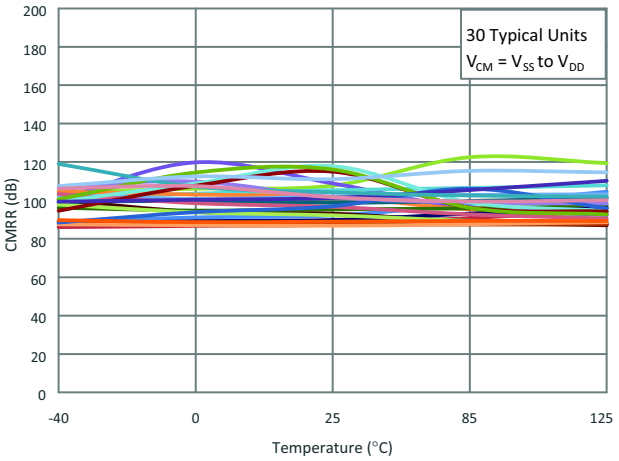


Figure 23. Common Mode Rejection Ratio vs. Temperature, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

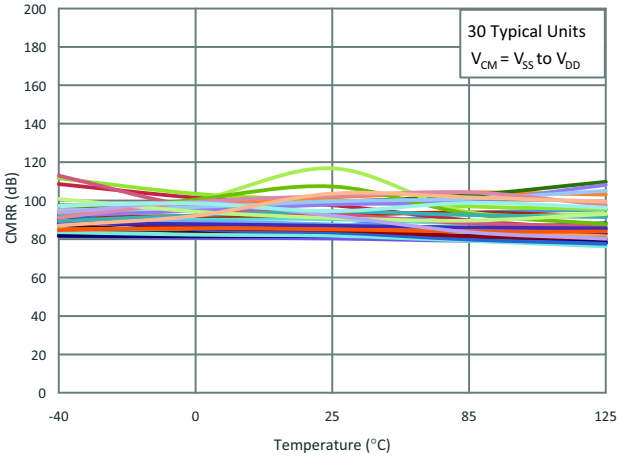


Figure 24. Common Mode Rejection Ratio vs. Temperature, V_S = 2.2 V

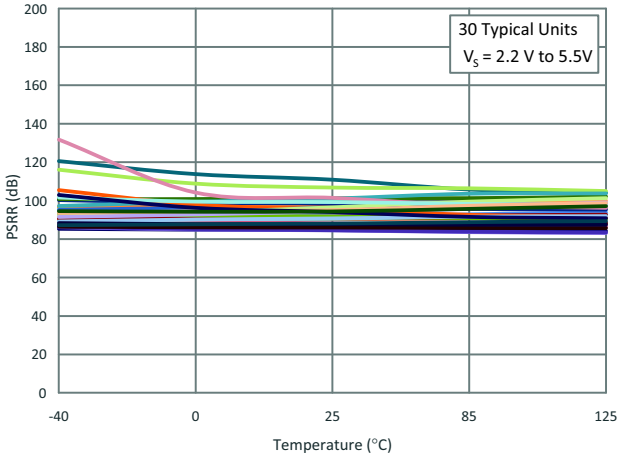


Figure 25. Power Supply Rejection Ratio vs. Temperature

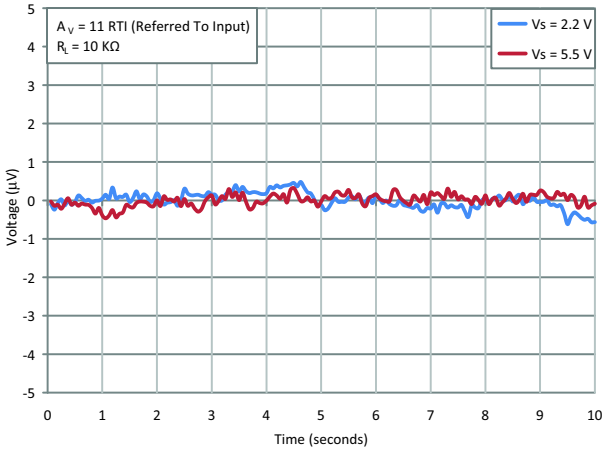


Figure 26. 0.1 Hz to 10 Hz Voltage Noise

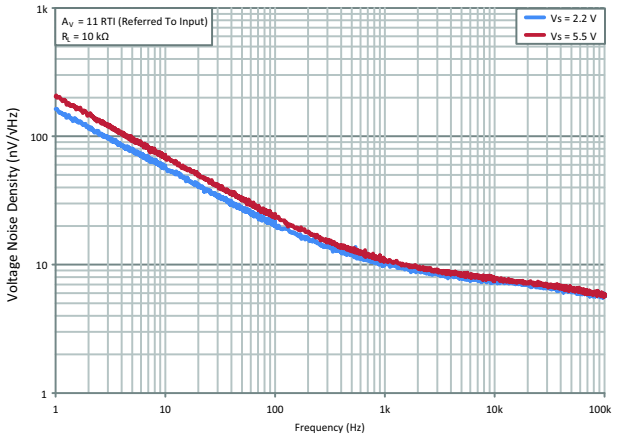


Figure 27. Voltage Noise Density vs. Frequency

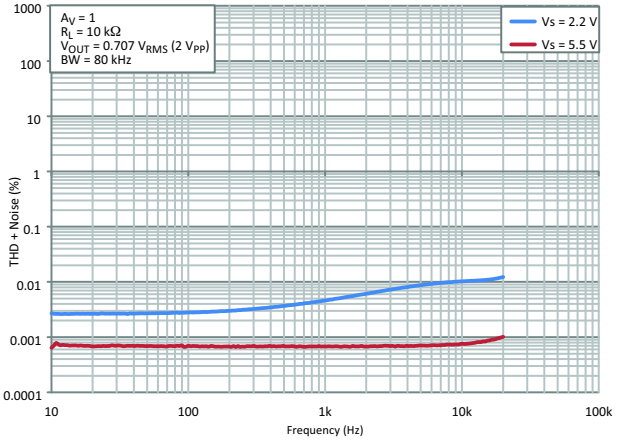


Figure 28. THD + Noise vs. Frequency

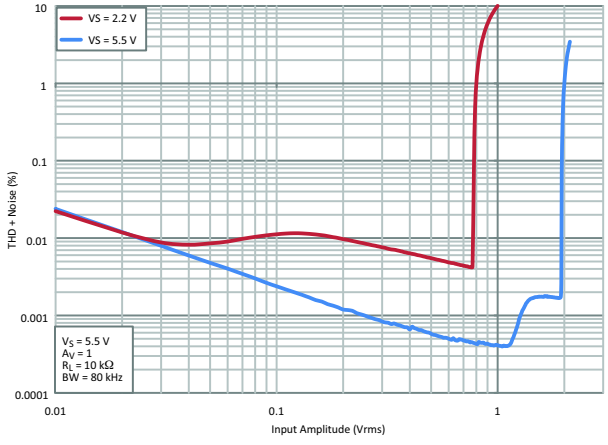


Figure 29. THD + Noise vs. Input Amplitude at 1 kHz

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

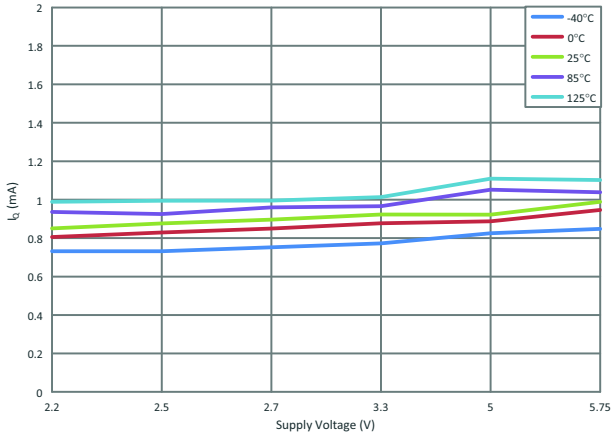


Figure 30. Quiescent Current vs. Supply Voltage

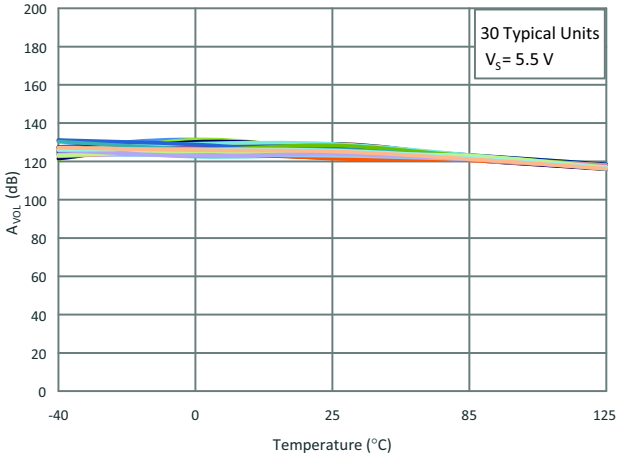


Figure 31. Open Loop Gain vs. Temperature, V_S = 5.5 V

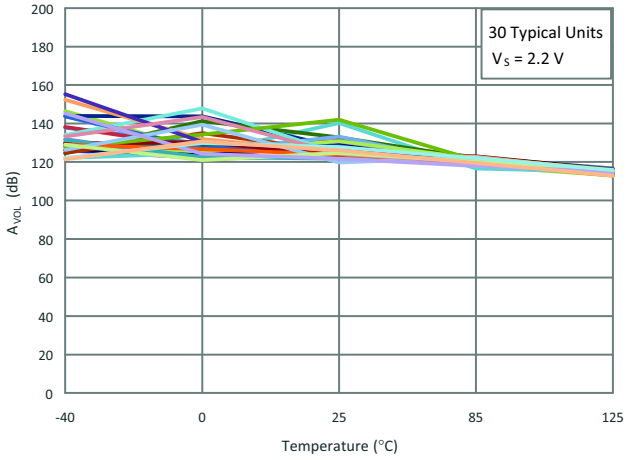


Figure 32. Open Loop Gain vs. Temperature, V_S = 2.2 V

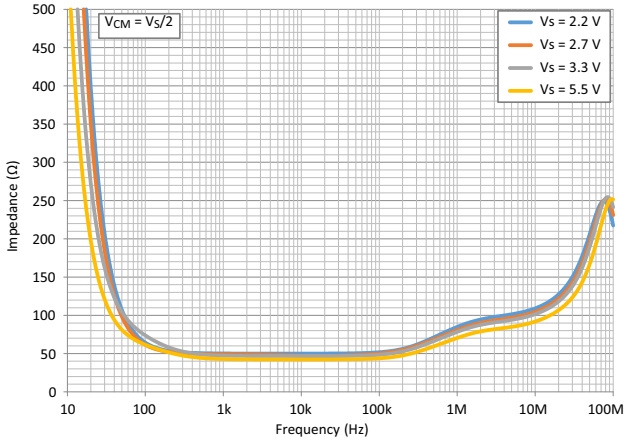


Figure 33. Open Loop Output Impedance vs. Frequency

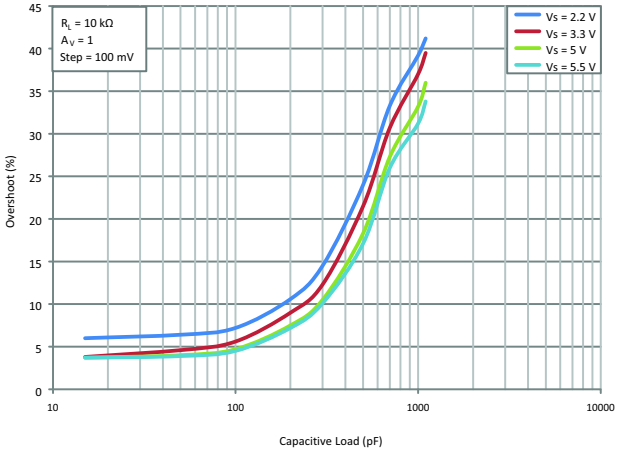


Figure 34. Small Signal Overshoot vs. Capacitive Load

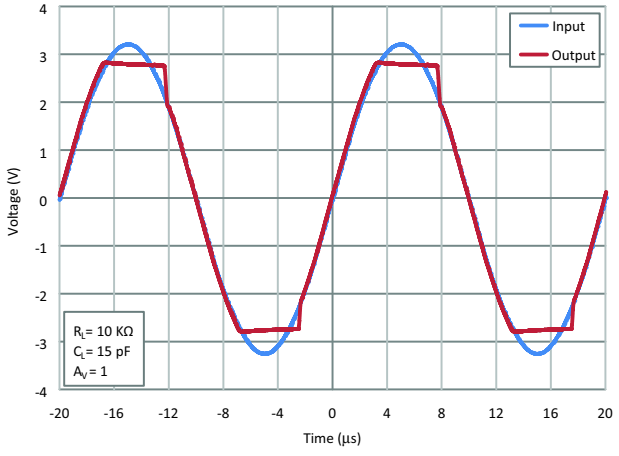


Figure 35. No Phase Reversal, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

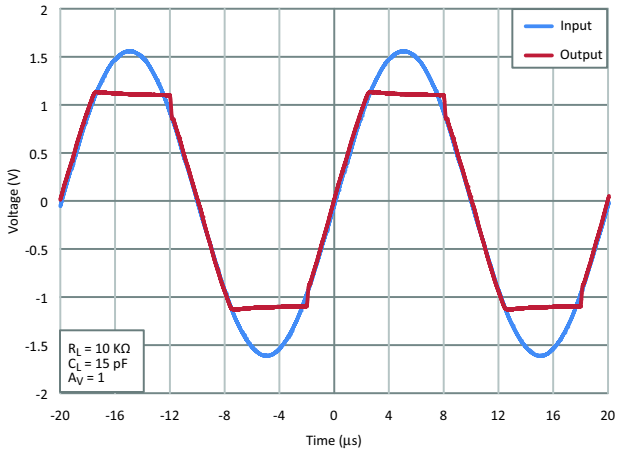


Figure 36. No Phase Reversal, V_S = 2.2 V

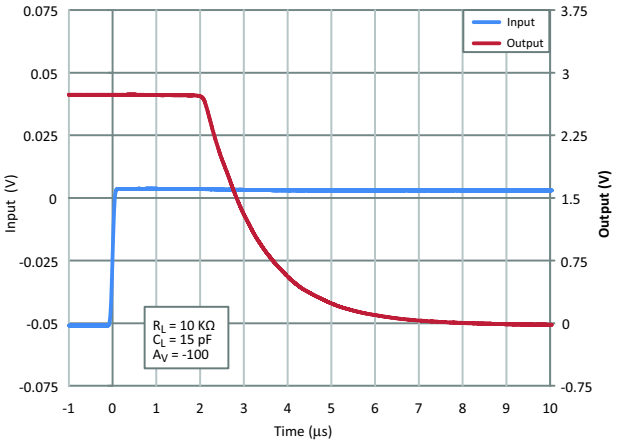


Figure 37. Positive Overload Recovery, V_S = 5.5 V

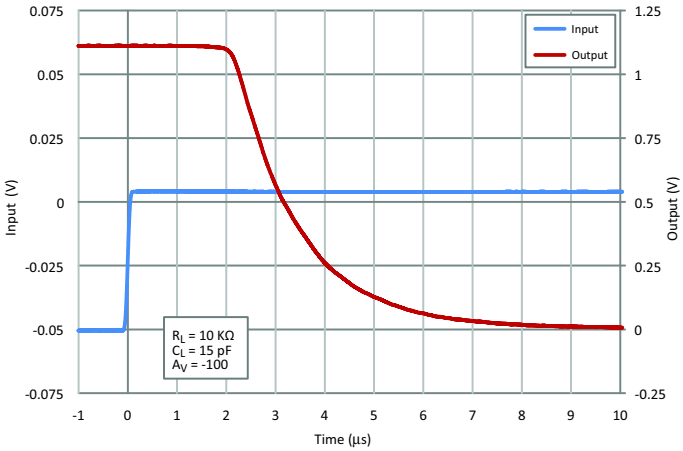


Figure 38. Positive Overload Recovery, V_S = 2.2 V

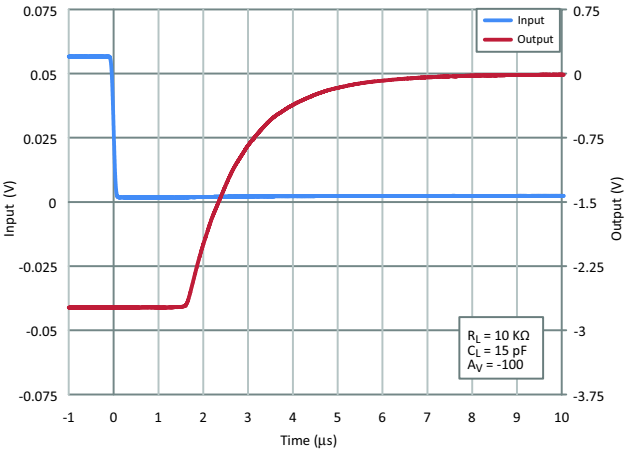


Figure 39. Negative Overload Recovery, V_S = 5.5 V

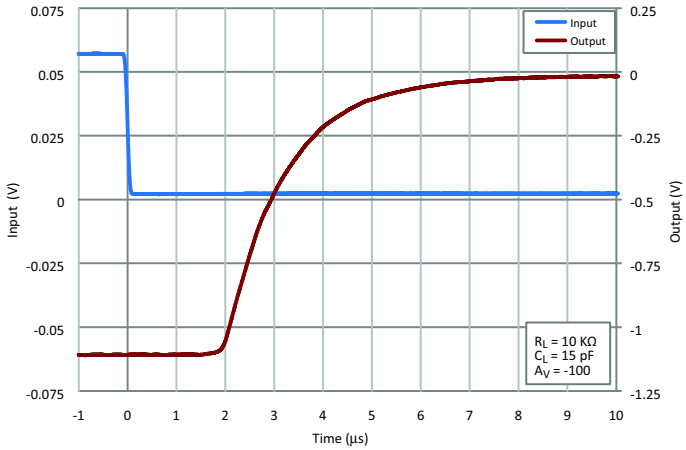


Figure 40. Negative Overload Recovery, V_S = 2.2 V

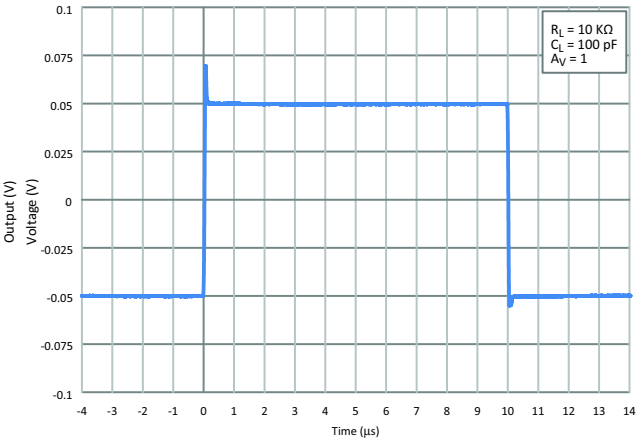


Figure 41. Small Signal Step Response, V_S = 5.5 V

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

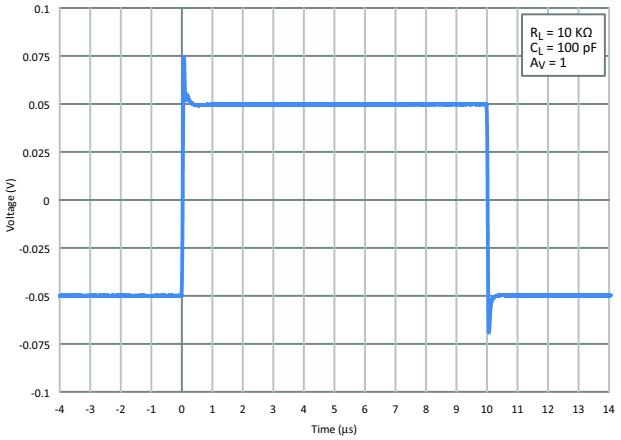


Figure 42. Small Signal Step Response, V_S = 2.2 V

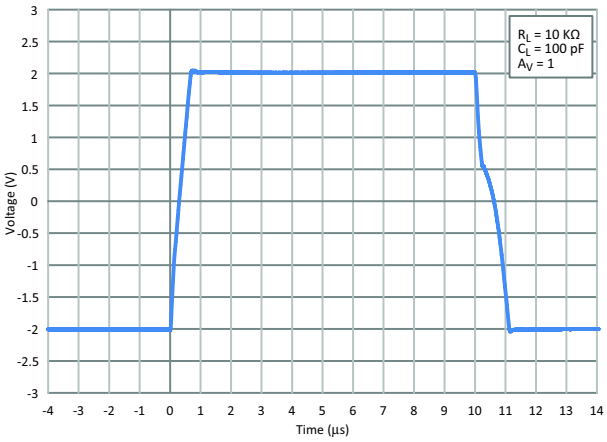


Figure 43. Large Signal Step Response, V_S = 5.5 V

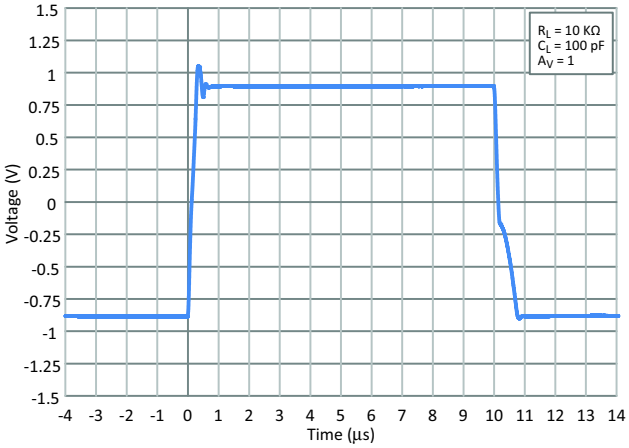


Figure 44. Large Signal Step Response, V_S = 2.2 V

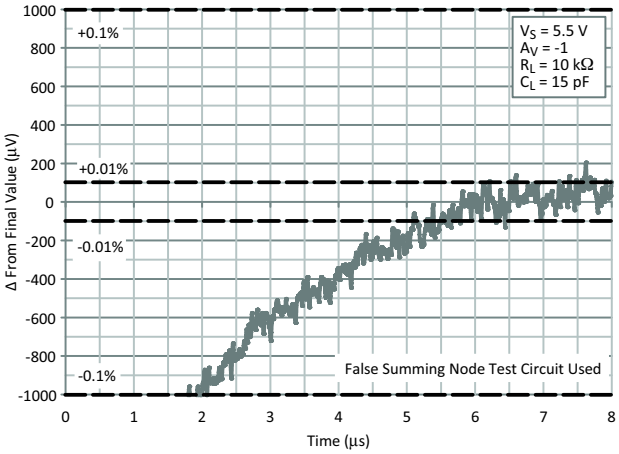


Figure 45. Large Signal Settling Time (2 V Positive Step)

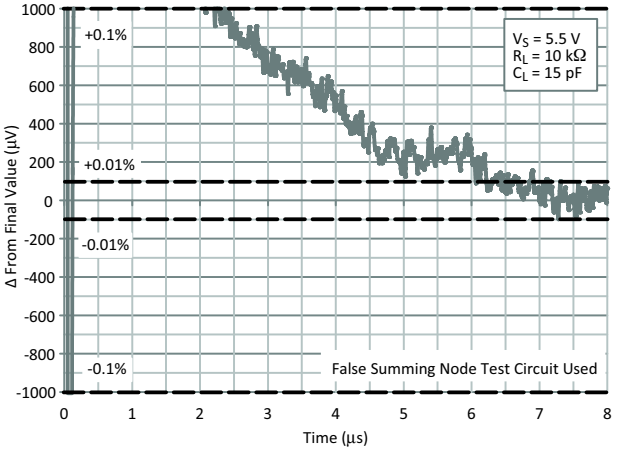


Figure 46. Large Signal Settling Time (2 V Negative Step)

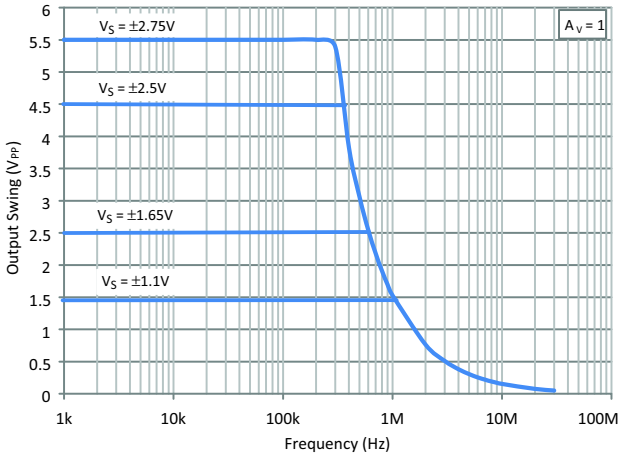


Figure 47. Full Power Bandwidth

TYPICAL CHARACTERISTICS

T_A = 25°C, V_S = 5.5 V, V_{CM} = V_S/2, unless otherwise noted.

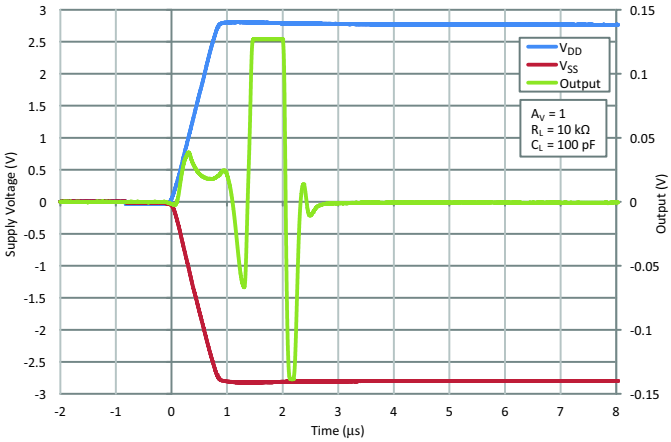


Figure 48. Turn On Time, V_S = 5.5 V

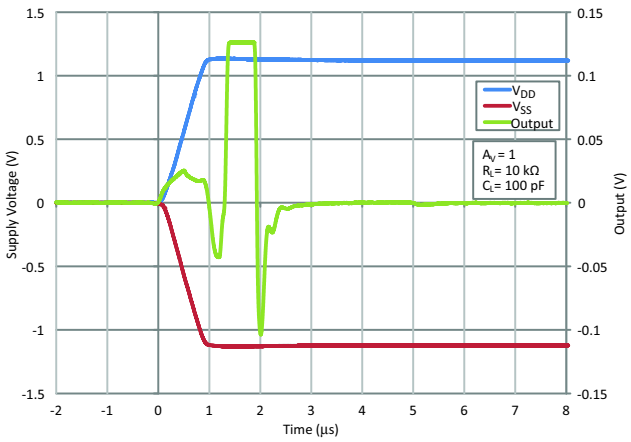


Figure 49. Turn On Time, V_S = 2.2 V

APPLICATIONS INFORMATION

APPLICATION CIRCUITS

Low−Side Current Sensing

The goal of low−side current sensing is to detect over−current conditions or as a method of feedback control. A sense resistor is placed in series with the load to ground. Typically, the value of the sense resistor is less than 100 mΩ to reduce power loss across the resistor. The op amp amplifies the voltage drop across the sense resistor with a gain set by external resistors R1, R2, R3, and R4 (where R1 = R2, R3 = R4). Precision resistors are required for high accuracy, and the gain is set to utilize the full scale of the ADC for the highest resolution.

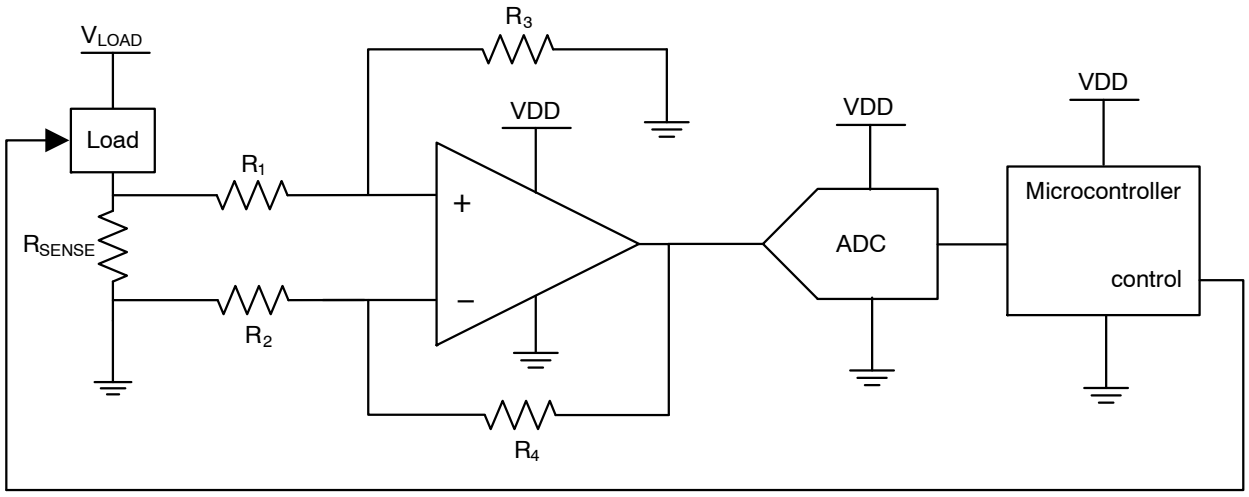


Figure 50. Low−Side Current Sensing

Differential Amplifier for Bridged Circuits

Sensors to measure strain, pressure, and temperature are often configured in a Wheatstone bridge circuit as shown in Figure 51. In the measurement, the voltage change that is produced is relatively small and needs to be amplified before going into an ADC. Precision amplifiers are recommended in these types of applications due to their high gain, low noise, and low offset voltage.

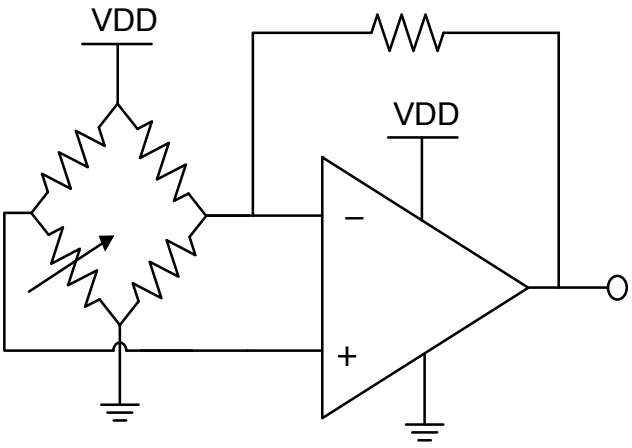


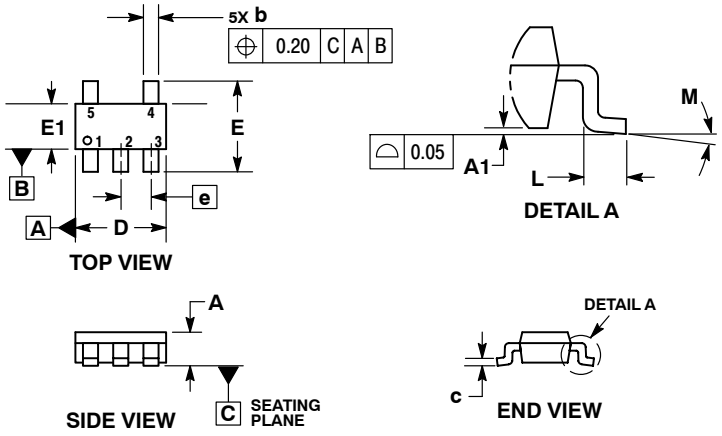
Figure 51. Bridge Circuit Amplification

GENERAL LAYOUT GUIDELINES

To ensure optimum device performance, it is important to follow good PCB design practices. Place 0.1 μF decoupling capacitors as close as possible to the supply pins. Keep traces short, utilize a ground plane, choose surface−mount components, and place components as close as possible to the device pins. These techniques will reduce susceptibility to electromagnetic interference (EMI). Thermoelectric effects can create an additional temperature dependent offset voltage at the input pins. To reduce these effects, use metals with low thermoelectric−coefficients and prevent temperature gradients from heat sources or cooling fans.

PACKAGE DIMENSIONS

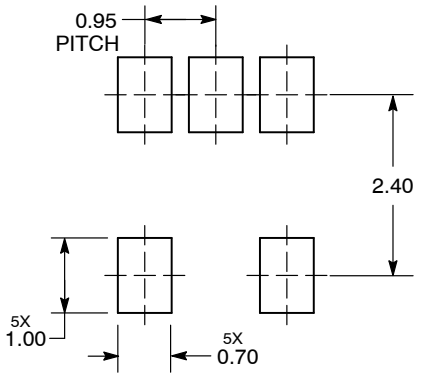
SC−74A
CASE 318BQ
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.10
A1	0.01	0.10
b	0.25	0.50
c	0.10	0.26
D	2.85	3.15
E	2.50	3.00
E1	1.35	1.65
e	0.95 BSC	
L	0.20	0.60
M	0 °	10 °

RECOMMENDED SOLDERING FOOTPRINT*

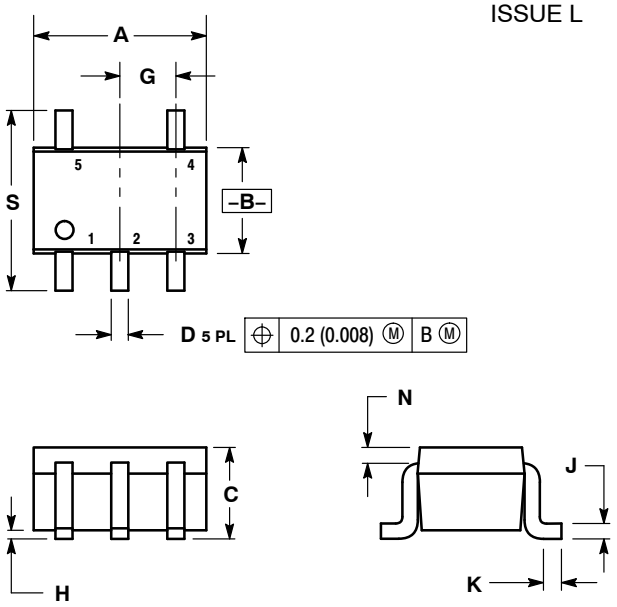


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

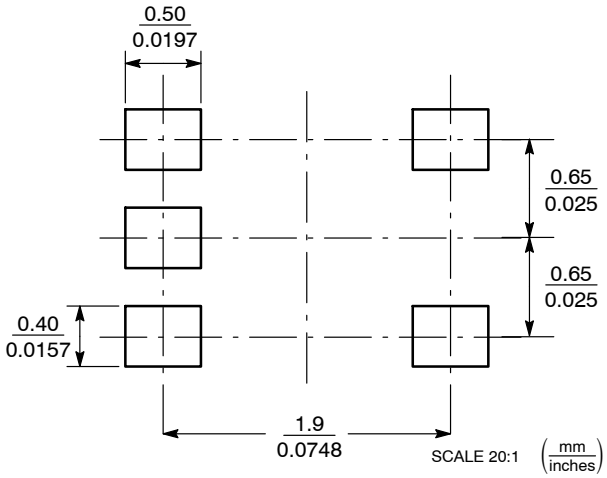
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

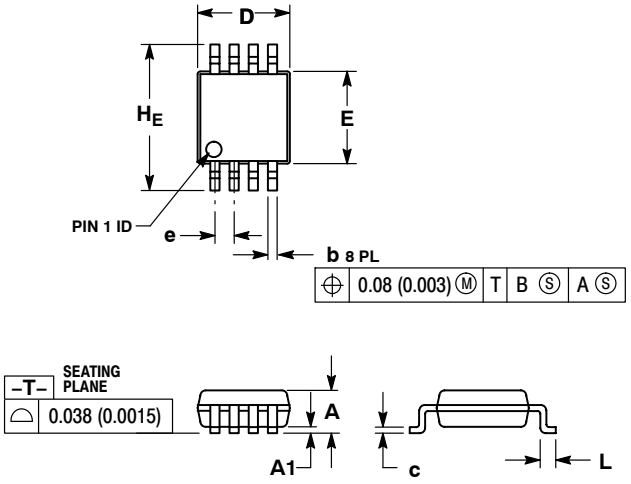
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



PACKAGE DIMENSIONS

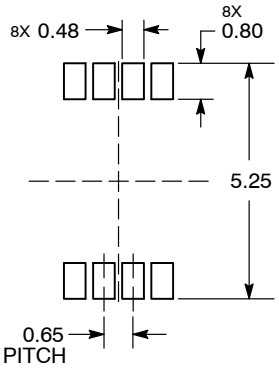
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

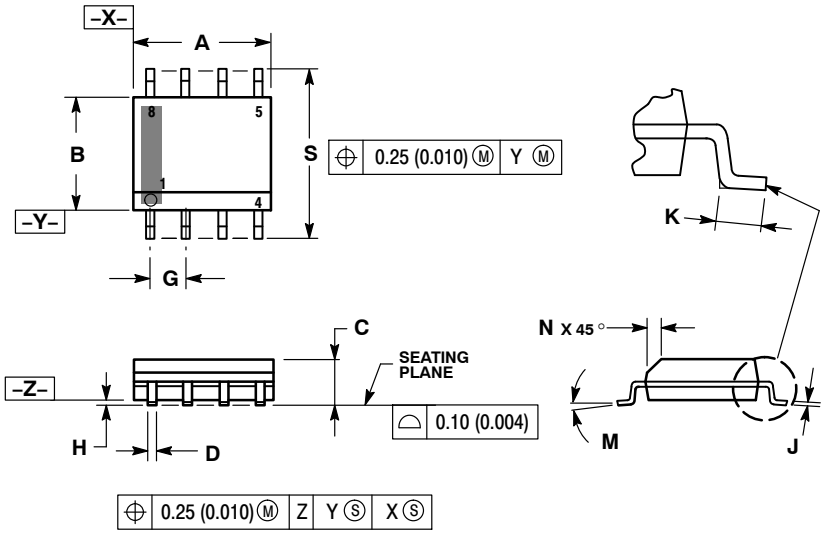


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

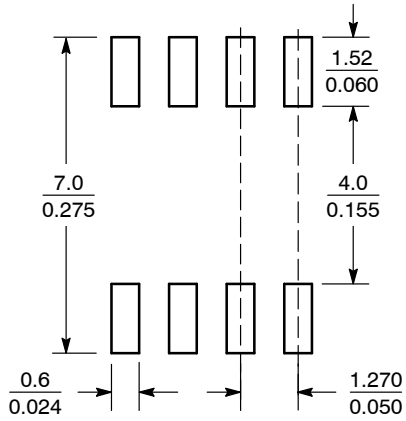
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

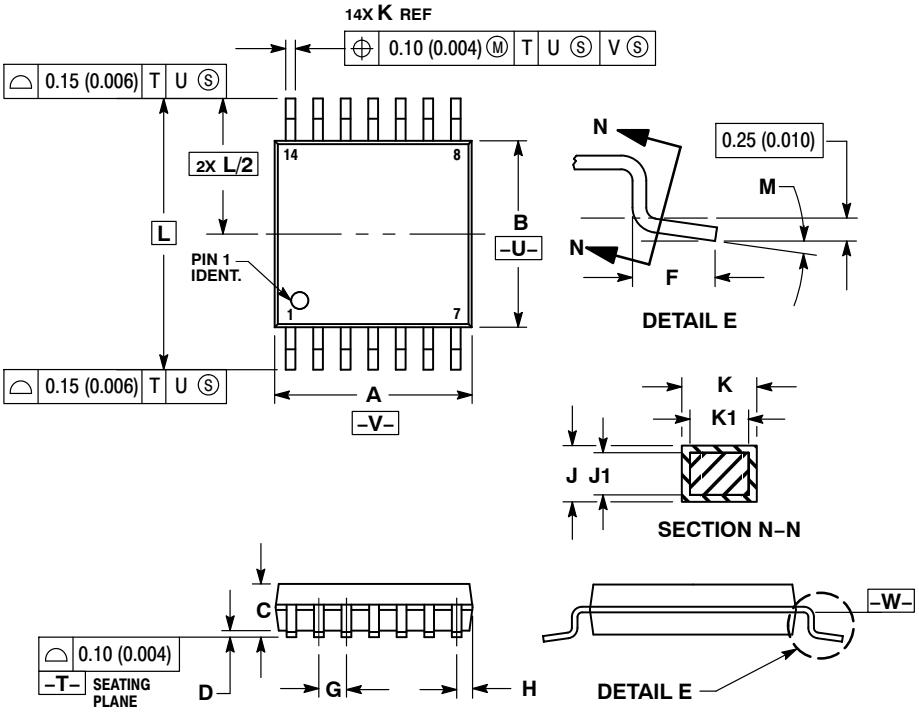


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

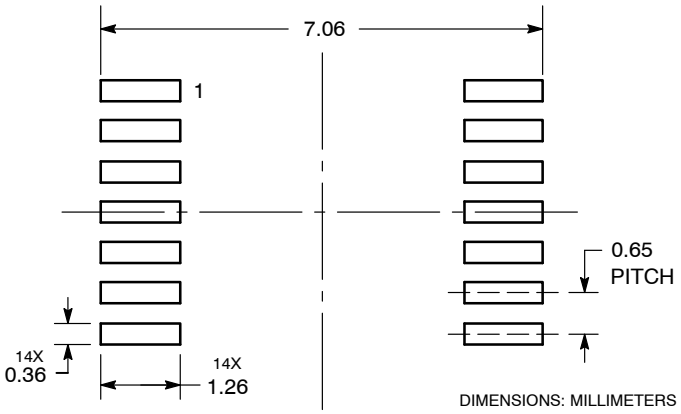
TSSOP−14 WB
CASE 948G
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

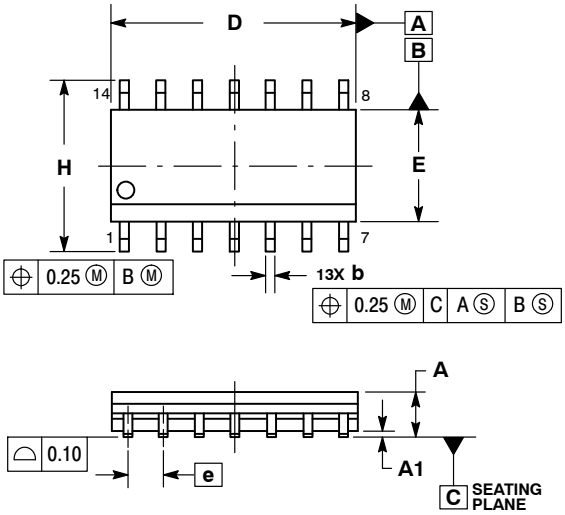
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

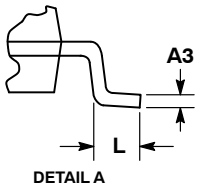
SOLDERING FOOTPRINT

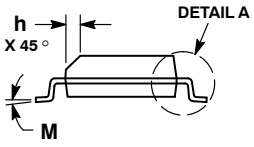


PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L



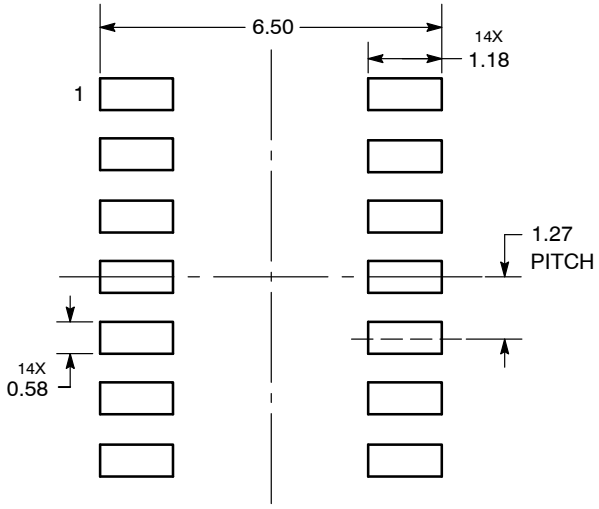




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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