NCT211A

Remote Diode Digital Temperature Sensor with Integrated Fan Control

The NCT211A is a two-wire serially programmable temperature sensor with integrated fan control. The chip monitors 2 temperature zones – the local (on-chip temperature) and the temperature of a remotely connected diode. The remote temperature value register can also be used to store temperature data pushed into it by the user. This temperature data can then be used in the fan control LUT algorithm. The NCT211A also features an ALERT output pin to signal out of limit conditions. This is an open-drain pin and can also be operated as an SMBALERT output. This is used to alert the system of out of limit conditions so that appropriate action can be taken.

An open-drain, Pulse-Width-Modulated (PWM) pin is used to control an externally connected fan. Fan speed readings can also be taken fron the tach pin. The NCT211A uses an eight point look-up table. This allows the user to program a fan speed profile based on the temperature.

Communication with the NCT211A is accomplished via the SMBus/I^2C interface which is compatible with industry standard protocols. Through this interface the NCT211As internal registers may be accessed. These registers allow the user to read the current temperature, change the configuration settings and adjust the temperature and fan limits.

The NCT211A is available in an 8 lead SOIC, MSOP and DFN packages.

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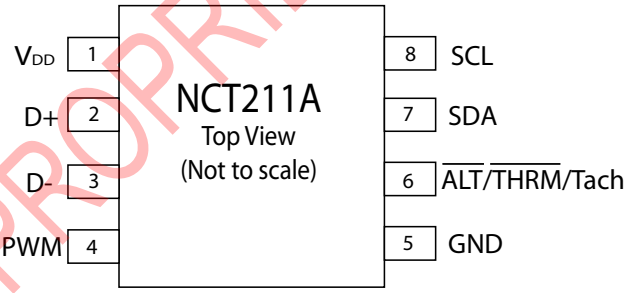
Pin Connections
(Top view)



Features

- Controls and monitors an external fan
- High and low frequency fan drive signal
- 1 on-chip and a remote temperature sensor
- Series resistance cancellation and beta compensation on the remote channel
- Extended temperature measurement range, up to 191°C
- Automatic fan speed control mode controls system cooling based on measured temperature
- Push Temperature Register
- Enhanced acoustic mode dramatically reduces user perception of changing fan speeds
- 3-wire and 4-wire fan speed measurement
- Limit comparison of all monitored values
- Meets SMBus 2.0 electrical specifications (fully SMBus 1.1 compliant)
- Fully RoHS compliant

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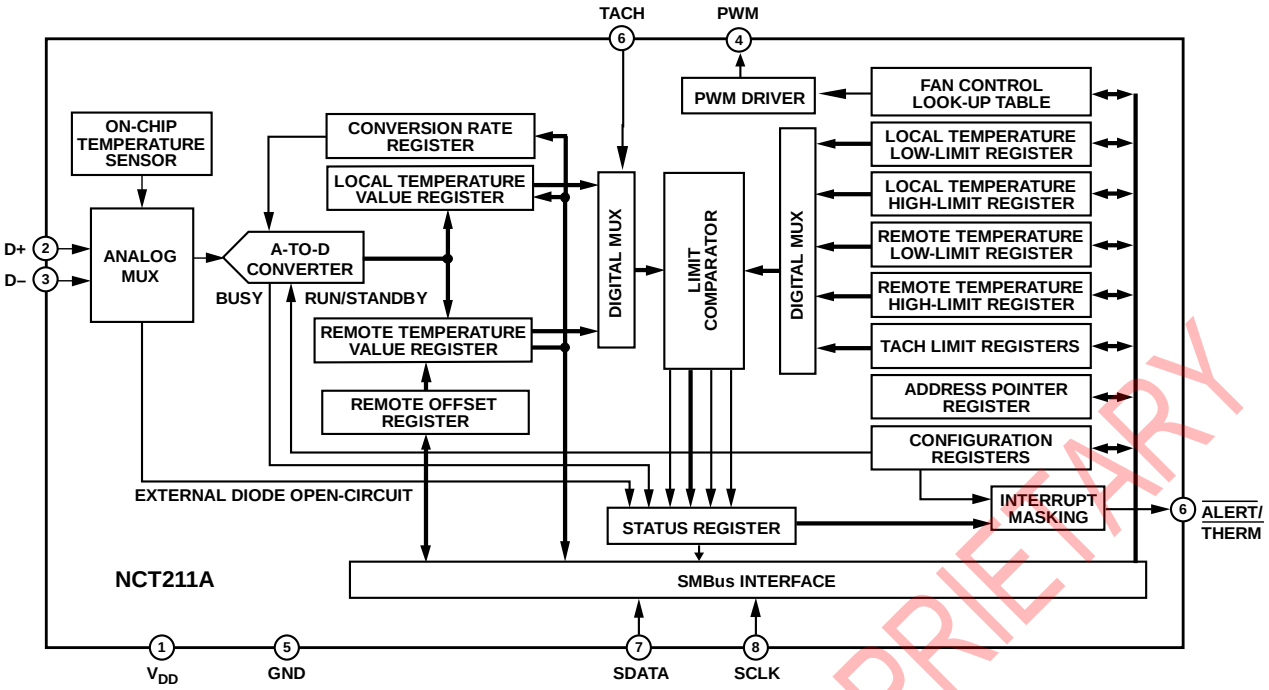

Figure 1. Functional Block Diagram of NCT211A

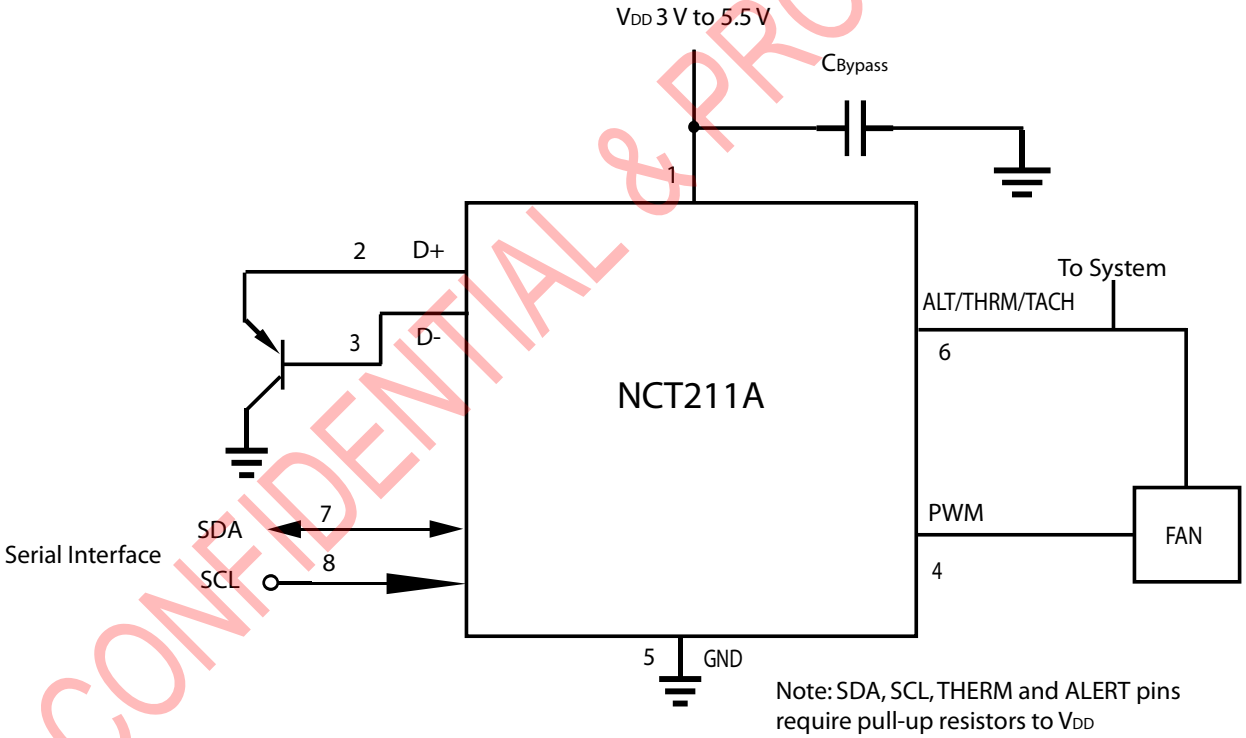

Figure 2. *Typical Application Circuit*

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{DD}	Positive Supply Voltage, 3 – 5.5 V. Bypass to ground with a **TBD**uF bypass capacitor.
2	D+	Positive Connection to Remote Temperature Sensor.
3	D-	Negative Connection to Remote Temperature Sensor.
4	PWM	Digital Output(Open Drain). Requires 10kΩ typical pull-up. Pulse-width modulated output to control the speed of Fan.
5	GND	Power Supply Ground.
6	ALT/ THRM/ TACH	ALERT: Open-Drain Logic Output Used as Interrupt or SMBus Alert. THERM: Open-Drain Output. Can be used to turn a fan on/off or throttle a CPU clock in the event of an overtemperature condition. Requires pullup resistor.TACH: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan. TACH: Digital Input (Open Drain). Fan tachometer input to measure speed of Fan.
7	SDA	SMBus/I^2C Serial Bi-directional Data Input/Output. Open-drain pin; needs a pull-up resistor.
8	SCL	Serial Clock Input. Open-drain pin; needs a pull-up resistor.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{DD})	V_{DD}	-0.3 to +5.5	V
Voltage on all pins		-0.3 to +5.5	V
Input Current at any pin	I_{IN}	±5	mA
Maximum Junction Temperature	$T_{J(max)}$	150.7	°C
Storage Temperature Range	T_{STG}	-65 to 160	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 3)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)

OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Supply Voltage	V_{CC}	3	5.5	V
Operating Ambient Temperature Range	T_A	-40	125	°C

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

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ELECTRICAL CHARACTERISTICS

$T_A = T_{MIN}$ to T_{MAX}, V_{DD} = 3 V to 5.5 V. All specifications for −40°C to +125°C, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
TEMPERATURE SENSOR AND ADC					
Remote Sensor Accuracy V_{DD} = 3 V to 5.5 V	T_D = 60°C to 110°C T_A = 25°C to 125°C			±1	°C
	T_D = 110°C to 125°C T_A = tbd			±2	°C
Local Sensor Accuracy V_{DD} = 3.0 V to 5.5 V	T_A = 0°C to +85°C			±2	°C
	T_A = 25°C to +125°C			±3	°C
Remote Sensor Source Current	High Level 1		240		µA
	Low Level 1		30		µA
	High Level 2			300	µA
	Low Level 2		37.5		µA
D- Voltage			0.7		V
ADC Resolution			10		Bits
Temperature Resolution			0.25		°C
Conversion Time	Averaging On			**TBD**	ms
	Averaging Off	**TBD**			ms
POWER REQUIREMENTS					
Supply Voltage		3		5.5	V
Supply Current	Peak current while converting and SMBus interface inactive			4.5 (@ 5.5 V)	mA
Average Current	Average current over 1 conversion cycle			**TBD**	µA
Standby Mode	Supply current in standby mode			**TBD**	µA
Power-On Reset		1.8		2.9	V
TACH MEASUREMENT					
TACH Accuracy	V_{DD} 3.0 – 3.6V			10	%
TACH Accuracy	V_{DD} 4.5 – 5.5V			10	%
Full Scale Count				65,535	
PWM OUTPUTS					
PWM Resolution				256	Steps
Frequency Accuracy				±10	%
PWM Duty Cycle		0		100	%
OPEN DRAIN DIGITAL OUTPUT (PWM1, PWM2, ALERT, THERM, SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = -8.0 mA			0.4	V
High Output Leakage Current, I_{OH}	V_{OUT} = V_{CC}		0.1	20	µA
SMBUS DIGITAL INPUTS (SDA, SCL)					
Input High Voltage V_{IH}		V_{DD}-?			V
Input Low Voltage, V_{IL}				0.5	V
Input Leakage Current	V_{IN} = 0 V to V_{DD}			**TBD**	µA
SCL, SDA Glitch Rejection	Input filtering suppresses noise spikes of less than 50 ns			50	ns
Pin Capacitance			**TBD**		pF
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage VIH		V_{DD}-?			V
Input Low Voltage, VIL				0.5	V
Input Capacitance, C_{IN}			**TBD**		pF

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SMBus SPECIFICATIONS						
Serial Clock Frequency	f_{SCLK}		10		400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
SCL Low Time	t_{LOW}		1.3			µs
SCL High Time	t_{HIGH}		0.6		50	µs
SCL, SDA Rise Time	t_r				1000	ns
SCL, SDA Fall Time	t_f				300	µs
Minimum RESET Pulse Width	t_{RESET}		1.3			µs
Start Condition Hold Time	$f_{HD; STA}$		0.6			µs
Start Condition Setup Time	$f_{SU; STA}$	90% of SCL to 90% of SDA	100			ns
Stop Condition Setup Time	$f_{SU:STO}$	90% of SCL to 10% of SDA	100			ns
Data Setup Time	$t_{SU; DAT}$	10% of SDA to 10% of SCL	100			ns
Data Hold Time	$t_{HD; DAT}$	10% of SCL to 10% of SDA	0		0.9	µs

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TYPICAL CHARACTERISTICS

Supply Current Vs. Conversion rate

Temp Error Vs. Power Supply Noise Frequency

Remote Temp Sensor Error over Temperature

Remote Temperature Error Vs. PCB Resistance, D+ to Gnd and Nominal Vdd and Temp.

Remote Temp Error Vs. D+ - D- Capacitance

Remote Temp Error Vs. CM Noise Freq. Coupled to D+ and D-

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Remote Temp Error Vs. DM Noise Freq Coupled to D+ and D-

Remote and Local Temp Error Vs. Power Supply Noise Frequency

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APPLICATION INFORMATION

LIMITS, STATUS REGISTERS AND INTERRUPTS

Limit Values
Associated with each measurement channel on the NCT211A are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out-of-limit condition and is detected by polling the device. Alternatively, SMBALERT interrupts can be generated to flag a procesor or microcontroller of out-of-limit conditions.

Temeprature Limits
Register 0x05, INT High Limit = 0x55 default
Register 0x06, INT Low Limit = 0x00 default
Register 0x22, INT THERM Limit = 0x60 default
Register 0x07, EXT1 High Limit MSB = 0x55 default
Register 0x08, EXT1 Low Limit MSB = 0x00 default
Register 0x13, EXT1 High Limit LSB = 0x55 default
Register 0x14, EXT1 Low Limit LSB = 0x00 default
Register 0x19, EXT1 THERM Limit = 0x60 default

Fan Speed Limits
Register 0x48, TACH Limit Low Byte = 0xFF default
Register 0x49, TACH Limit High Byte = 0xFF default

Out-of-limit Comparisons
All temperature measurements are done in a round-robin format. A comparison between the measured temperature and the limit programmed to the registers above is carried out. If an out-of-limit condition exists then the appropriate status bit is set. TACH measurements are not part of the round-robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High limit > comparison performed
Low limit ≤ comparison performed

Temperature limits use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This limit is needed only in manual fan control mode.

Interrupt Status Registers
The results of the limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2 (address 0x02 and 0x1A respectively). The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If the measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out of limits, the corresponding status register bit is set to 1.
The state of the various measurement channels can be polled by reading the status registers over the serial bus. Pin 8 can be configured as an SMBALERT output. This automatically notifies the system supervisor of an out−of−limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared. Interrupt mask registers (Register 0x16 and Register 0x1B) allow individual interrupt sources to be masked from causing an SMBALERT.

Interrupt Status Register 1 (0x02)
Bit 7 (ADC_BUSY) = 1, Asserts high when ADC is converting (Does not assert the ALERT o/p pin).
Bit 6 (INT) = 1, INT temp > HI_Limit or INT temp <= LO_Limit.
Bit 5 (ALERT) = 1, Asserted high if ALERT limits are exceeded.
Bit 4 (EXT1_HI) = 1, EXT1 temp > HI_Limit
Bit 3 (EXT1_LO) = 1, EXT1 temp <= LO_Limit
Bit 2 (EXT1 open/short) = 1, indicates an open or short on D1+/D1- inputs (Does not assert the ALERT o/p pin).
Bit 1 (EXT1 /THERM) = 1, Internal temp is above HI_Limit or at/below LO_Limit.
Bit 0 (Fan) = 1, TACH Limit (reg 0x48, 0x49) exceeded.

Interrupt Status Register 2 (0x1A)
Bit 7 (One_Fan_Stalled) = 1, Asserts if no rising edge seen on either tach signal for a specific time. The timeout check for the fan stalled will depend on the no. of tach periods (reg 0x31, bit [3:2]) being measured.
Bit 6 (THERM) = 1, THERM asserted.
Bit 5 Reserved
Bit 4 (INT /THERM) = 1, INT temp > THERM Limit.
Bit 3 Reserved
Bit 2 Reserved
Bit 1 Reserved
Bit 0 Reserved

ALERT/SMBALERT Interrupt Behavior
This is applicable when Pin 8 is configured as an ALERT output. The ALERT output goes low whenever an out-of-limit measurement is detected. It is an open-drain output and requires a pull-up resistor. Several ALERT outputs can be wire-OR'ed together, so that the common line goes low if one or more of the ALERT outputs goes low.
The ALERT output can be used as an interrupt signal to a processor, or as an SMBALERT. Slave devices on the SMBus cannot normally signal to the bus master that they want to talk, but the SMBALERT function allows them to do so.

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It is important to note how the SMBALERT output and status bits behave when writing interrupt handler software.

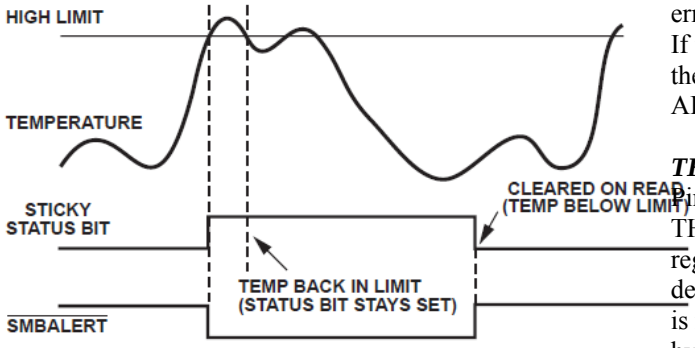

Figure 3. SMBALERT and Status Bit Behavior

Figure 3 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The interrupt status bit remains set until the error condition subsides and the interrupt status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out−of−limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low for the entire duration that a reading is out of limit and until the interrupt status register has been read. This has implications on how software handles the interrupt. Note that THERM overtemperature events are not sticky, resetting immediately after the overtemperature condition ceases.

The procedure for dealing with an SMBALERT is outlined in more detail below. When the SMBALERT line is pulled low by one of the devices, the following procedure occurs (see Figure 4):

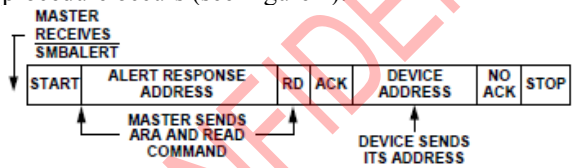

Figure 4. *Use of SMBALERT*

1. SMBALERT is pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose ALERT output is low responds to the alert response address and the master reads its device address. As the device address is seven bits, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's ALERT output is low, the one with the lowest device address takes priority, in accordance with normal SMBus arbitration.

Once the NCT211A has responded to the alert response address, it resets its ALERT output, provided that the error condition that caused the ALERT no longer exists. If the SMBALERT line remains low, the master sends the ARA again, and so on until all devices whose ALERT outputs were low have responded.

THERM Output

Pin 6 of the NCT211A can also be reconfigured as a THERM output by setting bit 7 of configuration register 2 (0x20). This pin will now operate as described below. The relevant channels THERM limit is now located in the high limit registers and the hysteresis value programmed to register 0x21 also applies to this THERM.

THERM is intended as a fail−safe interrupt output that cannot be masked. This is also an open drain output and requires a pull-up to V_{CC}. It asserts low if the external or local temperature exceeds the programmed THERM limits. THERM temperature limits should normally be equal to or greater than the high temperature limits. THERM is reset automatically when the temperature falls back within the THERM limit. The local and external 1 channels each have a programmable THERM limit and are set by default to 100°C in registers 0x22 and 0x19 respectively. A hysteresis value can be programmed; in which case, THERM resets when the temperature falls to the limit value minus the hysteresis value. This applies to all measurement channels. The power−on hysteresis default value is 10°C, but this can be reprogrammed to any value after powerup.

The hysteresis loop on the THERM outputs is useful when THERM is used, for example, as an on/off controller for a fan. The user's system can be set up so that when THERM asserts, a fan is switched on to cool the system. When THERM goes high again, the fan can be switched off. Programming a hysteresis value protects from fan jitter, where the temperature hovers around the THERM limit, and the fan is constantly switched on and off.

When THERM is asserted (the lowest of the programmed THERMs), the fan will run immediately to 100% or to the maximum PWM% programmed into the look-up table (LUT). This operation is determined by the state of bits 5 and 4 of configuration register 2 (0x20). By default, the fan will go to 100% on THERM (bit 5 is set to 1) but if bit 5 is cleared and bit 4 set then the fan will run to the maximum programmed duty cycle in the LUT.

Masking Interrupt Sources

Register 0x16, Interrupt Mask Register 1
Register 0x1B, Interrupt Mask Register 2

These registers allow individual interrupt sources to be

masked out to prevent SMBALERT interrupts. Masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

Interrupt Mask Register 1 (0x16)
Bit 7 (ADC_BUSY), This bit cannot be masked as it does not assert the ALERT output.
Bit 6 (INT) = 1, Masks the INT ALERT bit.
Bit 5 (ALERT), This bit cannot be masked.
Bit 4 (EXT1_HI) = 1, Masks EXT1_HI ALERT bit.
Bit 3 (EXT1_LO) = 1, Masks EXT1_LO ALERT bit.
Bit 2 (EXT1 open/short) = 1, This bit cannot be masked as it does not assert the ALERT output.
Bit 1 (EXT1 /THERM) = 1, Masks EXT1_THERM bit.
Bit 0 (Fan) = 1, Masks TACH ALERT bit.

Interrupt Mask Register 2 (0x1B)
Bit 7 (One_Fan_Stalled) = 1, Masks Fans_stalled bit
Bit 6 (THERM) = 1, Masks Therm output.
Bit 5 Resserved
Bit 4 (INT /THERM) = 1, Masks INT Therm.
Bit 3 Resserved
Bit 2 Resserved
Bit 1 Resserved
Bit 0 Resserved

TEMPERATURE MEASUREMENT
A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.
The technique used in the NCT211A measures the change in V_{BE} when the device operates at four different currents. Previous devices used only three operating currents, but it is the use of a fourth current that allows compensation for beta variation of the external temperature sensor.
Figure X shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it can equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded but is linked to the base.
To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. The amount this is biased by can be changed to a lower value of ~0.2V instead of ~0.7V by setting bit 6 to 1. C1 may be added as a noise filter (a recommended maximum value of **TBD** pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section. See the Layout Considerations section for more information on C1.
To measure ΔV_{BE}, the operating current through the sensor is switched among 4 currents, 2 x 2 related currents. As shown in Figure X, N1 x I_1 is a multiple of I_1 and N2 x I_2 is a multiple of I_2. The currents through the temperature diode are switched between I and N1 x I, giving ΔV_{BE1}; and then between I and N2 x I, giving ΔV_{BE2}. The temperature is then calculated using the two ΔV_{BE} measurements. This method cancels the effect of any series resistance on the temperature measurement and can also compensate for varying beta.

SERIES RESISTANCE CANCELLATION
Parasitic resistance to the D+ and D− inputs to the NCT211A, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5 degree C offset per ohm of parasitic resistance in series with the remote diode.
The NCT211A automatically cancels the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The NCT211A is designed to automatically cancel typically up to 100 Ω of resistance in series with each thermal diode input. By using an advanced temperature measurement method, this process is transparent to the user. This feature permits resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the section on Noise Filtering for more details.

BETA COMPENSATION
The NCT211A also offers Beta compensation. Beta variations in small geometry (<45 nm processes) can be cancelled by programming a beta value into registers 0x1D, 0x1E and 0x1F for the remote temp channel. This significantly reduces the large temperature errors caused by beta variation.

TEMPERATURE MEASUREMENT RESULTS
The results of the local and remote 1 temperature measurements are stored in the local and remote 1 temperature value registers in two's complement format. These results are then compared with limits programmed into the local and remote 1 high and low limit registers. The high and low limits for the local and remote 1 channels are also 2's complement format.
All the temperature measurement data for each channel is stored in two registers, one for the MSB and one for the LSB. This gives the temperature measurement resolution of 0.25°C. When reading the full external temperature value, read the LSB first. This causes the MSB to be locked (that is, the ADC does not write to it) until it is read. This feature ensures that the results read back from the two registers come from the same measurement.

Theoretically, the temperature sensor and ADC can measure temperatures from −64°C to +127.5°C with a resolution of +0.25°C. However, this exceeds the operating temperature range of the device, so local temperature measurements outside the NCT211A operating temperature range are not possible.

Table 1. Two's Complement Temperature Data Format

Temperature	Digital Output (10-Bit)
-64°C	1100 0000 **00**
-55°C	1100 1001 **00**
-40°C	1101 1000 **00**
-10°C	1111 0110 **00**
-1°C	1111 1111 **00**
-0.25°C	1111 1111 **11**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25°C	0001 1001 **00**
125°C	0111 1101 **00**
127.5°C	0111 1111 **10**
Diode Fault – 127.75	0111 1111 **11**

Note: Bold numbers denote the LSB bits from register 0x72 (internal temp), 0x10 (remote 1 temp) and 0x24 (remote 2 temp). They are stored in bits 7 and 6.

PUSH TEMPERATURE REGISTER

The remote temperature value register can also be used to store temperature data pushed into it by the user. This temperature data can then be used in the fan control LUT algorithm.

Offset Registers

Offset errors can be introduced into the temperature measurements by clock noise or when the thermal diode is located away from the hot spot. To achieve the specified accuracy on this channel, these offsets must be removed.

The offset value is stored as an 8−bit, twos complement value in register 0x71 (local temp offset) and register 0x11 (external 1 temp offset). The value in the offset register is added to, or subtracted from, the measured value of the relevant temperature. The offset register powers up with a default value of 0°C and has no effect unless the user writes a different value to it.

Turn off Averaging

For each temperature measurement read from a value register, 16 readings have been made internally and averaged before being placed in the value register. When value conversions are needed, setting bit 4 of register 0x04 turns off averaging. This effectively gives a reading 16 times faster but the reading may be noisier.

Fault Queue

The value written to this register determines how many out−of−limit measurements must occur before an ALERT is generated. The default value is that one out−of−limit measurement generates an ALERT. The maximum value that can be chosen is 4. The purpose of this register is to allow the user to perform some filtering of the output. This is particularly useful at the faster conversion rates, where no averaging takes place. The number of faults can be changed in configuration register 1 (0x03) bits 1 and 0.

ONE-SHOT MODE

One of the features of the NCT211A is a One-Shot Temperature Measurement Mode. This mode is useful if reduced power consumption is a design requirement. The NCT211A must be in standby mode for this function to operate. To do this you must set bit 6 of Config register 1 (0x03) to 1. This puts the NCT211A immediately into standby mode where the current consumption is reduced to a typical value of **TBD** µA. Writing to the one-shot register (0x0F) initiates a one-shot temperature measurement. This powers up the NCT211A, carries out a temperature measurement on each channel, updates the relevant measurement registers, compares the measured temperature with the relevant limit registers and asserts an ALERT or THERM if appropriate and then powers down again. The data written to this register is irrelevant and is not stored. It is the write operation that causes the one-shot conversion.

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FAN CONTROL

The NCT211A can be used to drive both 3 and 4-wire fans from its dedicated PWM pin. This is an open-drain output and therefore requires a pull-up resistor to V_{DD}. The PWM pin uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (on/off ratio) of a square wave applied to the fan to vary the fan speed.
The NCT211A controls the fan speed by using either manual mode or automatic mode (also known as look-up table mode).

Manual Mode

To put the part in manual mode the user needs to set bit 6 of register 0x4A to 1. Once under manual control, the PWM output duty cycle can be manually changed my writing to register 0x4C.

Alternate Mode

Another mode is available where the user can push a temperature into the remote temperature register and this value will be used in the LUT to control the fan.

Automatic Mode - Look-up Table

The NCT211A allows the user to program a temperature to fan speed profile for the fan. There are 16 registers in the fan look-up table, eight for temperature and eight for target PWM% drive. In total, there are eight available points.
There are two options when programming the look−up table. The NCT211A can be programmed to make the fan speed run at discrete speeds and jump to the new fan speed once the temperature threshold is crossed. Or, it can linearly ramp the PWM% between the two temperature thresholds.

By default, the NCT211A operates in discrete mode (bit 3 of register 0x73 = 0 i.e. once a temperature threshold is crossed the PWM% jumps to the next corresponding drive %. **Error! Reference source not found.** shows what the LUT looks like when all 8 points are programmed in discrete mode. At temperature T1, the fan runs at PWM % 1. As the temperature increases, the fan drive % will not increase until the temperature crosses the next programmed temperature in the LUT. At this point the PWM% jumps to the corresponding value. Then, if the measured temperature starts to decrease it must drop to a point below any lower threshold minus the programmed hysteresis value before it will run the fan at the corresponding PWM% drive. This hysteresis is in place at each of the temperature points on the LUT. The hysteresis value is 4°C by default and can be modified in register 0x4F.

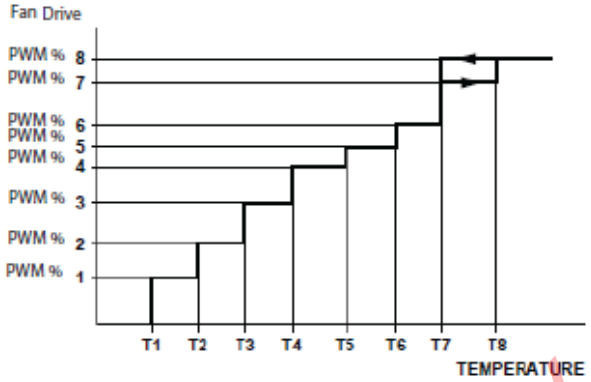

Figure 5. *Programming the Look-up Table in Discrete Fan Drive Mode*

When bit 3 of register 0x73 is set to 1 the look-up table operates in a linear manner i.e. once a temperature threshold is crossed the PWM% linearly ramps to the new drive % rather than jumping directly to it. This helps keep the acoustic noise to a minimum as the fan is not suddenly changing speed.

Figure 6 shows what the LUT looks like when all 8 points are programmed in linear mode. At temperature T1, the fan runs at PWM % 1. As the temperature increases, the fan drive % increases until it reaches PWM % 2 at T2 and so on. Then, if the measured temperature starts to decrease it linearly ramps down towards the next lowest PWM% value. The hysteresis seen in discrete mode above does not apply to linear mode as it would cause sudden changes in fan speed and thus null out the acoustic advantage of using linear mode.

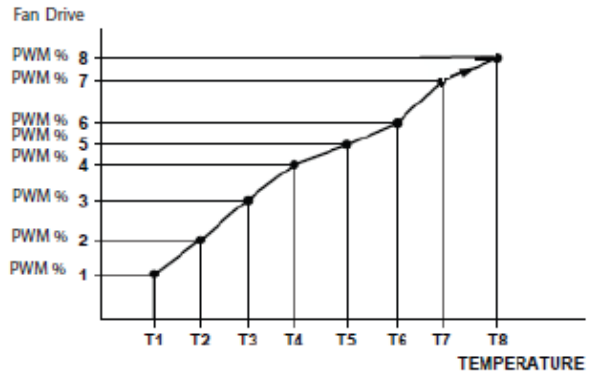

Figure 6. *Programming the Look-up Table in Linear Fan Drive Mode*

By default the NCT211A powers up in LUT mode but the data points are all programmed with their maximum values so the connected fan will not run until the LUT is programmed. The user cannot program the LUT to operate in a manner that does not help system cooling i.e. programming the fan PWM% to be lower than a previous point in the table is not allowed. If this occurs

the NCT211A will go to the next highest PWM% and use that instead.
Also, the LUT will not operate unless it is populated with non-zero values i.e. if you program the first few points with normal values and program the rest of the points to be zero, the LUT will not work and so the fan will not operate.
If the user does not communicate with the NCT211A within ~7 seconds the fans will automatically be ramped to 100% as a safety feature.

In both LUT mode and manual mode a THERM event will override the current fan settings and drive the fan at 100% duty cycle until the temperature drops below the THERM limit – hysteresis.

FAN SPEED MEASUREMENT
The NCT211A also has a shared fan speed measurement inputs (TACH).

The fan speed information is then stored in the fan speed registers. The fan tachometer readings are 16-bit values stored in two 8 bit registers.
Register 0x46, TACH Low Byte = 0x00 default
Register 0x47, TACH High Byte = 0x00 default

Each measurement involves a 2-register read; the low byte should be read first. This causes the high byte to be frozen until until both high and low byte registers have been read, preventing erroneous TACH readings. A 16-bit fan tachometer reading of 0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

The TACH channel has an associated TACH limit. These limits are also 16-bits wide and can be programmed to the following registers:
Register 0x48, TACH Limit Low Byte = 0xFF default
Register 0x49, TACH Limit High Byte = 0xFF default
If the measured fan speed falls below the programmed limit by 1 then the appropriate status bit is set and can be used to generate an SMBALERT.

PWM Logic State
The PWM output can be programmed high for a 100% duty cycle (non-inverted) or low for a 100% duty cycle (inverted). This is done in the fan configuration registers.

Fan1 Configuration Register 1 (0x4B)
Bit 4 POLARITY
0 = Logic high for 100% PWM duty cycle
1 = Logic low for 100% PWM duty cycle

PWM Frequency
The NCT211A can drive the fan in both high and low frequency mode. This is configurable for the connected fan. By default, low frequency mode is enabled (23.43 Hz). By adjusting bits 7 to 5 of register 0x75 the low frequency value can be varied in the range 5.86 Hz up to 750 Hz.
When using 4-wire fans high frequency mode can be enabled by setting bit 4 of the above register to 1. This changes the output drive frequency to 22.5 kHz.

Pulse Stretching
When driving a fan in low frequency mode the TACH information is chopped by the PWM drive signal, since power is not always applied to the fan. The TACH information can be retrieved using a technique called pulse stretching—switching the fan on long enough to gather the tach information (with a possible increase of audible noise). This can be enabled and disabled in register 0x74. By default it is enabled. When the drive signal is changed to high frequency mode this mode is disabled automatically as it is no longer needed.

Fan Spin-Up
Fans have different spin−up characteristics and take different times to overcome inertia. The NCT211A runs the fan just fast enough to overcome inertia and is quieter on spin−up than a fan programmed for a given spin−up time.
This spin-up function can be configured in two ways:

- It spins the fan at 100% duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. This mode can be enabled by setting bit 5 of register 0x4B.
- The other option is to set the fan to run at 100% duty cycle for a set time irrespective of what the TACH is doing. This is done by adjusting bits 2 to 0 of register 0x4B. The spin up times range from ~88 µs up to 5.8 seconds.

By default, the first option (spin up based on TACH pulses received) is enabled. To disable spin ups both bit 5 and bits 2 to 0 have to be cleared to 0.

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SERIAL BUS INTERFACE

Control of the NCT211A is carried out using the serial system management bus (SMBus). The NCT211A is connected to the bus as a slave device, under the control of a master controller.It has a 7-bit serial bus address. The address is by default 0x4C but if more than one part is needed on the same system then there is another part with an address of 0x4D. This allows the user to avoid conflicts with other devices sharing the same SMBus address, for example, if more than one NCT211A is used in a system.

The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishinga start condition, defined as a high−to−low transition on SDATA, the serial data line, while SCLK, the serial clock line, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7−bit address (MSB first) plus an R/W bit, which determines the direction of the data transfer, that is, whether data is written to, or read from, the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, the master writes to the slave device. If the R/W bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in a sequence of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low−to−high transition when the clock is high can be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master takes the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition. Any number of bytes of data are transferable over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. For the NCT211A, write operations contain either one or two bytes, while read operations contain one byte.

To write data to one of the device data registers, or to read data from it, the address pointer register must be set so that the correct data register is addressed. The first byte of a write operation always contains a valid address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.
This procedure is illustrated in Figure 7. The device address is sent over the bus followed by R/W set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

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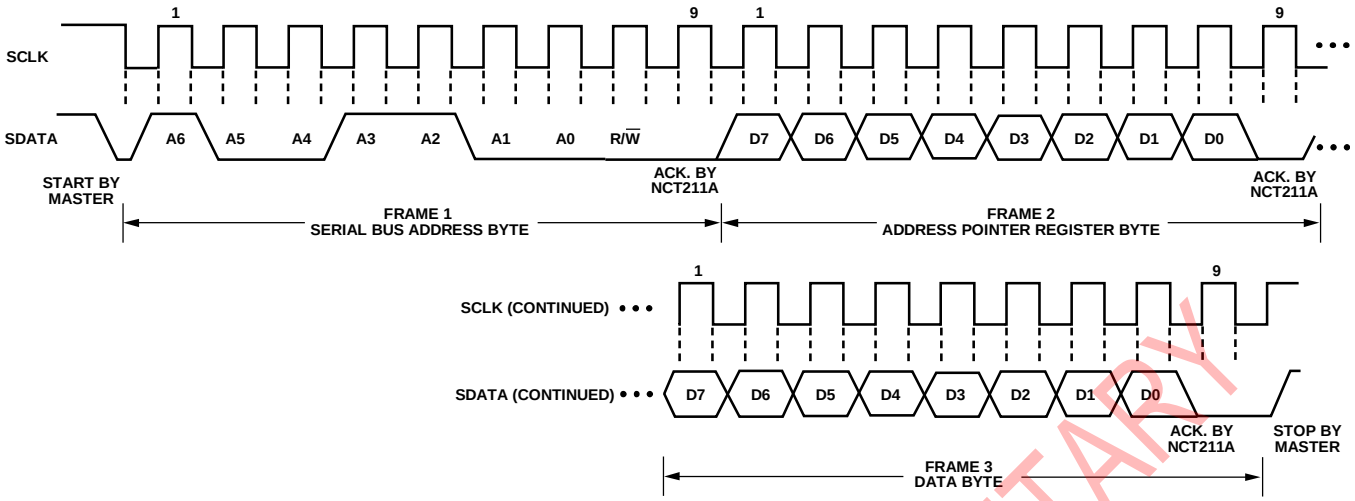

Figure 7. *Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register*

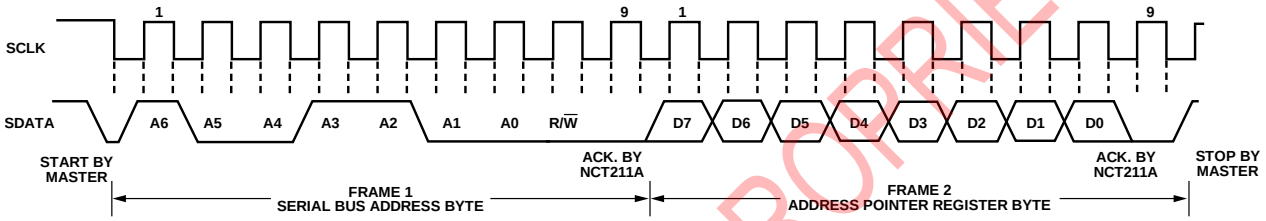

Figure 8. *Writing to the Address Pointer Register Only*

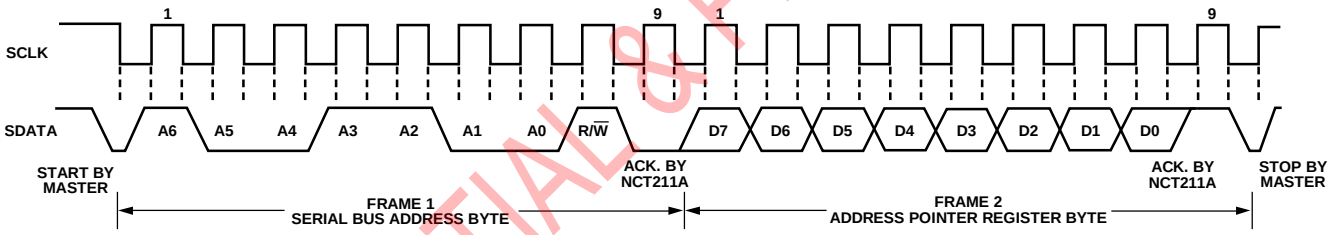

Figure 9. *Reading from a Previously Selected Register*

When reading data from a register there are two possibilities.

- If the address pointer register value of the NCT211A is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by writing to the NCT211A as before, but only the data byte containing the register read address is sent, because data is not to be written to the register see Figure 8. A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte read from the data register see Figure 9.
- If the address pointer register is known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register and the bus transaction shown in Figure 8can be omitted.

Notes:

- It is possible to read a data byte from a data register without first writing to the address pointer register. However, if the address pointer register is already at the correct value, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.
- Some of the registers have different addresses for read and write operations. The write address of a register must be written to the address pointer if data is to be written to that register, but it may not be possible to read data from that address. The read address of a register must be written to the address pointer before data can be read from that register.

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SMBus Timeout
The NCT211A includes an SMBus timeout feature. If there is no SMBus activity for **TBD** ms, the NCT211A assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot work with the SMBus timeout feature, so it can be disabled.
By default this feature is disabled but if the SMBus speed is quite fast then it is recommended that this feature be enabled.

Configuration Register 1 (0x03)
Bit 3 = 0; SMBus timeout enabled
Bit 3 = 1; SMBus timeout disabled (default)

LAYOUT CONSIDERATIONS
Digital boards can be electrically noisy environments, and the NCT211A is measuring very small voltages from the remote sensor, so care must be taken to minimize noise induced at the sensor inputs. Take the following precautions:

- Place the NCT211A as close as possible to the remote sensing diode. Provided that the worst noise sources, that is, clock generators, data/address buses, and CRTs are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. To minimize inductance and reduce noise pickup, a 5 mil track width and spacing is recommended. Provide a ground plane under the tracks, if possible.

Figure 10. *Typical Alignment of signal tracks*

- Try to minimize the number of copper/solder joints that can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and at the same temperature.
- Thermocouple effects should not be a major problem as 1°C corresponds to about 200 mV, and thermocouple voltages are about 3 mV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.
- Place a 0.1 µF bypass capacitor close to the V_{DD} pin. In extremely noisy environments, place an input filter capacitor across D+ and D− close to the NCT211A. This capacitance can effect the temperature measurement, so ensure that any capacitance seen at D+ and D− is, at maximum, **TBD** pF. This maximum value includes the filter capacitance, plus any cable or stray capacitance between the pins and the sensor diode.
- If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. A total of 6 feet to 12 feet is needed. For really long distances (up to 100 feet), use a shielded twisted pair. Connect the twisted pair to D+ and D− and the shield to GND close to the NCT211A. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, the filter capacitance can be reduced or removed.

Table 2. Register Map - Register Order

Addr	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	Lockable
0x00	R	Local Temp MSB	9	8	7	6	5	4	3	2	0x00	-
0x01	R/W	Remote 1 Temp MSB	9	8	7	6	5	4	3	2	0x00	-
0x02	R	Status 1	BUSY	Local	ALT	R1_HI	R1_Lo	R1 OPEN	R1T	Fan	0x00	
0x03	R/W	Configuration Reg 1	Mask_ ALT	STBY	-	-	SMBus T/O	ALT/TACH	Queue [1]	Queue [0]	0x00	
0x04	R/W	Conversion Rate	-	-	-	AvgOff	Conv3	Conv2	Conv1	Conv0	0x08	
0x05	R/W	Local High Limit	7	6	5	4	3	2	1	0	0x55	
0x06	R/W	Local Low Limit	7	6	5	4	3	2	1	0	0x00	
0x07	R/W	Remote 1 High Limit MSB	9	8	7	6	5	4	3	2	0x55	
0x08	R/W	Remote 1 Low Limit MSB	9	8	7	6	5	4	3	2	0x00	
0x09	R/W	Configuration Reg 1	Mask_ ALT	STBY	-	-	SMBus T/O	ALT/TACH	Queue [1]	Queue [0]	0x00	
0x0A	R/W	Conversion Rate	-	-	-	AvgOff	Conv3	Conv2	Conv1	Conv0	0x08	
0x0B	R/W	Local High Limit	7	6	5	4	3	2	1	0	0x55	
0x0D	R/W	Remote 1 High Limit MSB	9	8	7	6	5	4	3	2	0x55	
0x0E	R/W	Remote 1 Low Limit MSB	9	8	7	6	5	4	3	2	0x00	
0x0F	W	One-Shot	-	-	-	-	-	-	-	-	-	-
0x10	R	Remote 1 Temp LSB	1	0	-	-	-	-	-	-	0x00	-
0x11	R/W	Remote 1 Temp Offset	7	6	5	4	3	2	1	0	0x00	
0x13	R/W	Remote 1 High Limit LSB	1	0	-	-	-	-	-	-	0x00	
0x14	R/W	Remote 1 Low Limit LSB	1	0	-	-	-	-	-	-	0x00	
0x16	R/W	ALERT Mask 1	-	Local	-	R1_HI	R1_Lo	-	R1T	Fan	0xA4	
0x19	R/W	Remote 1 THERM Limit	7	6	5	4	3	2	1	0	0x60	
0x1A	R/W	Status Reg 2	Fan Stalled	THRM	-	Local THRM	-	-	-	-	0x00	
0x1B	R/W	ALERT Mask 2	Fan Stalled	THRM	-	Local THRM	-	-	-	-	0x02	
0x1D	R/W	Remote 1 Beta Comp Reg 1	-	-	-	-	-	-	-	-	0x00	
0x1E	R/W	Remote 1 Beta Comp Reg 2	-	-	-	-	-	-	-	-	0x00	
0x1F	R/W	Remote 1 Beta Comp Reg 3	-	-	-	-	-	-	-	-	0x00	
0x20	R/W	Configuration Reg 2	En TH2	Lo D-Bias	FS on THRM	Max on THRM	Lock	Monitor	-	-	0x24	
0x21	R/W	THERM Hysteresis	-	-	-	-	TH_b3	TH_b2	TH_b1	TH_b0	0x0A	
0x22	R/W	Local Temp THERM Limit	7	6	5	4	3	2	1	0	0x60	
0x39	R	Fan Current PWM	7	6	5	4	3	2	1	0	0x00	
0x46	R	TACH Value LSB	7	6	5	4	3	2	1	0	0x00	
0x47	R	TACH Value MSB	15	14	13	12	11	10	9	8	0x00	
0x48	R/W	TACH Limit LSB	7	6	5	4	3	2	1	0	0xFF	

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0x49	R/W	TACH Limit MSB	15	14	13	12	11	10	9	8	0xFF	
0x4A	R/W	Fan Configuration 1	-	Fan1 LUT/Man	-	Fan1 INV	-	-	-	-	0x00	
0x4B	R/W	Fan Configuration 2	-	-	Spinup en	-	-	Spin time [2]	Spin time [1]	Spin time [0]	0x3C	
0x4C	R/W	Fan 1 PWM Value (Manual)	7	6	5	4	3	2	1	0	0x00	
0x4F	R/W	Fan 1 Temp Hysteresis	-	-	-	4	3	2	1	0	0x04	
0x50	R/W	Fan Lookup Temp 1	-	6	5	4	3	2	1	0	0x7F	
0x51	R/W	Fan Lookup PWM 1	7	6	5	4	3	2	1	0	0xFF	
0x52	R/W	Fan Lookup Temp 2	-	6	5	4	3	2	1	0	0x7F	
0x53	R/W	Fan Lookup PWM 2	7	6	5	4	3	2	1	0	0xFF	
0x54	R/W	Fan Lookup Temp 3	-	6	5	4	3	2	1	0	0x7F	
0x55	R/W	Fan Lookup PWM 3	7	6	5	4	3	2	1	0	0xFF	
0x56	R/W	Fan Lookup Temp 4	-	6	5	4	3	2	1	0	0x7F	
0x57	R/W	Fan Lookup PWM 4	7	6	5	4	3	2	1	0	0xFF	
0x58	R/W	Fan Lookup Temp 5	-	6	5	4	3	2	1	0	0x7F	
0x59	R/W	Fan Lookup PWM 5	7	6	5	4	3	2	1	0	0xFF	
0x5A	R/W	Fan Lookup Temp 6	-	6	5	4	3	2	1	0	0x7F	
0x5B	R/W	Fan Lookup PWM 6	7	6	5	4	3	2	1	0	0xFF	
0x5C	R/W	Fan Lookup Temp 7	-	6	5	4	3	2	1	0	0x7F	
0x5D	R/W	Fan Lookup PWM 7	7	6	5	4	3	2	1	0	0xFF	
0x5E	R/W	Fan 1 Lookup Temp 8	-	6	5	4	3	2	1	0	0x7F	
0x5F	R/W	Fan Lookup PWM 8	7	6	5	4	3	2	1	0	0xFF	
0x71	R/W	Local Temp Offset	7	6	5	4	3	2	1	0	0x00	
0x72	R	Local Temp LSB	1	0	-	-	-	-	-	-	0x00	
0x73	R/W	Fan Configuration 3	-	Fan1 FS	Fan1 Off	Fan1 PWM min	Fan1 Lin/Dis	BHVR R2	BHVR R1	BHVR Local	0x01	
0x74	R/W	Fan Configuration 4	Fan1 Acou2	Fan1 Acou1	Fan1 Acou0	Fan1 Acou En	Fan1 Tachs [1]	Fan1 Tachs [0]	Pulse Str Fan1	-	0x02	
0x75	R/W	Fan Configuration 5	Lo Freq Sel [2]	Lo Freq Sel [1]	Lo Freq Sel [0]	HF En	-	-	-	-	0x40	
0xFD	R	Product ID	-	-	-	-	-	-	1	0	0xXX	
0xFE	R	Manufacturer ID	7	6	5	4	3	2	1	0	0x1A	
0xFF	R	Die Revision ID	-	-	-	-	3	2	1	0	0x00	

Table 3. Temperature Reading Registers

Address	R/W	Description
0x00	R	Local Temperature reading (8 MSBs)[1]
0x01	R/W	Remote 1 Temperature reading (8 MSBs)[2]

[1] Extended resolution bits for local temp reading are located in register 0x72 (bits 7 and 6).
[2] Extended resolution bits for remote 1 temp reading are located in register 0x10 (bits 7 and 6).

Table 4. Status Register 1 (0x02)

Bit No.	Mnemonic	R/W	Description
[0]	Fan	R	Fan = 1 indicates that the TACH limit for Fan1 (registers 46h and 47h) has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[1]	R1T	R	R1T = 1 indicates that the remote 1 THERM limit has been exceeded.
[2]	R1 OPEN	R	R1 OPEN = 1 indicates that the remote 1 connection is open circuit or shorted out. When this is set the remote 1 temperature data will be 127.75 °C.
[3]	R1_Lo	R	R1_Lo = 1 indicates that the remote 1 temperature is less than or equal to the remote 1 low limit (R1 <= R1_lo_limit).
[4]	R1_Hi	R	R1_Hi = 1 indicates that the remote 1 temperature is greater than the remote 1 high limit (R1 > R1_hi_limit). If pin 13 is configured as a second THERM then this bit becomes a THERM2 status bit. I.e. if the THERM2 limit is exceeded then this bit will be asserted.
[5]	ALT	R	ALT = 1 indicates that one of the programmed limits has been exceeded. This bit is asserted if any one or combination of the programmed limits for the fans or temperature is exceeded.
[6]	Local	R	Local = 1 indicates that either the local high or local low limit has been exceeded. This bit does not distinguish between the two limits. It will be asserted if the local temperature is > than local high limit or <= local low limit.
[7]	BUSY	R	BUSY = 1 indicates that the ADC is currently active and performing a conversion.

Table 5. Configuration Register 1 (0x03/0x09)

Bit No.	Mnemonic	R/W	Description
[1:0]	Queue [1:0]	R/W	**[1:0]** / **#Faults before ALERT** 00 / 1 (Default) 01 / 2 10 / 3 11 / 4
[2]	ALT/TACH	R/W	Changes the configuration of the pin to be an ALERT pin.
[3]	SMBus T/O	R/W	SMBus T/O = 1 indicates that SMBus timeout check is enabled. When enabled, the SMBus times out after typically 23 ms of no activity. Default = 0.
[4]	-	R	Reserved
[5]	-	R	Reserved
[6]	STBY	R/W	STBY = 1 puts the part into low power mode. Only this standby bit and the one-shot register (0x0F) can be written to in this mode. The temperature and status registers can be read from. Default = 0.
[7]	Mask_ALT	R/W	Mask_ALT = 1 indicates that all generated alerts will be masked. If the ALERT pin is configured as a second THERM then this bit will mask any THERMs generated for that pin. Default = 0.

Table 6. Conversion Rate Register (0x04/0x0A)

Bit No.	Mnemonic	R/W	Description
[3:0]	Conv[3:0]	R/W	**Conv Bits** / **Conv/Sec** / **Averaging On/Off** 0000 / 1/16 / ON 0001 / 1/8 / ON 0010 / 1/4 / ON 0011 / 1/2 / ON 0100 / 1 / ON 0101 / 2 / OFF 0110 / 4 / OFF 0111 / 8 / OFF 1000 / 12 / OFF (default) 1001 / 13 (continuous) / OFF 1010-1111 / 13 (continuous) / OFF
[4]	AvgOff	R/W	AvgOff = 1 indicates that averaging is disabled. Note: this only works if a conversion rate that has averaging on is being used. Default = 0.
[7:5]	-	R	Reserved

Table 7. Temperature Registers

Register Address	R/W	Description	Power-On Default
0x05 (0x0B)	R/W	Local high limit register	0x55
0x06	R/W	Local low limit register	0x00
0x07 (0x0D)	R/W	Remote 1 High Limit MSB	0x55
0x08 (0x0E)	R/W	Remote 1 Low Limit LSB	0x00
0x10	R/W	Remote 1 Temp LSB	0x00
0x11	R/W	Remote 1 Temp Offset	0x00
0x13	R/W	Remote 1 High Limit LSB	0x00
0x14	R/W	Remote 1 Low Limit LSB	0x00

Table 8. Mask Register 1 (0x16)

Bit No.	Mnemonic	R/W	Description
[0]	Fan	R/W	Fan = 1 masks the fan limit exceeded ALERT.
[1]	R1T	R/W	R1T = 1 masks the remote 1 THERM
[2]	-	R	Reserved
[3]	R1_Lo	R/W	R1_Lo = 1 masks the remote 1 low ALERT
[4]	R1_Hi	R/W	R1_Hi = 1 masks the remote 1 high ALERT.
[5]	-	R	Reserved
[6]	Local	R/W	Local = 1 masks the local ALERT.
[7]	-	R	Reserved

Table 9. THERM Limit Register (Remote 1)

Register Address	R/W	Description	Power-On Default
0x19	R/W	Remote 1 THERM Limit register	0x60

Table 10. Status Register 2 (0x1A)

Bit No.	Mnemonic	R/W	Description
[0]	-	R	Reserved
[1]	-	R	Reserved
[2]	-	R	Reserved
[3]	-	R	Reserved
[4]	Local THRM	R	Local THRM = 1 indicates local THERM > THERM limit.
[5]	-	R	Reserved
[6]	THRM	R	THRM = 1 indicates that a THERM limit has been exceeded on either local, remote 1 or remote 2.
[7]	Fan Stalled	R	Fan Stalled = 1 indicates that no rising edge has been seen on the tach signal for a specific time. This bit will assert between 725ms and 1.45s if no tach readings are being received

Table 11. Mask Register 2 (0x1B)

Bit No.	Mnemonic	R/W	Description
[0]	-	R	Reserved
[1]	-	R	Reserved
[2]	-	R	Reserved
[3]	-	R	Reserved
[4]	Local THRM	R/W	Masks a Local THERM assertion.
[5]	-	R	Reserved
[6]	THRM	R/W	This bit masks any asserted THERM.
[7]	Fan Stalled	R/W	Masks the fan stalled ALERt bit.

Table 12. Remote 1 Beta Compensation Registers

Register Address	R/W	Description	Power-On Default
0x1D	R/W	Remote 1 Beta Compensation Register 1	0x00
0x1E	R/W	Remote 1 Beta Compensation Register 2	0x00
0x1F	R/W	Remote 1 Beta Compensation Register 3	0x00

Table 13. Configuration Register 2 (0x20)

Bit No.	Mnemonic	R/W	Description
[1:0]	-	R	Reserved
[2]	Monitor	R/W	Monitor = 1 enables monitoring. This is the default configuration. If set to 0 then monitoring of the temperature channels and TACH signals is stopped. When monitoring is disabled the temperature and fan speed registers hold their previous values until monitoring is enabled again.
[3]	Lock	R/W	Lock = 1 stopped the user from writing to the register map. The part must be powered down and then back up again to release the registers. A full list of the registers locked is in the general description section.
[4]	Max on THRM	R/W	Max on THRM = 1 enables failsafe cooling by setting the fan to the maximum programmed duty cycle in the LUT (look up table) when a THERM limit is tripped. Each fan will use its respective LUT maximum value. They will return to previous levels when the over temperature event has subsided.
[5]	FS on THRM	R/W	FS on THRM = 1 enables failsafe cooling by setting the fan to 100% duty when a THERM limit is tripped. They will return to previous levels when the over temperature event has subsided. This is enabled by default.
[6]	Lo D- Bias	R/W	Lo D- Bias = 1 changes the D- bias voltage from ~0.7 V to ~0.2 V. Set to 0 to return to ~0.7 V level.
[7]	En TH2	R/W	En TH2 = 1 enables a second THERM output on pin 13.

Table 14. THERM Hysteresis (0x21)

Bit No.	Mnemonic	R/W	Description
[3:0]	TH_b[3:0]	R/W	THERM hysteresis value. Temperature must drop by (THERM limit – THERM Hystersis) before the THERM output is deasserted. 1 °C – 16 °C range. Default value is 10 °C (1010b).
[7:4]	-	R	Reserved

Table 15. Local THERM Limit

Register Address	R/W	Description	Power-On Default
0x22	R/W	Local THERM Limit register	0x60

Table 16. Fan Reading and Limit Registers

Register Address	R/W	Description	Power-On Default
0x46	R	TACH 1 Value LSB	0x00
0x47	R	TACH 1 Value MSB	0x00
0x48	R/W	TACH 1 Limit LSB	0xFF
0x49	R/W	TACH 1 Limit MSB	0xFF

Table 17. Fan Configuration 1 (0x4A)

Bit No.	Mnemonic	R/W	Description
[3:0]	-	R	Reserved
[4]	Fan1 INV	R/W	Fan1 INV = 1 inverts the PWM output (i.e. 100% duty cycle would represent off when inverted). Default = 0.
[5]	-	R	Reserved
[6]	Fan1 LUT/Man	R/W	Fan1 LUT/Man = 1 puts fan 1 in manual mode. The PWM duty cycle is manually programmed into register 0x4C. Fan1 LUT/Man = 0 puts fan 1 into look up table mode. Fan speed is determined by the

			values in the LUT (registers 0x50 – 0x5F). Defalut = 0.
[7]	-	R	Reserved

Table 18. Fan Configuration 2 (0x4B)

Bit No.	Mnemonic	R/W	Description
[2:0]	Spin time [2:0]	R/W	**Spinup_sel** / **Spinup Timeout** 000 – 88.9 µs (fast spinup) 001 – 83 ms 010 – 166 ms 011 – 332 ms 100 – 664 ms 101 – 1.328 s 110 – 2.656 s 111 – 5.312 s
[4:3]	-	R	Reserved
[5]	Spinup en	R/W	
[7:6]	-	R	Reserved

Table 19. Fan Manual Register and Hysteresis

Register Address	R/W	Description	Power-On Default
0x4C	R/W	Fan PWM Value (Manual)	0x00
0x4F	R/W	Fan Temp Hysteresis	0x04

Table 20. Fan Lookup Table

Register Address	R/W	Description	Power-On Default
0x50	R/W	Fan Lookup Temp 1	0x7F
0x51	R/W	Fan Lookup PWM 1	0xFF
0x52	R/W	Fan Lookup Temp 2	0x7F
0x53	R/W	Fan Lookup PWM 2	0xFF
0x54	R/W	Fan Lookup Temp 3	0x7F
0x55	R/W	Fan Lookup PWM 3	0xFF
0x56	R/W	Fan Lookup Temp 4	0x7F
0x57	R/W	Fan Lookup PWM 4	0xFF
0x58	R/W	Fan Lookup Temp 5	0x7F
0x59	R/W	Fan Lookup PWM 5	0xFF
0x5A	R/W	Fan Lookup Temp 6	0x7F
0x5B	R/W	Fan Lookup PWM 6	0xFF
0x5C	R/W	Fan Lookup Temp 7	0x7F
0x5D	R/W	Fan Lookup PWM 7	0xFF
0x5E	R/W	Fan Lookup Temp 8	0x7F
0x5F	R/W	Fan Lookup PWM 8	0xFF

Table 21. Local Temperature Registers

Register Address	R/W	Description	Power-On Default
0x71	R/W	Local Temperature Offset	0x00
0x72	R/W	Local Temperature LSB	0x00

Table 22. Fan Configuration 3 (0x73)

Bit No.	Mnemonic	R/W	Description
[0]	BHVR Local	R/W	Local temp channel is used as a reference temperature to control Fan1 LUT.
[1]	BHVR R1	R/W	Remote 1 temp channel is used as a reference temperature to control Fan 1 LUT.
[2]	BHVR R2	R/W	Remote 2 temp channel is used as a reference temperature to control Fan 1 LUT.
[3]	Fan1 Lin/Dis	R/W	Fan1 Lin/Dis = 1 Lookup table uses linear PWM speed calculation. Hysteresis and acoustic modes are disabled in this mode. Fan1 Lin/Dis = 0 Lookup table uses discrete PWM steps. Hystersis and acoustic modes are enabled in this mode.

[4]	Fan1 PWM min	R/W	Fan1 PWM min = 1 sets the PWM to the minimum PWM in LUT if the temperature is below Tmin. Fan1 PWM min = 0 sets the PWM to 0 if the temperature is below Tmin.
[5]	Fan1 Off	R/W	Fan1 Off = 1 turns fan1 off. Default 0 (normal operation).
[6]	Fan1 FS	R/W	Fan1 FS = 1 sets fan1 to 100% duty cycle. Default 0 (normal operation).
[7]	-	R	Reserved

Table 23. Fan Configuration 4 (0x74)

Bit No.	Mnemonic	R/W	Description
[0]	-	R	Reserved
[1]	Pulse Str Fan1	R/W	Pulse Str Fan1 = 1 enables pulse stretching on PWM1 (default). Pulse Str Fan1 = 0 disables pulse stretching on PWM1.
[3:2]	Fan1 Tachs [1:0]	R/W	**[3:2] / TACH Period Measured** 00 – 1 01 – 2 10 – 3 11 – 4 Determines how many TACH periods are measured.
[4]	Fan1 Acou En	R/W	Fan1 Acou En = 1 enables acoustic settings for fan channel 1. It cannot be enabled when in linear mode. Fan1 Acou En = 0 disables acoustic settings for fan channel 1 (default).
[7:5]	Fan1 Acou [2:0]	R/W	**Fan1 Acou [2:0] / PWM Step Size** 000 – 1 (0.4%) 001 – 2 (0.8%) 010 – 3 (1.2%) 011 – 5 (2%) 100 – 8 (3.2%) 101 – 12 (4.7%) 110 – 27 (10.6%) 111 – 48 (18.9%)

Table 24. Fan Configuration 5 (0x75)

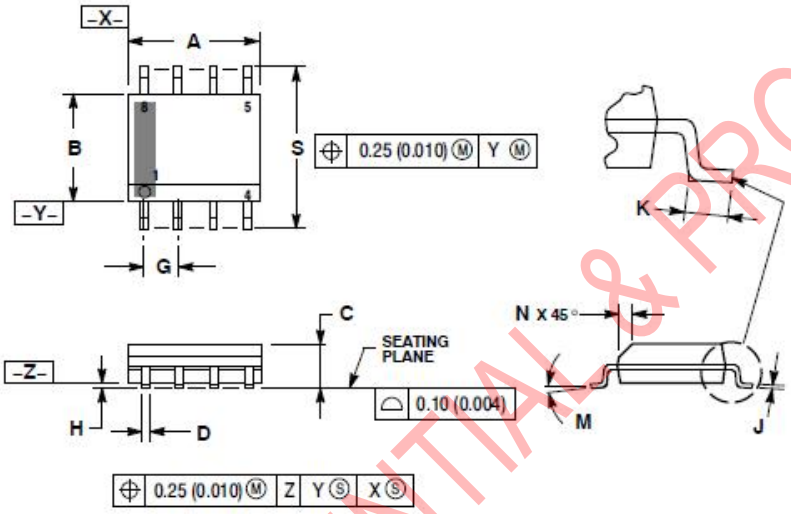
Bit No.	Mnemonic	R/W	Description
[3:0]	-	R	Reserved.
[4]	HF En	R/W	HF En = 1 enables high frequency PWM on PWM 1. HF En = 0 enables low frequency PWM on PWM 1 (default).
[7:5]	Lo Freq Sel [2:0]	R/W	**[2:0] / PWM Freq** 000 – 5.86 Hz 001 – 11.7 Hz 010 – 23.43 Hz 011 – 47.88 Hz 100 – 93.75 Hz 101 – 187.5 Hz 110 – 375 Hz 111 – 750 Hz

Figure 11. Identification Registers

Register Address	R/W	Description	Power-On Default
0xFD	R	Product ID register	0xXX
0xFE	R	Manufacturer ID	0x1A

PACKAGE DIMENSIONS

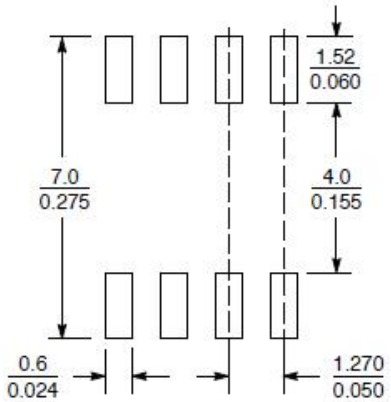
SOIC–8 NB
CASE 751–07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1962.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDARD IS 751–07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

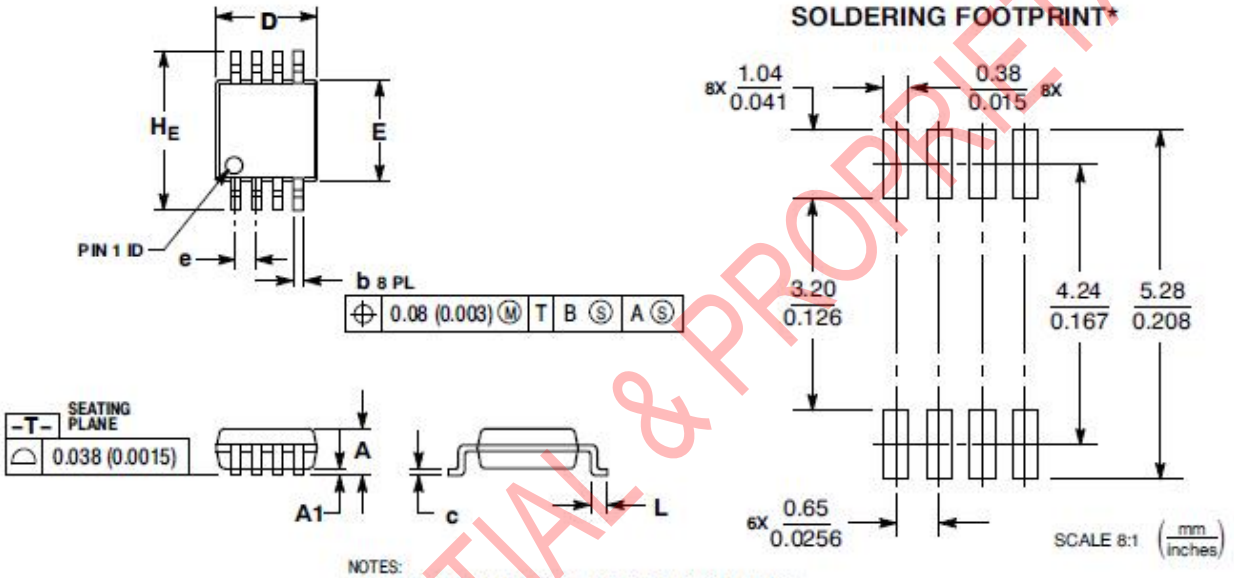
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

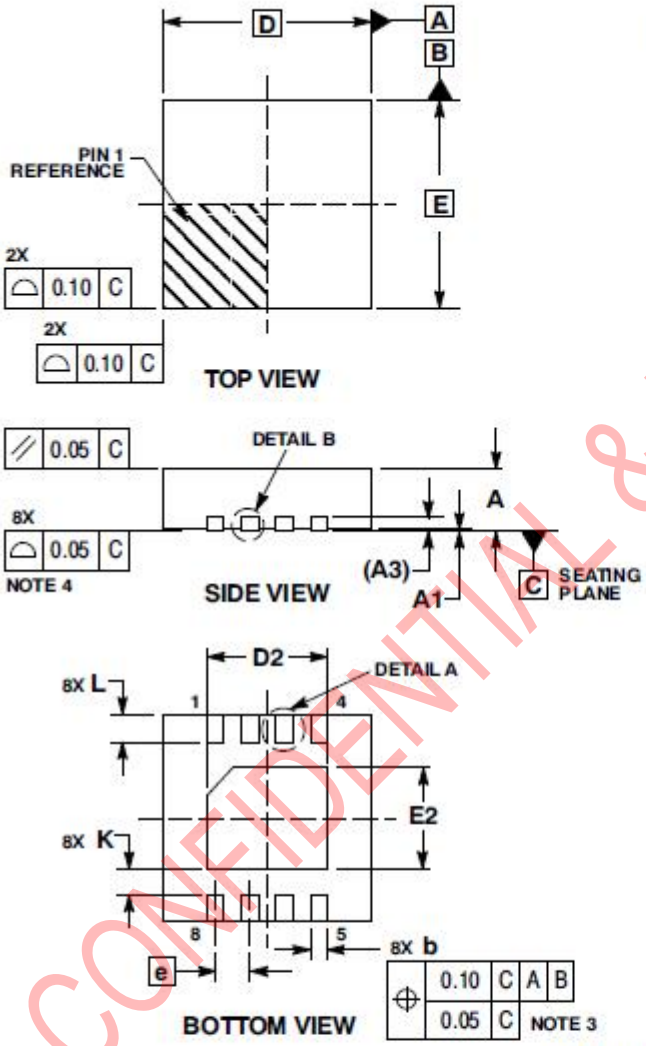
Micro8™
CASE 846A-02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

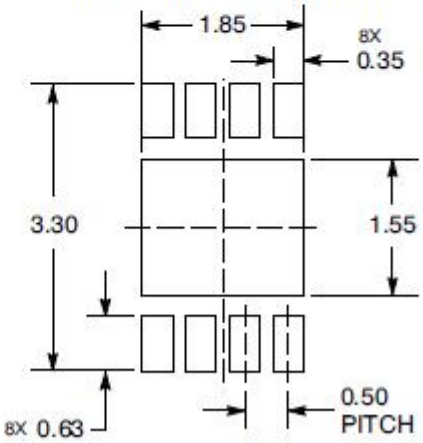
DFN8 3x3, 0.5P
CASE 506BJ-01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS