NCV4264-2

Linear Regulator - Low Dropout, Low I_Q

The NCV4264−2 is functionally and pin for pin compatible with NCV4264 with a lower quiescent current consumption. Its output stage supplies 100 mA with ±2.0% output voltage accuracy.

Maximum dropout voltage is 500 mV at 100 mA load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 3.3 V and 5.0 V Fixed Output
- ±2.0% Output Accuracy, Over Full Temperature Range
- 60 μA Maximum Quiescent Current at I_{OUT} = 100 μA
- 500 mV Maximum Dropout Voltage at 100 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

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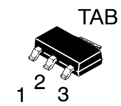
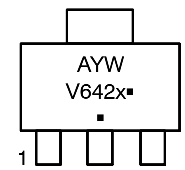
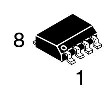
MARKING DIAGRAM

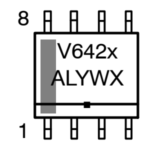


SOT−223
ST SUFFIX
CASE 318E





SOIC−8 Fused
CASE 751



x	= 5 (5.0 V Version)
	3 (3.3 V Version)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

(SOT−223)

PIN	FUNCTION
1	V_{IN}
2,TAB	GND
3	V_{OUT}

(SOIC−8 Fused)

PIN	FUNCTION
1	NC
2,	V_{IN}
3	GND
4.	V_{OUT}
5−8.	NC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

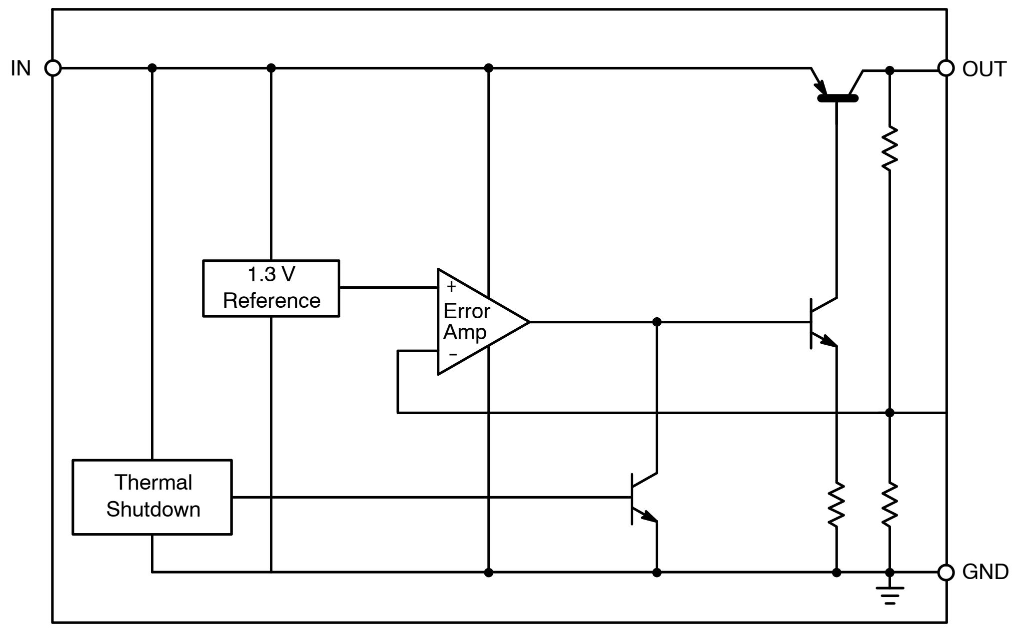


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.		Symbol	Function
SOT−223	SOIC−8		
1	2	V_{IN}	Unregulated input voltage; 4.5 V to 45 V.
2	3	GND	Ground; substrate.
3	4	V_{OUT}	Regulated output voltage; collector of the internal PNP pass transistor.
TAB	–	GND	Ground; substrate and best thermal connection to the die.
–	1, 5−8	NC	No Connection.

OPERATING RANGE

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Input Operating Voltage (Note 3)	V_{IN}	4.5	+45	V
Junction Temperature Operating Range	T_J	−40	+150	°C

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Input Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+18	V
Storage Temperature	T_{stg}	−55	+150	°C
Moisture Sensitivity Level SOT223 SOIC−8 Fused	MSL	3 1		–
ESD Capability, Human Body Model (Note 1)	V_{ESDHB}	4000	–	V
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	–	V
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 2)	T_{sld}	–	265 pk	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)
2. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.
3. See specific conditions for DC operating input voltage lower than 4.5 V in the ELECTRICAL CHRACTERISTICS table at page 3

THERMAL RESISTANCE

Parameter		Symbol	Min	Max	Unit
Junction−to−Ambient	SOT−223 SOIC−8 Fused	$R_{\theta JA}$	–	99 (Note 4) 145	°C/W
Junction−to−Case	SOT−223 SOIC−8 Fused	$R_{\theta JC}$	–	17 –	

ELECTRICAL CHARACTERISTICS (V_{IN} = 13.5 V, T_J = −40°C to +150°C, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	V_{OUT}	5.0 mA ≤ I_{OUT} ≤ 100 mA (Note 5) 6.0 V ≤ V_{IN} ≤ 28 V	4.900	5.000	5.100	V
Output Voltage 3.3 V Version	V_{OUT}	5.0 mA ≤ I_{OUT} ≤ 100 mA (Note 5) 4.5 V ≤ V_{IN} ≤ 28 V	3.234	3.300	3.366	V
Output Voltage 3.3 V Version	V_{OUT}	I_{OUT} = 5 mA, V_{IN} = 4 V (Note 7)	3.234	3.300	3.366	V
Line Regulation 5.0 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 6.0 V ≤ V_{IN} ≤ 28 V	−30	5.0	+30	mV
Line Regulation 3.3 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 4.5 V ≤ V_{IN} ≤ 28 V	−30	5.0	+30	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	1.0 mA ≤ I_{OUT} ≤ 100 mA (Note 5)	−40	5.0	+40	mV
Dropout Voltage − 5.0 V Version	V_{IN}–V_{OUT}	I_{OUT} = 100 mA (Notes 5 & 6)	–	270	500	mV
Dropout Voltage − 3.3 V Version	V_{IN}–V_{OUT}	I_{OUT} = 100 mA (Notes 5 & 8)	–	–	1.266	V
Quiescent Current	I_q	I_{OUT} = 100 μA T_J = 25°C T_J = −40°C to +85°C T_J = −40°C to 150°C	 – – –	 33 33 33	 55 60 70	μA
Active Ground Current	$I_{G(ON)}$	I_{OUT} = 50 mA (Note 5)	–	1.5	4.0	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 $V_{P−P}$, F = 100 Hz	–	67	–	dB
Output Capacitor for Stability 5.0 V Version	C_{OUT} ESR	I_{OUT} = 0.1 mA to 100 mA (Notes 5 & 7)	10 –	– –	– 9.0	μF Ω
Output Capacitor for Stability 3.3 V Version	C_{OUT} ESR	I_{OUT} = 0.1 mA to 100 mA (Notes 5 & 7)	22 –	– –	– 16	μF Ω

PROTECTION

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 4.5 V (5.0 V Version) (Note 5) V_{OUT} = 3.0 V (3.3 V Version) (Note 5)	150 150	– –	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 5)	40	–	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 7)	150	–	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. 1 oz., 100 mm^2 copper area.
5. Use pulse loading to limit power dissipation.
6. Dropout voltage = (V_{IN}–V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
7. Not tested in production. Limits are guaranteed by design.
8. V_{DO} = V_{IN} − V_{OUT}. For output voltage set to < 4.5 V, V_{DO} will be constrained by the minimum input voltage.

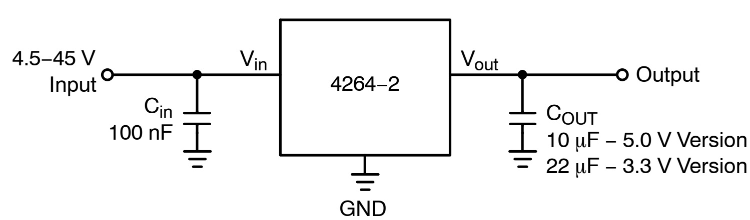


Figure 2. Applications Circuit

TYPICAL CHARACTERISTIC CURVES − 5 V Version

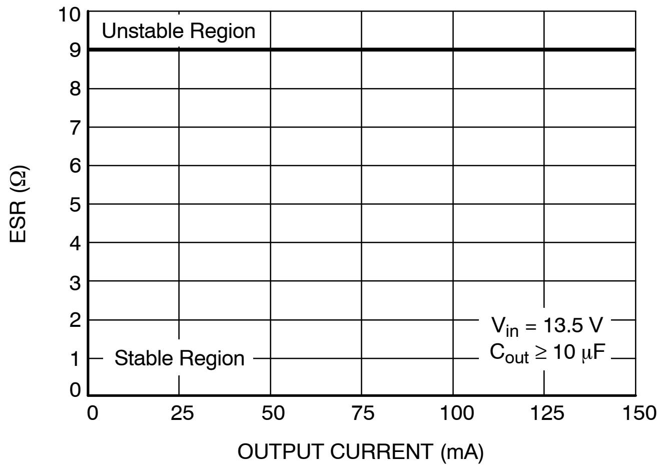


Figure 3. ESR Stability vs. Output Current (5 V Version)

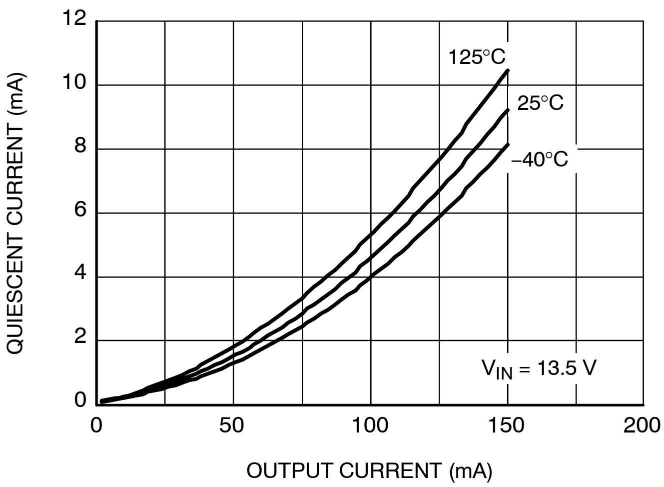


Figure 4. Quiescent Current vs. Output Current (5 V Version)

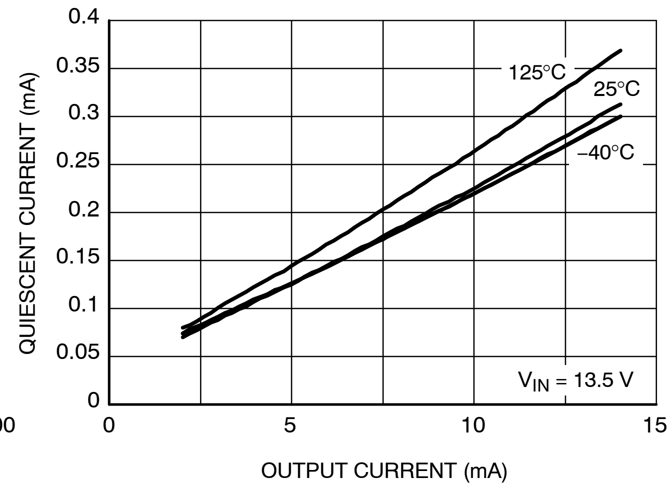


Figure 5. Quiescent Current vs. Output Current (Light Load) (5 V Version)

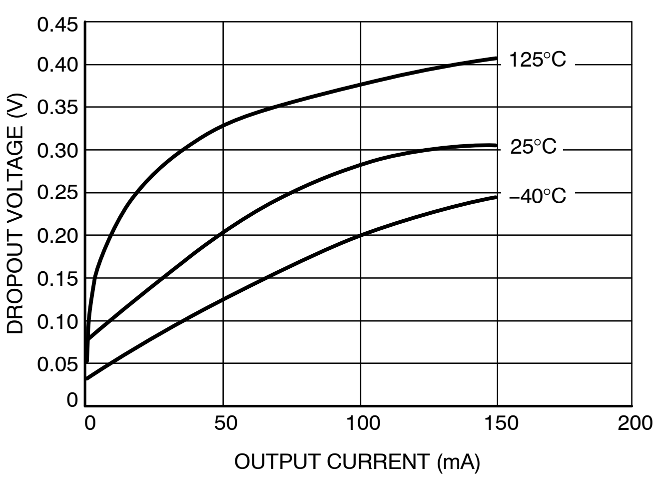


Figure 6. Dropout Voltage vs. Output Current (5 V Version)

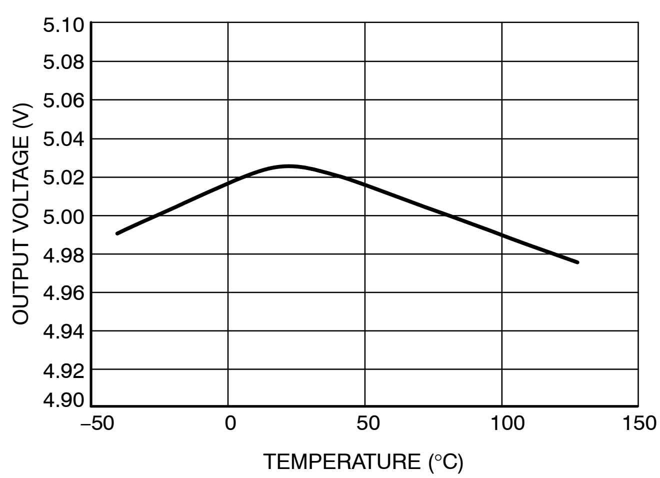


Figure 7. Output Voltage vs. Temperature (5 V Version)

TYPICAL CHARACTERISTIC CURVES − 5 V Version

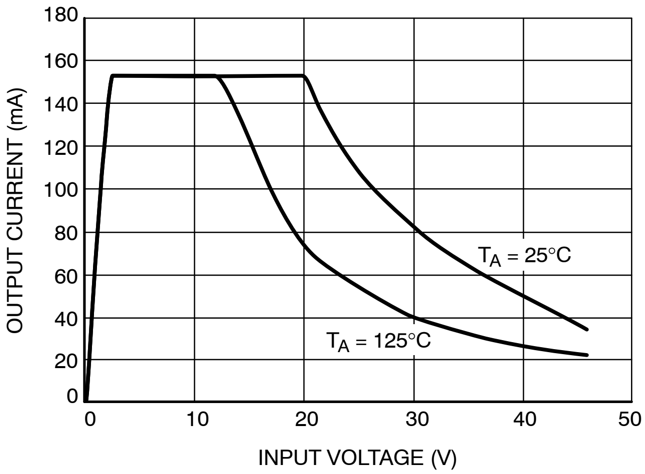


Figure 8. Output Current vs. Input Voltage (5 V Version)

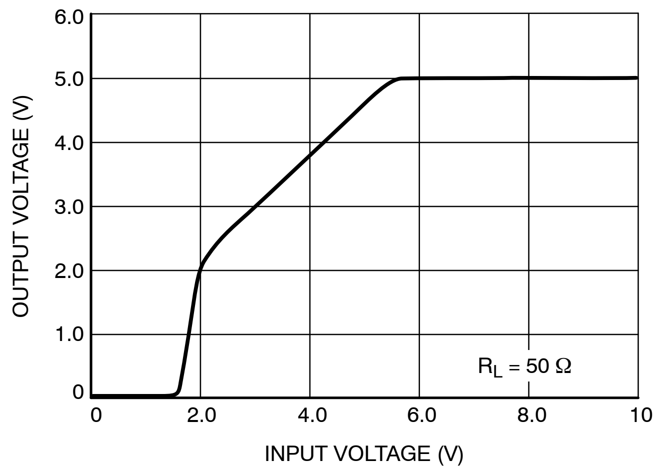


Figure 9. Output Voltage vs. Input Voltage (5 V Version)

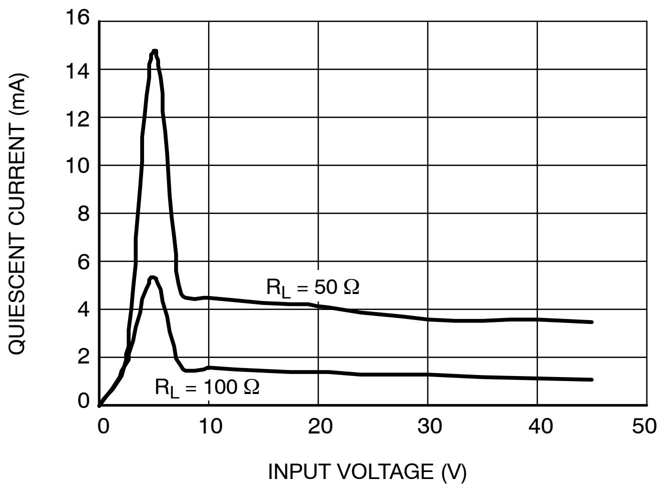


Figure 10. Quiescent Current vs. Input Voltage (5 V Version)

TYPICAL CHARACTERISTIC CURVES − 3.3 V Version

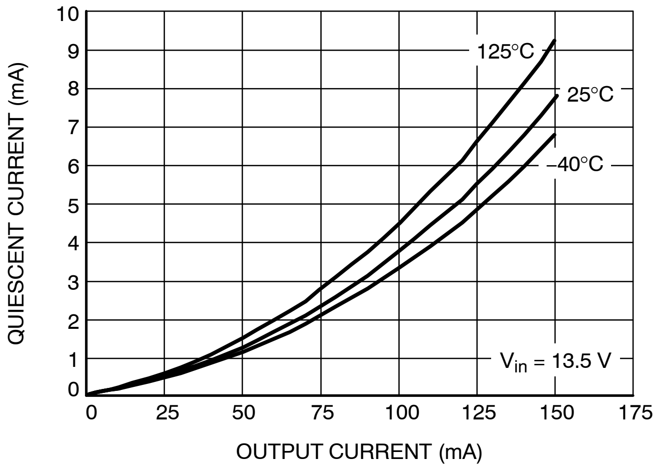


Figure 11. Quiescent Current vs. Output Current (3.3 V Version)

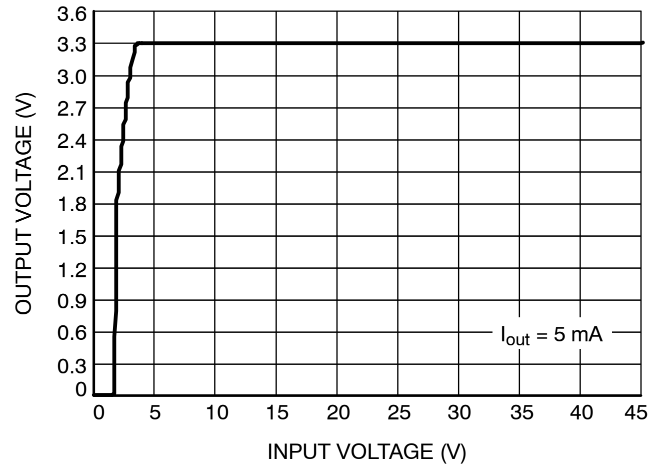


Figure 12. Output Voltage vs. Input Voltage (3.3 V Version)

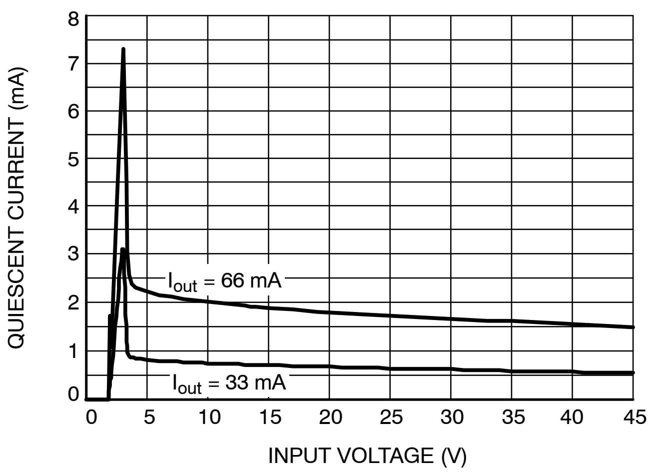


Figure 13. Quiescent Current vs. Input Voltage (3.3 V Version)

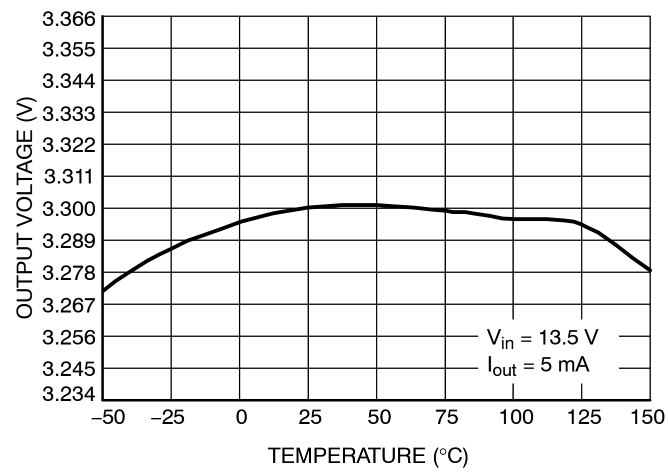


Figure 14. Output Voltage vs. Temperature (3.3 V Version)

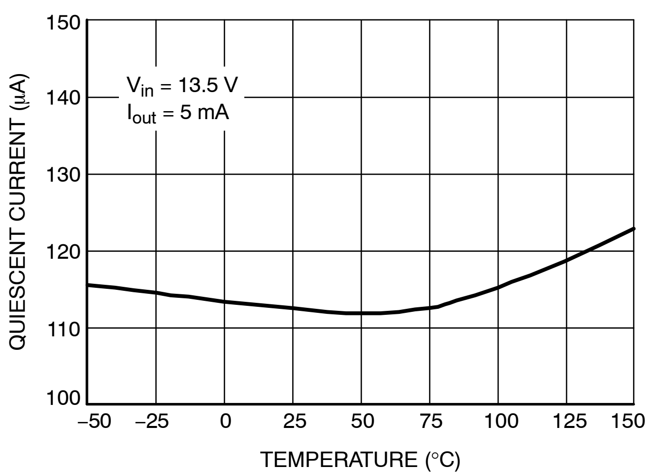


Figure 15. Quiescent Current vs. Temperature (3.3 V Version)

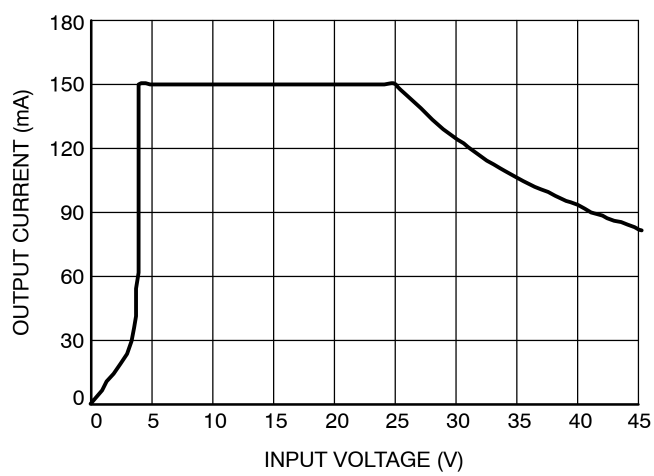


Figure 16. Output Current vs. Input Voltage (3.3 V Version)

TYPICAL CHARACTERISTIC CURVES − 3.3 V Version

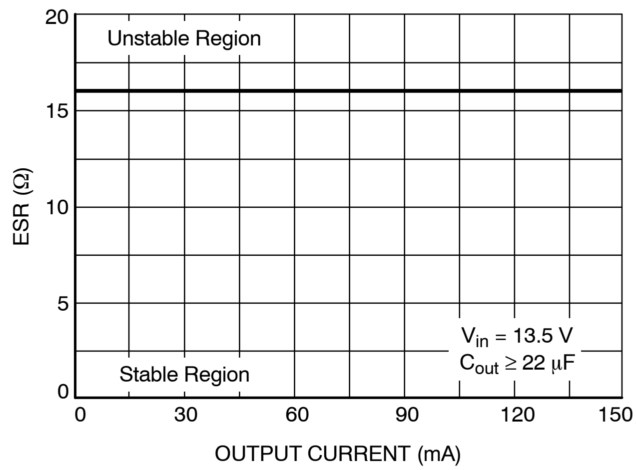


Figure 17. ESR Stability vs. Output Current (3.3 V Version)

Circuit Description

The NCV4264−2 is functionally and pin for pin compatible with NCV4264 with a lower quiescent current consumption. Its output stage supplies 100 mA with ±2.0% output voltage accuracy.

Maximum dropout voltage is 500 mV at 100 mA load current. It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{OUT}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{I2}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values of $C_Q \geq 10\ \mu F$, with an ESR $\leq 9\ \Omega$ for the 5.0 V Version, and $C_Q \geq 22\ \mu F$ with an ESR $\leq 16\ \Omega$ for the 3.3 V Version within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 2) is:

$$P_{D(max)} = \left[V_{IN(max)} - V_{OUT(min)}\right] * I_{OUT(max)} + V_{IN(max)} * I_q \qquad \text{(eq. 1)}$$

Where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{OUT(max)}$. Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{(150^{\circ}C - T_A)}{P_D} \qquad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JA}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

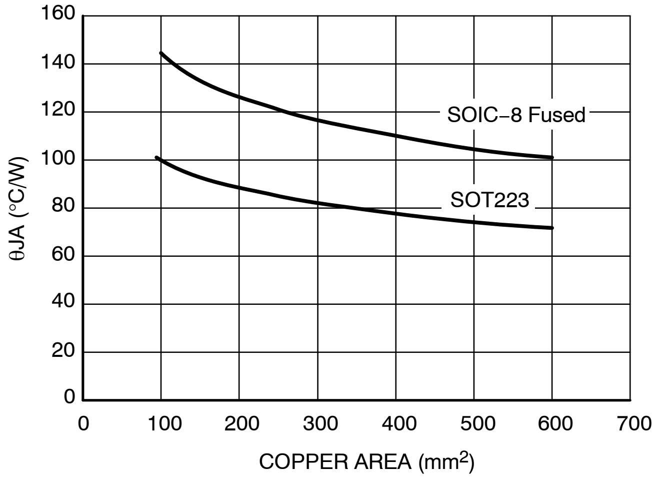


Figure 18. θJA vs. Copper Spreader Area

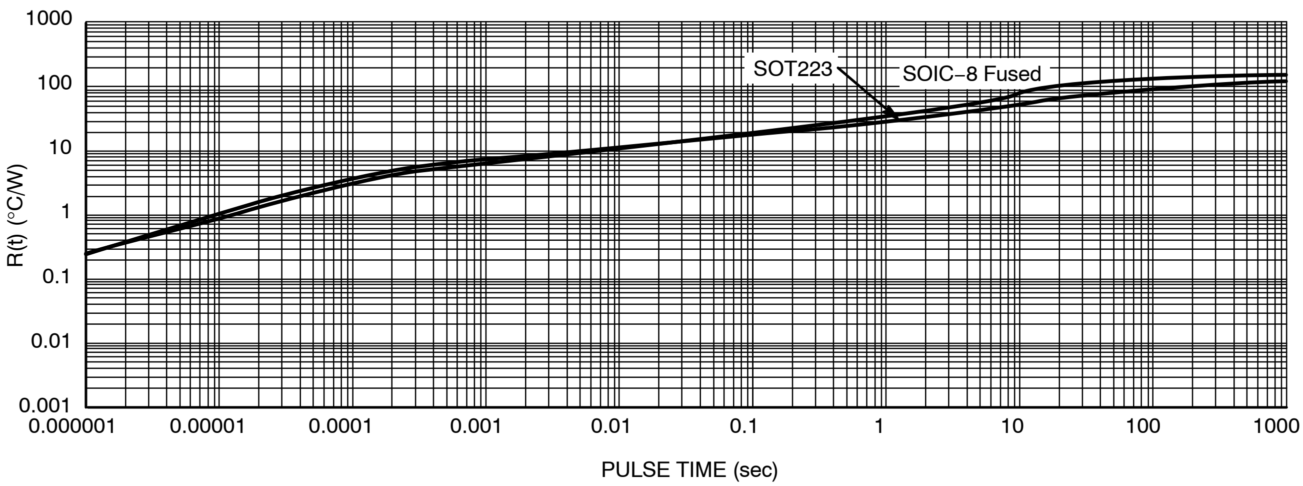


Figure 19. R(t) vs. Pulse Time

ORDERING INFORMATION

Device*	Package	Shipping†
NCV4264−2ST50T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4264−2ST33T3G	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV4264−2D33R2G	SOIC−8 Fused (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.