This document, NCV7361/D is Not Recommended for New Design. Please refer to NCV7361A/D. 12/Oct/2004

October, 2004 − Rev. 1
Publication Order Number:
NCV7361/D

NCV7361

Voltage Regulator with Integrated LIN Transceiver

The NCV7361 consists of a low drop voltage regulator, 5.0 V/50 mA and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conforming to “LIN−Protocol Specification” rev. 1.3.

The combination of voltage regulator and bus transceiver make it ideal for a powerful and cheap slave node in a LIN Bus system.

Features

- Operating Voltage V_{SUP} = 5.5 to 18 V
- Very Low Standby Current Consumption < 110 μA in Normal Mode (< 50 μA in Sleep Mode)
- LIN−Bus Transceiver:
  - PNP−Bipolar Transistor Driver
  - Slew Rate Control and Wave Shaping for Best EMC Behavior
  - BUS Input Voltage −24 V to 30 V (Independent of V_{SUP})
  - Wake−Up Via LIN Bus
  - Baud Rate up to 20 kBaud
  - Compatible to LIN Specification 1.3
  - Compatible to ISO9141
- Wake−Up by LIN BUS and Startup Capable Independent of EN Voltage Level
- Linear Low Drop Voltage Regulator:
  - Output Voltage 5.0 V ±2%
  - Output Current Max. 50 mA
  - Output Current Limit
  - Overtemperature Shutdown
- Reset Time 100 ms and Reset Threshold Voltage 4.65 V
- CMOS Compatible Interface to Microcontroller
- Load Dump Protected (40 V Peak)
- Resistant Against Transient Pulses According to ISO 7637 at Pin V_{SUP}, BUS and EN
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

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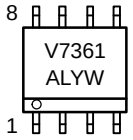
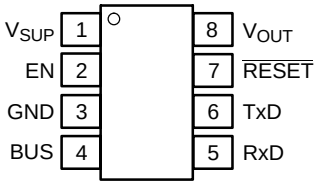
MARKING DIAGRAM

SO−8
D SUFFIX
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7361D	SO−8	98 Units/Rail
NCV7361DR2	SO−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

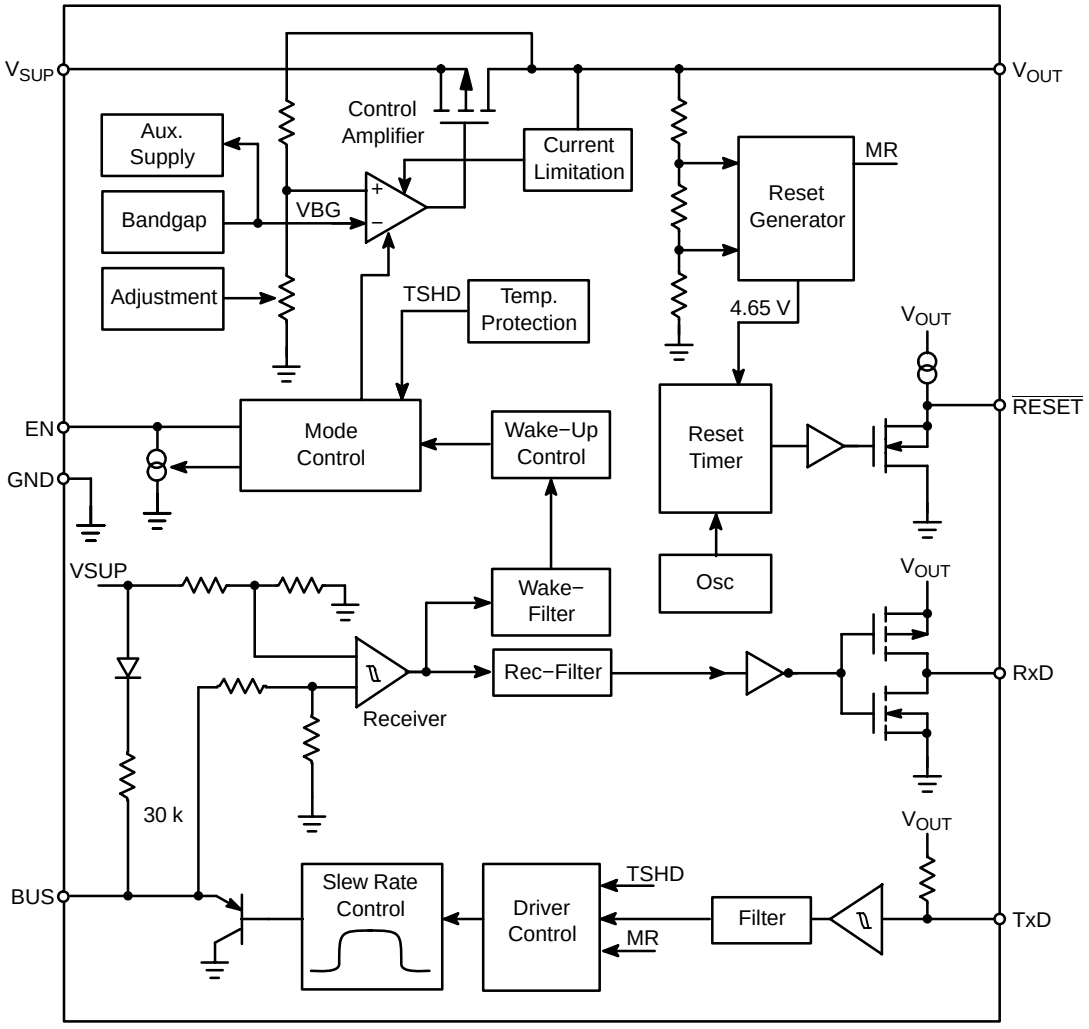


Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

Pin	Symbol	Description
1	V_{SUP}	Supply voltage.
2	EN	Enable input controls the regulator. Active high.
3	GND	Ground
4	BUS	LIN bus line.
5	RxD	Receive output (push−pull to V_{OUT}).
6	TxD	Transmit input (pullup−input to V_{OUT}).
7	$\overline{RESET}$	Reset output, active low (pullup to V_{OUT}).
8	V_{OUT}	Regulator output 5.0 V/50 mA.

ELECTRICAL SPECIFICATIONS

All voltages are referenced to ground (GND). Positive currents flow into the IC.

The maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device can't be guaranteed if any of these limits are exceeded.

OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	VSUP	5.25	18	V
Operating Ambient Temperature	T_A	−40	+125	°C
Junction Temperature	T_J	−	+150	°C

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
V_{SUP}	V_{SUP}	−	−1.0	30	V
		T ≤ 500 ms	−	40	
BUS	V_{BUS}	−	−24	30	V
		T ≤ 500 ms	−	40	
Difference VSUP−V_{OUT}	VSUP−V_{OUT}	−	−0.3	40	V
EN	V_{INEN}	−	−0.3	VSUP + 0.3	V
TxD, RxD, $\overline{\text{RESET}}$	V_{IN}	−	−0.3	V_{OUT} + 0.3	V
EN, TxD, RxD, $\overline{\text{RESET}}$	I_{IN}	−	−25	25	mA
Short Circuit of Pin VSUP and V_{OUT}	I_{INSH}	−	−500	500	mA
ESD Capability TxD Pin	ESD_{BUSHB}	Human Body Model, 100 pF via 1.5 kΩ	−1.0	1.0	kV
ESD Capability on All Other Pins	ESD_{HB}	Human Body Model, 100 pF via 1.5 kΩ	−2.0	2.0	kV
Junction Temperature	T_J	−	−	150	°C
Storage Temperature	T_{STG}	−	−55	150	°C
Lead Temperature Soldering Reflow: (SMD styles only)	T_{sld}	60 second maximum above 183°C −5°C/+0°C allowable conditions	−	240 peak	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL RATINGS

Parameter	Test Conditions Typical Value		Units
SO−8 Package	**Min−Pad Board** (Note 1)	**1.0 in Pad Board** (Note 2)	
Junction−to−Tab (psi−JL2, Ψ_{JLZ}) (Note 3)	48	43	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	183	120	°C/W

1. 1 oz copper, 54 mm^2 copper area, 0.062" thick FR4.
2. 1 oz copper, 714 mm^2 copper area, 0.062" thick FR4.
3. psi−JL2 temperature was made at foot of lead #2.

ELECTRICAL CHARACTERISTICS (5.25 V ≤ VSUP ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
GENERAL						
Supply Current with V_{OUT} "No Load" (Note 4)	I_{Snl}	V_{EN} = V_{SUP} = 12 V, V_{BUS} > VSUP − 0.5 V, Pins 5 to 8 Open	−	−	110	μA
Supply Current, "Sleep Mode"	I_{Ssleep}	V_{SUP} = 12 V, V_{EN} = 0 V, V_{BUS} > V_{SUP} − 0.5 V	−	35	50	μA
Thermal Shutdown (Note 5)	$T_{jshutdown}$	−	155	−	175	°C
Thermal Recovery (Note 5)	T_{jrec}	−	126	−	130	°C
V_{OUT}						
Output Voltage	V_{OUTt}	5.5 V ≤ V_{SUP} ≤ 18 V 0 < I_{OUT} < 50 mA	4.90	5.0	5.10	V
	V_{OUTh}	V_{SUP} > 18 V	4.90	5.0	5.25	V
	V_{OUTl}	IV_{OUT} = 20 mA, V_{SUP} = 3.3 V	−	V_{SUP}−V_D	−	V
		IV_{OUT} = 50 mA, V_{SUP} = 3.3 V	−	V_{SUP}−V_D	−	V
Drop−Out Voltage (Note 6) V_D = V_{SUP}−V_{OUT}	V_D	IV_{OUT} = 20 mA	−	−	150	mV
		IV_{OUT} = 50 mA	−	−	500	mV
Output Current	IV_{OUT}	3.0 V < V_{SUP} < 18 V V_{OUT} = 0 V	50	−	150	mA
Load Capacity	C_{load}	Reference Figure 25	4.7	−	−	μF
ENABLE (EN)						
Input Voltage Low	V_{ENL}	−	−0.3	−	1.6	V
Input Voltage High	V_{ENH}	−	2.5	−	VSUP +0.3	V
Hysteresis (Note 5)	V_{ENHYS}	−	100	−	−	mV
Pulldown Current	I_{pdEN}	V_{EN} > V_{ENH}	1.8	4.0	7.5	μA
		V_{EN} < V_{ENL}	70	100	130	μA
$\overline{\text{RESET}}$						
Output Voltage Low	V_{OL}	I_{OUT} = 1.0 mA, V_{SUP} > 5.5 V	−	−	0.8	V
		10 kΩ $\overline{\text{RESET}}$ to V_{OUT} V_{SUP} = V_{OUT} = 0.8 V	−	−	0.2	V
Pullup Current	I_{pu}	−	−500	−375	−250	μA
$\overline{\text{RESET}}$ Threshold	V_{RES}	Referred to V_{OUT}, V_{SUP} > 4.6 V	4.5	4.65	4.8	V
Power−on−Reset Threshold (Note 5)	V_{POR}	−	3.0	3.15	3.3	V

4. See Figure 5 for test setup.
5. Not production tested, guaranteed by design and qualification.
6. Measured when the output voltage has dropped 100 mV from the V_{SUP} = 12 V nominal value.

ELECTRICAL CHARACTERISTICS (5.25 V ≤ VSUP ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
LIN BUS INTERFACE						
Receive Threshold	V_{thr_rec}, V_{thr_dom}	7.3 V ≤ VSUP ≤ 18 V	0.4 *VSUP	−	0.6 *VSUP	V
Receive Center Point $V_{thr\_cnt} = (V_{thr\_rec} + V_{thr\_dom})/2$	V_{thr_cnt}		0.475 *VSUP	0.5 *VSUP	0.525 *VSUP	
Receive Hysteresis $V_{thr\_hys} = V_{thr\_rec} - V_{thr\_dom}$	V_{thr_hys}		0.12 *VSUP	0.135 *VSUP	0.15 *VSUP	
BUS Input Current (Recessive) (Note 7)	I_{INBUSR}	8.0 ≤ V_{BUS} ≤ 18 V, V_{SUP} = V_{BUS} − 0.7 V, TxD = 4.5 V	−	−	20	μA
BUS Input Current (Recessive)	$-I_{INBUSR}$	V_{SUP} = 0 V, V_{BUS} = −12 V	−1.0	−	−	mA
BUS Input Current (Recessive)	$-I_{INBUSR}$	V_{SUP} = Open, V_{BUS} = −18 V	−1.0	−	−	mA
BUS Pullup Resistor	R_{BUSpu}	−	20	30	47	kΩ
BUS Output Voltage (Dominant) (Note 7)	V_{BUSdom}	7.3 ≤ V_{SUP} ≤ 18 V, TxD = 0 V, R_L = 500 Ω	−	−	1.2	V
BUS Output Voltage (Recessive) (Notes 7 and 8)	V_{BUSrec}	7.3 ≤ V_{SUP} ≤ 18 V, TxD = 4.5 V	0.8 *VSUP	−	−	V
BUS Current Limit	I_{LIM}	V_{BUS} > 2.5 V, TxD = 0 V	40	−	120	mA
TxD						
Pull−Up Current	Ipu	−	−500	−375	−250	μA
Input Low Level	V_{IL}	−	−	−	1.25	V
Input High Level	V_{IH}	−	3.75	−	−	V
RxD						
Output Voltage Low	V_{OL}	I_{OUT} = 1.0 mA	−	−	0.8	V
Output Voltage High	V_{OH}	I_{OUT} = −1.0 mA	4.2	−	−	V

7. See Figures 6, 7, and 8 for test setup.
8. The recessive voltage on BUS should be less than 80% direct battery. The LIN protocol requires an external reverse battery diode between the battery and VSUP. VSUP = V_{BAT} −0.7 V.

ELECTRICAL CHARACTERISTICS (8.0 V ≤ VSUP ≤ 18 V, −40°C ≤ T_A ≤ 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ AC CHARACTERISTICS						
Reset Time	t_{Res}	5.25 ≤ V_{SUP} ≤ 18 V	70	100	140	ms
Reset Rise Time (Note 9)	t_{rr}	5.25 ≤ V_{SUP} ≤ 18 V	3.0	6.5	10	μs
LIN BUS INTERFACE AC CHARACTERISTICS						
Transmit Propagation Delay TxD −> BUS (Notes 10 and 11)	t_{dr_TXD}, t_{df_TXD}	R_L/C_L at BUS 1.0 kΩ/1.0 nF 660 Ω/6.8 nF 500 Ω/10 nF	−	−	4.0	μs
Symmetry of Propagation Delay BUS −> RxD (Note 10)	t_{dsym_TXD}	$t_{dr\_TXD} - t_{df\_TXD}$	−2.0	−	2.0	μs
Receiver Propagation Delay BUS −> RxD (Notes 10 and 11)	t_{dr_RXD} t_{df_RXD}	$C_{L(RXD)}$ = 50 pF	−	−	6.0	μs
Symmetry of Propagation Delay TxD −> BUS (Note 10)	t_{dsym_RXD}	$t_{dr\_RXD} - t_{df\_RXD}$	−2.0	−	2.0	μs
Slew Rate BUS Rising Edge (Note 9)	dV/dT_{rise}	20% ≤ V_{BUS} ≤ 80% C_L = 1.0 nF, R_L = 1.0 kΩ	1.0	2.0	2.5	V/μs
Slew Rate BUS Falling Edge (Note 9)	dV/dT_{fall}	20% ≤ V_{BUS} ≤ 80% C_L = 1.0 nF, R_L = 1.0 kΩ	−2.5	−2.0	−1.0	V/μs
Slope Time, Transition from Recessive to Dominant (Notes 11 and 12)	t_{sdom}	VSUP = 8.0 V R_L = 500 Ω/C_L = 10 nF	−	−	12	μs
Slope Time, Transition from Dominant to Recessive (Notes 11 and 13)	t_{srec}	VSUP = 8.0 V R_L = 500 Ω/C_L = 10 nF	−	−	12	μs
Slope Time Symmetry	t_{ssym}	VSUP = 8.0 V R_L = 500 Ω/C_L = 10 nF $T_{ssym} = t_{sdom} - t_{srec}$	−7.0	−	1.0	μs
Slope Time, Transition from Recessive to Dominant (Notes 11 and 12)	t_{sdom}	VSUP = 18 V R_L = 500 Ω/C_L = 10 nF	−	−	18	μs
Slope Time, Transition from Dominant to Recessive (Notes 11 and 13)	t_{srec}	VSUP = 18 V R_L = 500 Ω/C_L = 10 nF	−	−	18	μs
Slope Time Symmetry	t_{ssym}	VSUP = 18 V R_L = 500 Ω/C_L = 10 nF $T_{ssym} = t_{sdom} - t_{srec}$	−5.0	−	5.0	μs
BUS Debounce Time (Note 14)	t_{deb_BUS}	−	1.5	2.8	4.0	μs
Wake−Up Time	t_{Wake_BUS}	−	25	60	120	μs

9. Not production tested, guaranteed by design and qualification.
10. See Figures 2 and 3, Timing Diagrams.
11. See Figures 4, 5, 6, 7, and 8 for test setup.
12. $t_{sdom} = (t_{VBUS40\%} - t_{VBUS95\%}) / 0.55$.
13. $t_{sdom} = (t_{VBUS60\%} - t_{VBUS5\%}) / 0.55$.
14. See Figure 14.

TIMING DIAGRAMS

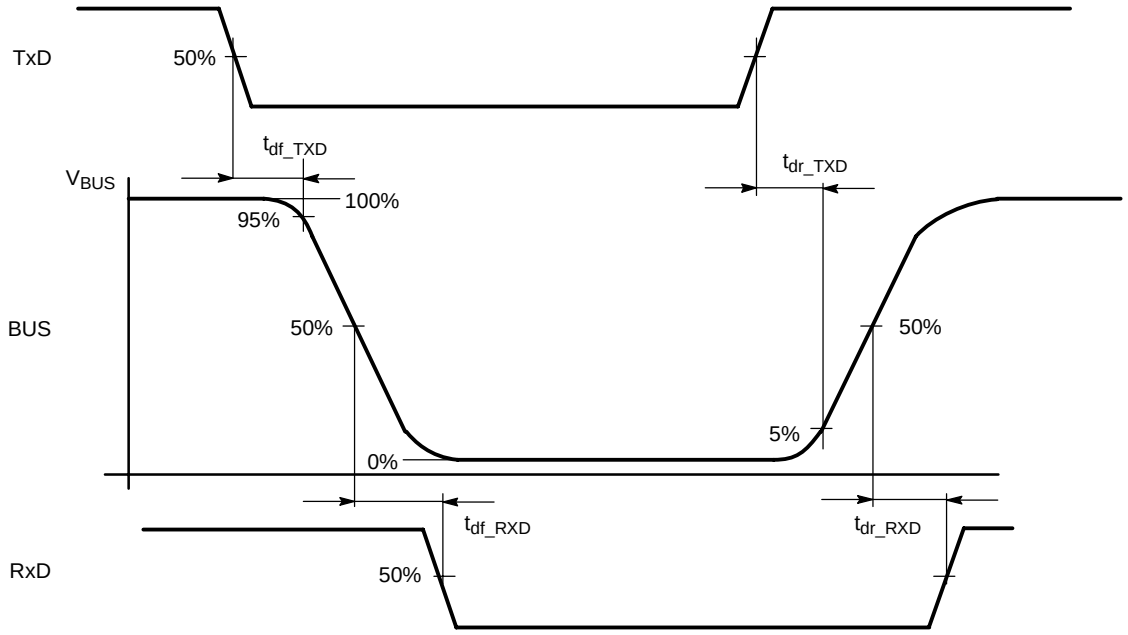


Figure 2. Timing Diagram for Propagation Delay

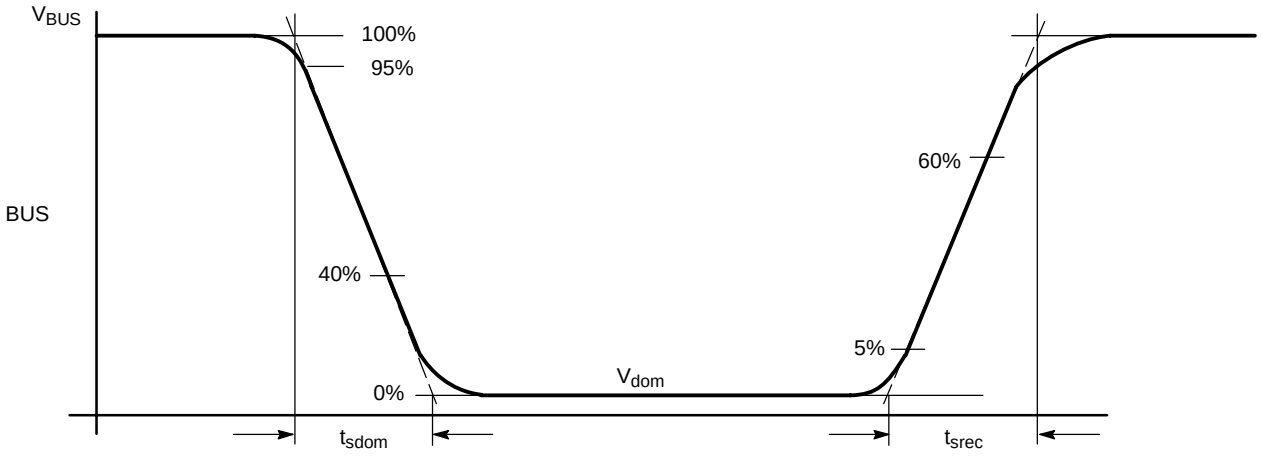


Figure 3. Timing Diagram for Slope Times

TEST CIRCUITS

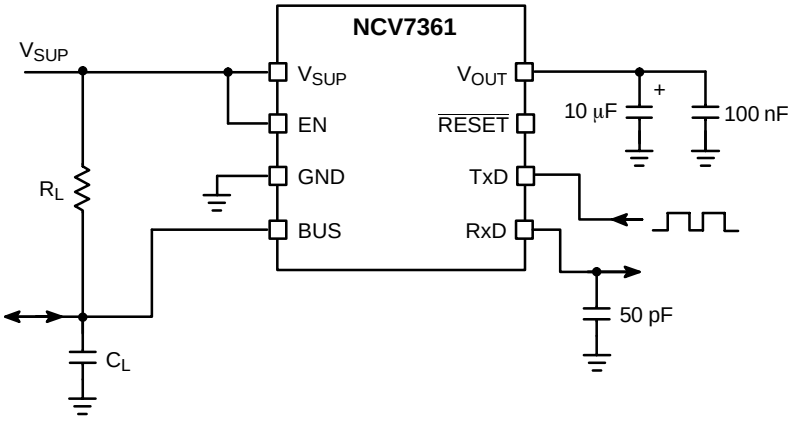


Figure 4. Test Circuit for Delay Time and Slope Control

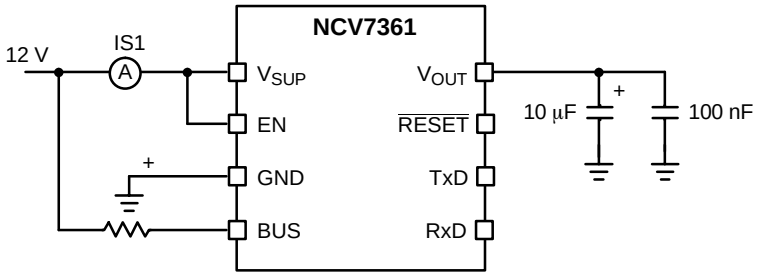


Figure 5. Test Circuit for Supply Current I_{SnI}

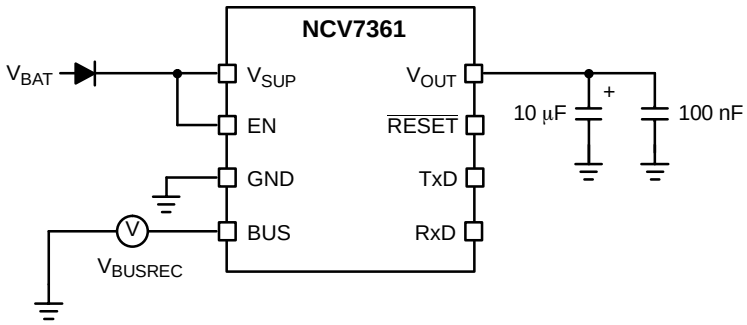


Figure 6. Test Circuit for Bus Voltage "Recessive" (V_{BUSREC})

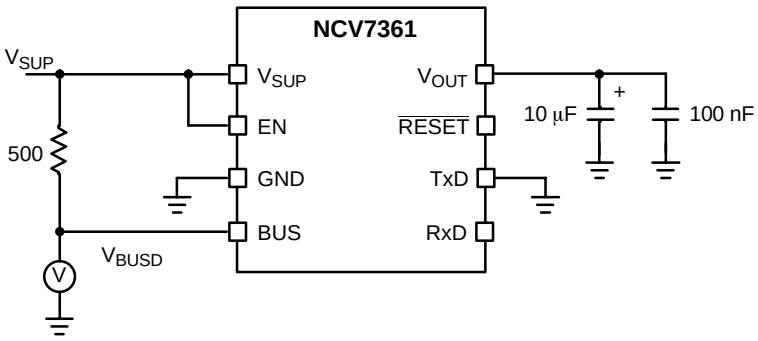


Figure 7. Test Circuit for Bus Voltage "Dominant" V_{BUSDOM}

TEST CIRCUITS (continued)

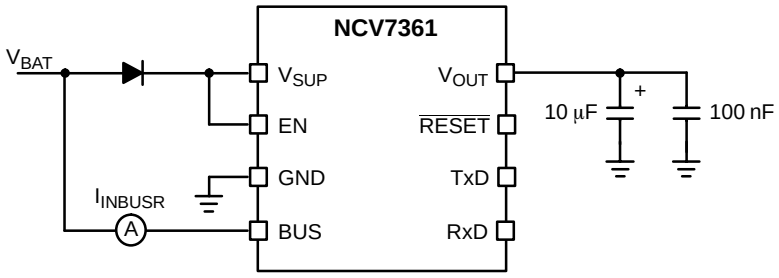


Figure 8. Test Circuit for Bus Current "Recessive" I_{INBUSR}

TYPICAL OPERATING CHARACTERISTICS

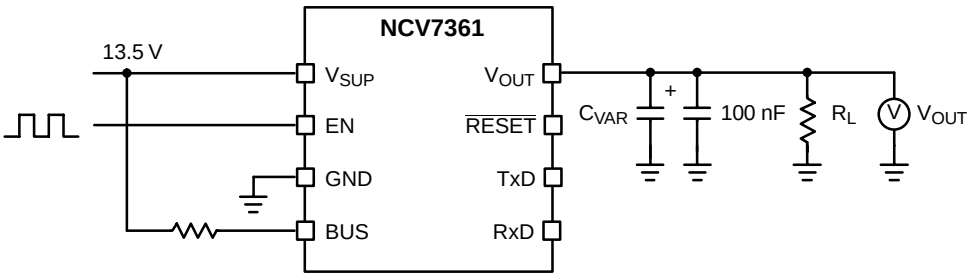


Figure 9. Test Circuit for V_{OUT} Rise Time vs. Load Capacitance and Resistance

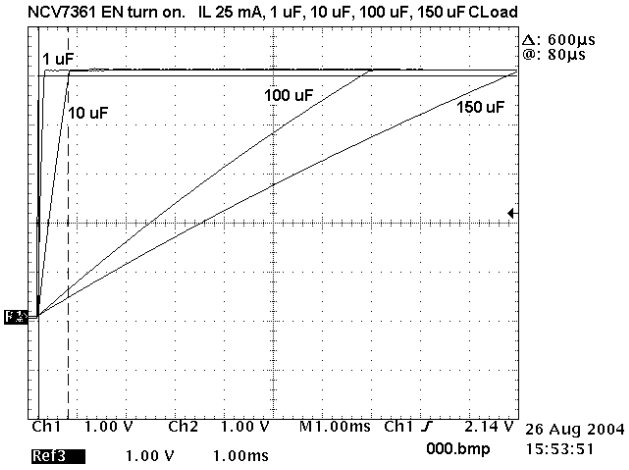


Figure 10. V_{out} Rise Time with 1 µF, 10 µF, 100 µF, and 150 µF Capacitors and 200 Ω Load using EN to Enable the Output.

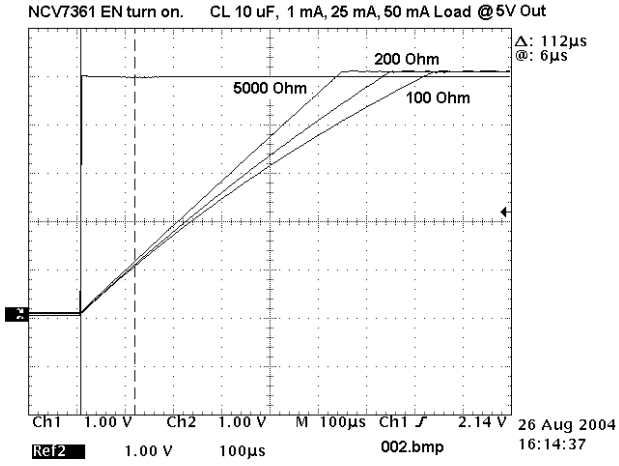


Figure 11. V_{out} Rise Time with a 10 µF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

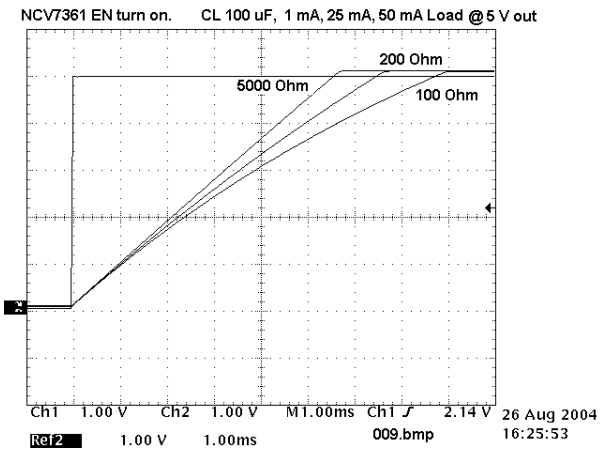


Figure 12. V_{out} Rise Time with a 100 µF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

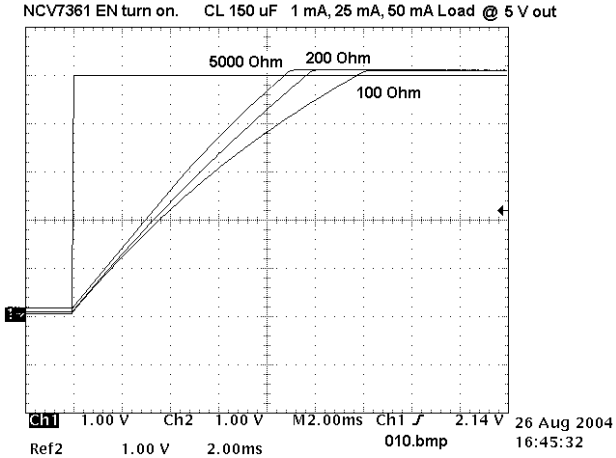


Figure 13. V_{out} Rise Time with a 150 µF Load Capacitor and 1 kΩ, 200 Ω, and 100 Ω Load using EN to Enable the Output.

FUNCTIONAL DESCRIPTION

The NCV7361 consists of a low drop voltage regulator 5.0 V/50 mA and a LIN Bus transceiver, which is a bidirectional bus interface for data transfer between the LIN bus and the LIN protocol controller.

Additionally, the NCV7361 features a $\overline{\text{RESET}}$ output with a reset delay of 100 ms and a fixed threshold of 4.65 V and Enable (EN) control for the regulator.

Operating Modes

The EN pin controls the NCV7361 different operating modes:

Normal Mode

All circuitry is active. Switching to normal mode can be done via the following actions:

- EN Low to High (Local Wake−Up)
- Activity on the LIN Bus (Remote Wake−Up)
- Power On Reset

Sleep Mode

The sleep mode is the most current saving mode. EN high to low switches to this node. The voltage regulator will be switched off and the LIN transceiver is in the recessive state.

Switching into sleep mode can be done independent from the current transceiver state. That means the transmitters dominant state will be cancelled and will switch to the recessive state.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 155°C, the NCV7361 may switch into the thermal shutdown mode. Thermal shutdown is comparable with the sleep mode.

If T_J falls below the thermal shutdown temperature (typ. 140°C), the NCV7361 will be switched to the previous state.

LIN BUS Transceiver

The NCV7361 is a bidirectional bus interface device for data transfer between the LIN bus and the LIN protocol controller.

The transceiver consists of a pnp−driver (1.2 V @ 40 mA) with slew rate control, wave shaping and current limit, and a high voltage receiver/comparator followed by a filter circuit.

Transmit Mode

During transmission the data at the TxD pin will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver has integrated slew rate control and wave shaping circuitry.

Transmitting will be interrupted in the following cases:

- Sleep Mode
- Thermal Shutdown Active
- Master Reset (V_{OUT} < 3.15 V)

The recessive BUS level is generated from the integrated 30 k pullup resistor in series with a diode This diode prevents reverse current on V_{BUS} when $V_{BUS} > V_{SUP}$.

No additional termination resistor is necessary to use the NCV7361 in LIN slave nodes. If this IC is used for LIN master nodes, it is necessary to terminate the bus pin with an external 1.0 kΩ resistor in series with a diode to VBAT.

Receive Mode

The data signal from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus are suppressed by the internal filter circuit (τ = 2.8 μs).

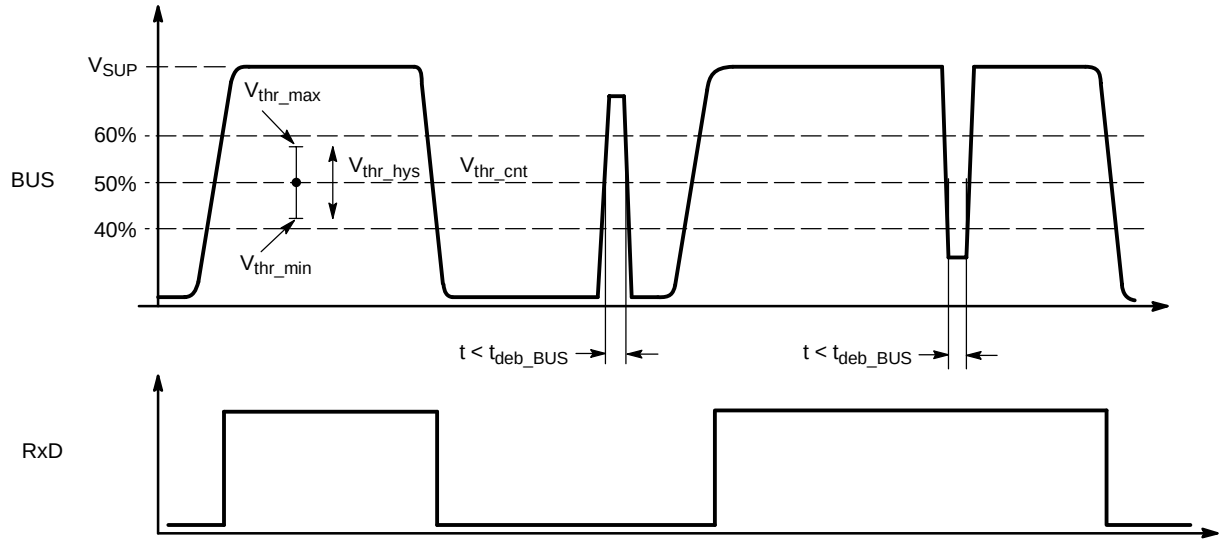


Figure 14. Receive Mode Impulse Diagram

The receive threshold values V_{thr_max} and V_{thr_min} are symmetrical to 0.5*VSUP with a hysteresis of 0.135*VSUP. The LIN specific receive threshold is between 0.4*VSUP and 0.6*VSUP.

Data Rate

The NCV7361 is a *constant slew rate* transceiver. The bus driver works with a fixed slew rate range of 1.0 V/μs $\leq \Delta V/\Delta T \leq$ 2.5 V/μs. This principle provides good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).

The NCV7361 guarantees data rates up to 20 kbit within the complete bus load range under worst case conditions. The constant slew rate principle holds appropriate voltage levels and can operate within the LIN Protocol Specification for RC oscillator systems with a matching tolerance up to ±2% between 2 nodes.

TxD Input

The 5.0 V input TxD directly controls the BUS level:

TxD = low $\rightarrow$ BUS = low (dominant level)

TxD = high $\rightarrow$ BUS = high (recessive level)

The TxD pin has an internal pullup resistor connected to V_{OUT}. This secures that an open TxD pin generates a recessive BUS level.

RxD Output

The received BUS signal will be output to the 5.0 V RxD pin:

BUS < V_{thr_cnt} − 0.5 * V_{thr_hys} → RxD = low

BUS > V_{thr_cnt} + 0.5 * V_{thr_hys} → RxD = high

This output is a push−pull driver between V_{OUT} and GND with an output current capability of 1.0 mA.

Linear Regulator

The NCV7361 has an integrated low dropout linear regulator with a P−Channel MOSFET output driver whose output is 5.0 V ±2% at ≤50 mA and 5.5 V ≤ V_{SUP} ≤ 18 V. Figure 15 shows typical current limit based on the output voltage.

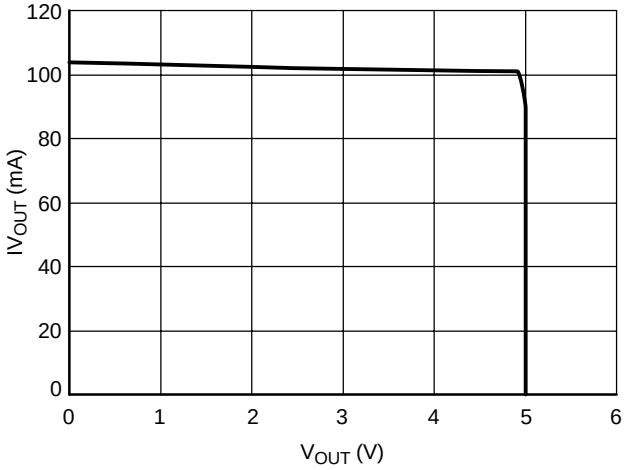


Figure 15. Characteristic of Current Limit vs. Output Voltage

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ switches from low to high if V_{SUP} is switched on and $V_{OUT} > V_{RES}$ for t_{Res}.

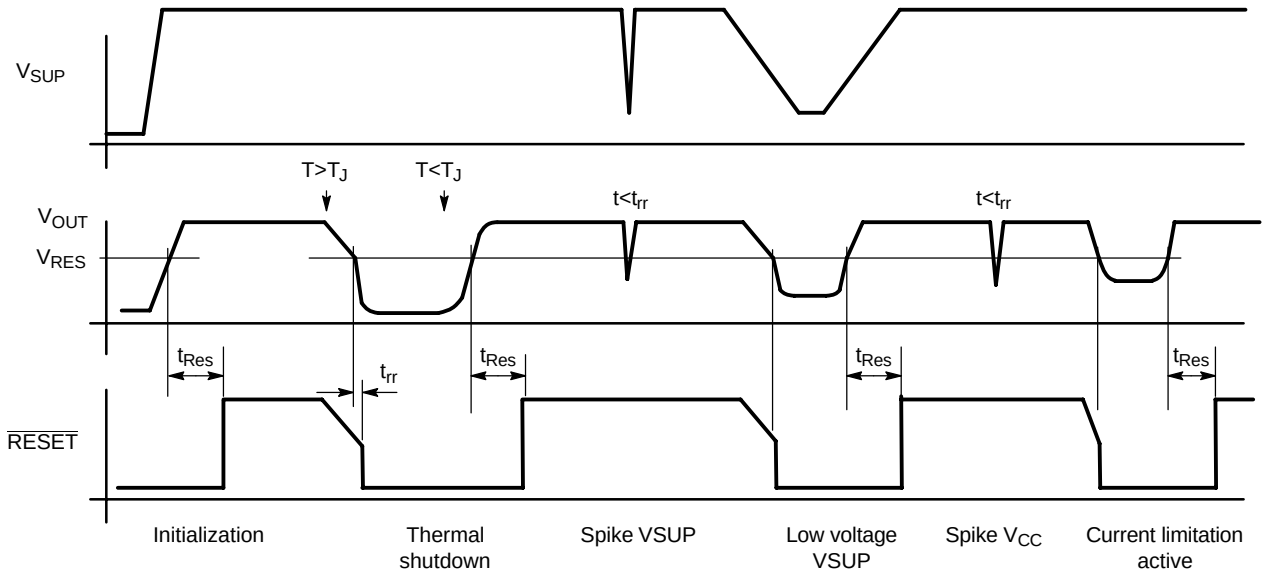


Figure 16. $\overline{\text{RESET}}$ Behavior

If V_{OUT} drops below V_{RES}, the $\overline{\text{RESET}}$ output goes from high to low after t_{rr}. Short transients will be filtered.

The $\overline{\text{RESET}}$ output driver is driven from V_{OUT} to guarantee proper operation.

Initialization

The initialization is started if V_{SUP} is switched on. This is independent of the EN pin.

VSUP−Power ON

The NCV7361 starts in the normal mode when V_{SUP} is applied [>3.15 V (typ)]. The internal circuitry on V_{OUT} as well as the internal regulator starts the initialization with power−on−reset. The voltage regulator is switched on.

If $V_{OUT} > V_{POR}$ the bus−interface will be activated.

If V_{OUT} is higher than V_{Res}, the reset time t_{Res} = 100 ms is started. After t_{Res} the $\overline{\text{RESET}}$ output switches from low to high (see Figure 16).

The initialization procedure at power on is started independent from the EN state. The regulator can only be turned off with a high level followed by a low level on the EN pin.

Mode Input EN

The NCV7361 is switched into the sleep mode when EN goes from high to low. The normal mode will be kept as long as EN = high.

The regulator can be turned off by switching EN high to low independent of the state of the bus−transceiver.

The EN input is internally pulled down to guarantee a low with no connection. In the high state, the pulldown current will be switched off to reduce the quiescent current.

Wake−Up

If the regulator is in a standby (sleep) mode, it can be woken up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 25 μs switches on the regulator.

After the BUS wake−up for the regulator, it can only be turned off with a high level followed by a low level on the EN pin.

Overtemperature Shutdown

The thermal shutdown threshold is $155°C < T_j < 175°C$. When exceeded, the overtemperature shutdown will be active and the regulator voltage will be switched off. V_{OUT} drops down, the reset state is entered and the bus−transceiver is switched off (recessive state).

After T_j falls below 140°C, the NCV7361 will be initialized (see Figure 16), independent from the voltage levels on EN and BUS. Within the thermal shutdown mode, the transceiver can't be switched to the normal mode with local or with remote wake−up.

Function of the NCV7361 is possible between T_{Amax} (125°C) and the switch off temperature, but small parameter differences can appear.

After overtemperature switch−off the IC behaves as described in the $\overline{\text{RESET}}$ chapter.

APPLICATION HINTS

LIN System Parameter

Bus Loading Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{BAT}	8.0	−	18	V
Voltage Drop of Reverse Protection Diode	V_{Drop_rev}	0.4	0.7	1.0	V
Voltage Drop at the Series Diode in Pull Up Path	$V_{SerDiode}$	0.4	0.7	1.0	V
Battery Shift Voltage	V_{Shift_BAT}	0	−	0.1	V_{BAT}
Ground Shift Voltage	V_{Shift_GND}	0	−	0.1	V_{BAT}
Master Termination Resistor	R_{master}	900	1000	1100	Ω
Slave Termination Resistor	R_{slave}	20	30	60	kΩ
Number of System Nodes	N	2	−	16	−
Total Length of Bus Line	LEN_{BUS}	−	−	40	m
Line Capacitance	C_{LINE}	−	100	150	pF/m
Capacitance of Master Node	C_{Master}	−	220	−	pF
Capacitance of Slave Node	C_{Slave}	−	220	250	pF
Total Capacitance of the Bus including Slave and Master Capacitance	C_{BUS}	1.0	4.0	10	nF
Network Total Resistance	$R_{Network}$	537	−	863	Ω
Time Constant of Overall System	τ	1.0	−	5.0	μs

Recommendations for System Design

The goal of the LIN physical layer standard is to have a universal definition of the LIN system for plug and play solutions in LIN networks up to 20 kbd bus speeds.

In case of small and medium LIN networks, it's recommended to adjust the total network capacitance to at least 4.0 nF for good EMC and EMI behavior. This can be done by setting only the master node capacitance. The slave node capacitance should have a unit load of typically 220 pF for good EMC/EMI behavior.

In large networks with long bus lines and the maximum number of nodes, some system parameters can exceed the defined limits and the LIN system designer must intervene.

The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally, there is the capacitance of wires and connectors, and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent on the technology of the IC manufacturer and should be in the range of 30 pF to 150 pF. If the bus lines have a total length of nearly 40m, the total bus capacitance can exceed the LIN system limit of 10 nF.

A second parameter of concern is the integrated slave termination resistor tolerance. If most of the slave nodes have a slave termination resistance near by the allowed maximum of 60 kΩ, the total network resistance is more than 700 Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10 nF, the network time constant is higher than 7.0 μs.

This problem can be solved only by adjusting the master termination resistor to the required maximum network time constant of 5.0 μs (max).

The LIN bus output driver of the NCV7361 provides a higher drive capability than necessary (40 mA @ 1.2 V) within the LIN standard (33.6 mA @ 1.2 V). With this driver stage the system designer can increase the maximum LIN networks with a total network capacitance of more than 10 nF. The total network resistance can be decreased to:

$$R_{tl\_min} = (V_{Bat\_max} - V_{BUSdom})/I_{BUS\_max}$$
$$= (18\ V - 1.2\ V)/40\ mA = 420\ \Omega$$

NOTE: The NCV7361 meets the requirements for implementation in RC−based slave nodes. The LIN Protocol Specification requires the deviation of the slave node clock to the master node clock after synchronization must not differ by more than ±2%.

Setting the network time constant is necessary in large networks (primary resistance) and also in small networks (primary capacitance).

MIN/MAX SLOPE TIME CALCULATION

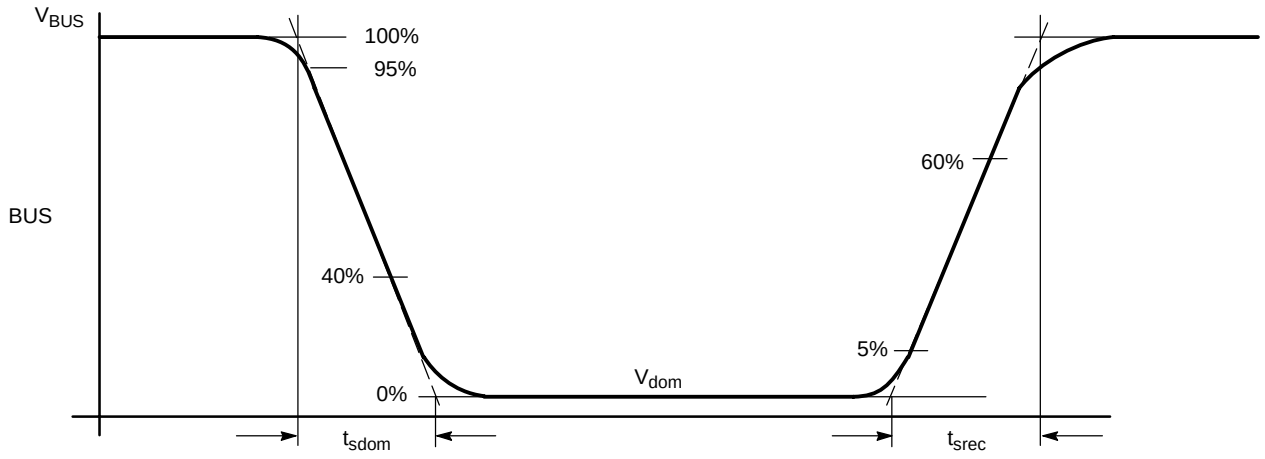


Figure 17. Slope Time Calculation

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2 * V_{swing}/(t_{40\%}-t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%}-t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing}/dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

Power Dissipation and Operating Range

The max power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.

The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{OUT}) * I_{VOUT} + P_{D\_TX}$$

The power dissipation of the transmitter P_{D_TX} depends on the transceiver configuration and its parameters as well as on the bus voltage $V_{BUS} = V_{BAT} - V_D$, the resulting termination resistance R_L, the capacitive bus load C_L and the bit rate. Figure 18 shows the dependence of power dissipation of the transmitter as function of VSUP. The conditions for calculation the power dissipation was: R_L = 500 Ω, C_L = 10 nF, Bitrate = 20 kbit and duty cycle on TxD of 50%.

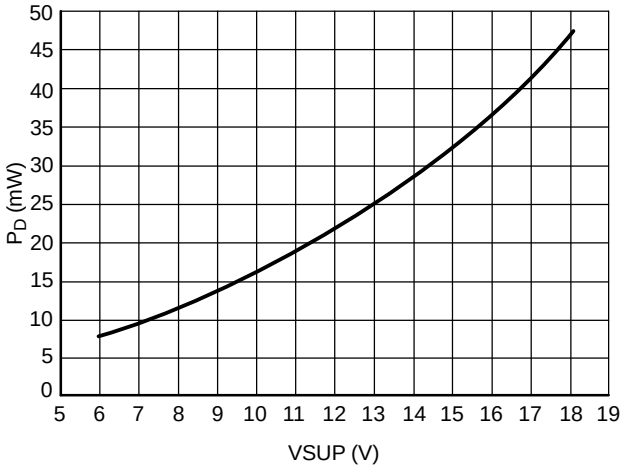


Figure 18. Power Dissipation LIN Transceiver @ 20 kbit

The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_J - T_A}{R_{\theta J-A}}$$

If we consider that $P_{D\_TX\_max}$ = f(VSUP), it can be calculated the max output current IV_{OUT} on V_{OUT}:

$$I_{VOUTmax} = \frac{\frac{T_J-T_A}{R_{\theta J-A}} - P_{D\_TX\_max} @ VSUP}{VSUP - VOUT}$$

T_J−T_A is the temperature difference between junction and ambient, and R_{th} is the thermal resistance of the package. The thermal energy is transferred via the package and the pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

Table 1. SO−8 Thermal RC Network Models*

Copper Area (1 oz thick)			54 mm²	714 mm²		54 mm²	714 mm²	
(SPICE Deck Format)			Cauer Network			Foster Network		
			54 mm²	714 mm²	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	**1.08E−05**	**1.08E−05**	W−s/C	1.00E−06	1.00E−06	sec
C_C2	**node1**	**Gnd**	**4.10E−05**	**4.10E−05**	W−s/C	1.00E−05	1.00E−05	sec
C_C3	**node2**	**Gnd**	**1.13E−04**	**1.13E−04**	W−s/C	1.00E−04	1.00E−04	sec
C_C4	**node3**	**Gnd**	**4.42E−04**	**4.40E−04**	W−s/C	5.00E−04	5.00E−04	sec
C_C5	**node4**	**Gnd**	**1.74E−03**	**1.71E−03**	W−s/C	1.00E−03	1.00E−03	sec
C_C6	**node5**	**Gnd**	**1.39E−03**	**1.34E−03**	W−s/C	1.00E−02	1.00E−02	sec
C_C7	**node6**	**Gnd**	**2.08E−02**	**1.78E−02**	W−s/C	1.00E−01	1.00E−01	sec
C_C8	**node7**	**Gnd**	**1.08E−02**	**9.75E−03**	W−s/C	1.00E+00	1.00E+00	sec
C_C9	node8	Gnd	1.14E−01	1.84E−01	W−s/C	1.00E+01	1.00E+01	sec
C_C10	node9	Gnd	8.11E−01	3.00E+00	W−s/C	5.00E+01	5.00E+01	sec
						R's	**R's**	
R_R1	**Junction**	**node1**	**0.119**	**0.119**	C/W	0.070	0.070	C/W
R_R2	**node1**	**node2**	**0.286**	**0.286**	C/W	0.152	0.152	C/W
R_R3	**node2**	**node3**	**0.857**	**0.859**	C/W	0.481	0.481	C/W
R_R4	**node3**	**node4**	**1.181**	**1.189**	C/W	0.690	0.690	C/W
R_R5	**node4**	**node5**	**1.241**	**1.276**	C/W	0.584	0.584	C/W
R_R6	**node5**	**node6**	**2.574**	**2.690**	C/W	3.223	3.223	C/W
R_R7	**node6**	**node7**	**18.065**	**21.708**	C/W	0.823	0.823	C/W
R_R8	**node7**	**node8**	**27.965**	**26.035**	C/W	26.801	35.166	C/W
R_R9	node8	node9	80.896	49.821	C/W	63.710	52.538	C/W
R_R10	node9	Gnd	49.468	15.252	C/W	86.119	25.510	C/W

*Bold face items in the tables above represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

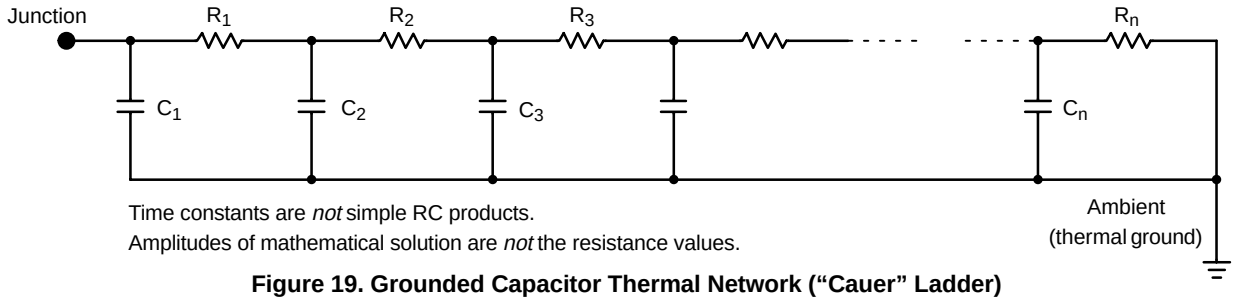


Figure 19. Grounded Capacitor Thermal Network ("Cauer" Ladder)

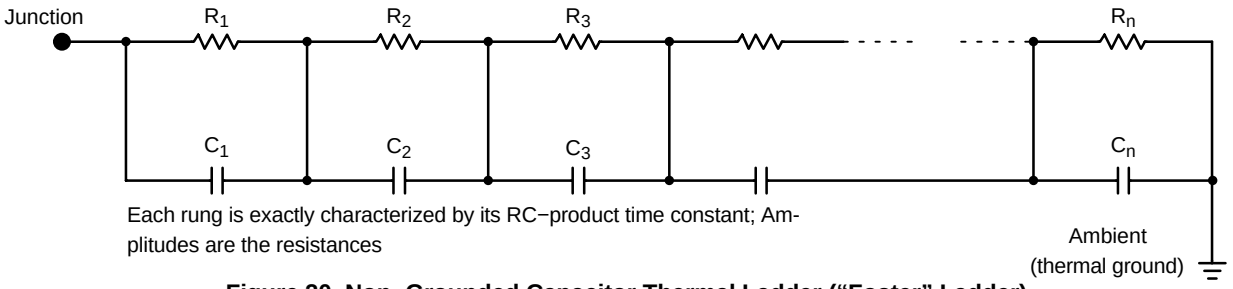


Figure 20. Non−Grounded Capacitor Thermal Ladder ("Foster" Ladder)

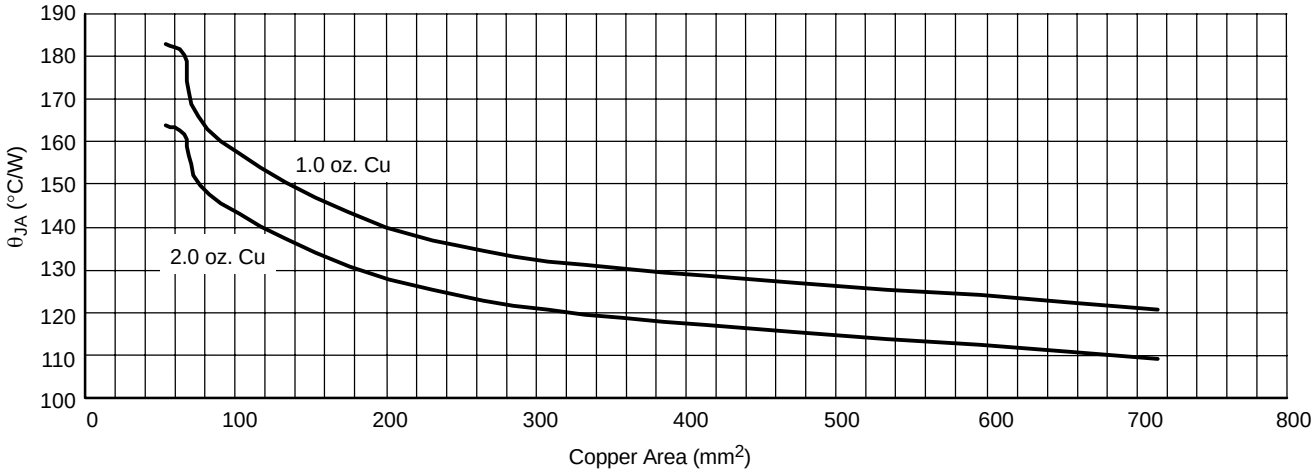


Figure 21. SO−8, θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

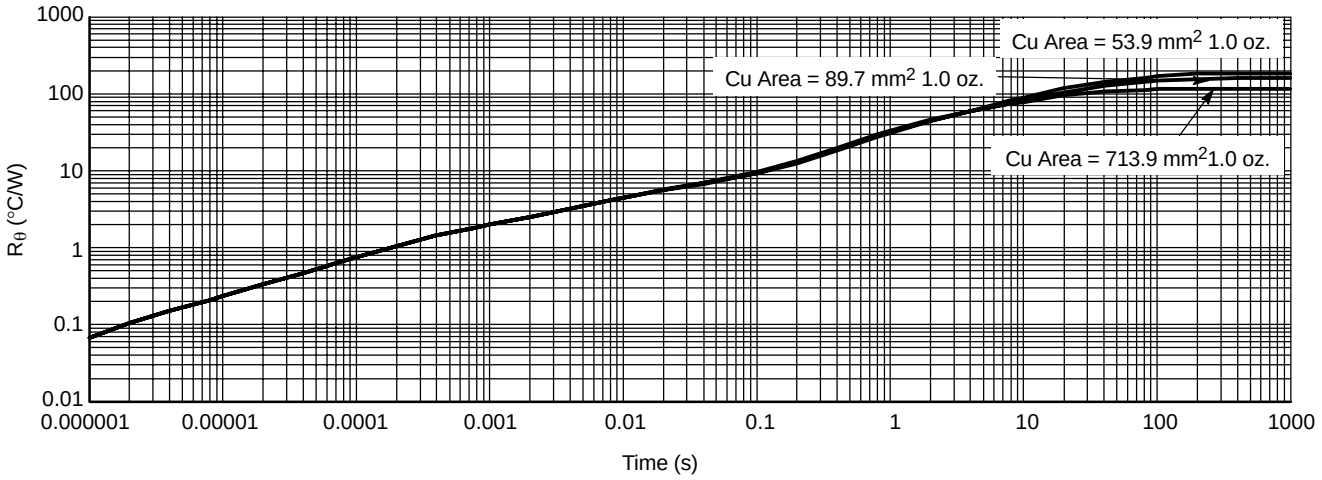


Figure 22. SO−8 Thermal Transient Response on Typical Test Boards

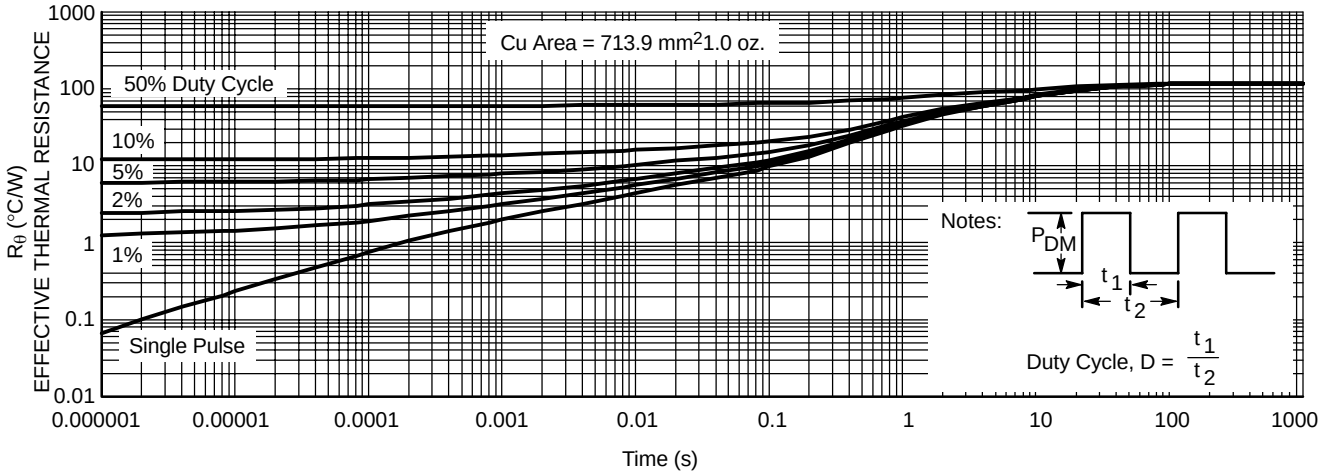


Figure 23. SO−8 Thermal Duty Cycle Curves on 1.0 in. Spreader Test Board

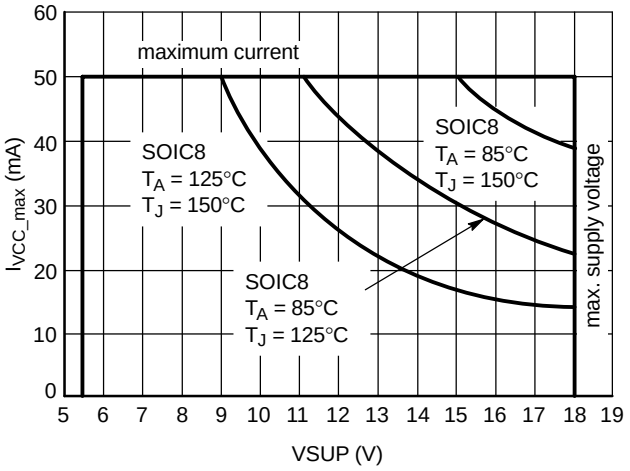


Figure 24. Safe Operating Area

The linear regulator of the NCV7361 operates with input voltages up to 18 V and can output a current of 50 mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 50 mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between VSUP and V_{CC}. See Figure 24 for safe operating areas for different ambient and junction temperatures.

Regulator Circuitry

V_{OUT}

The linear regulator needs a minimum load capacity of 4.7 μF connected to V_{OUT} for stable operating within the whole operating area.

The choice of type and dimension of the load capacity must be done from the application point of view (e.g. Tantalum 10 μF). Essential parameters are the switch on time of V_{OUT} and the load regulation.

Small capacity values should not be combined with small ESR values to avoid stability problems.

V_{SUP}

The capacitors connected to the V_{SUP} pin influence the regulation behavior, especially the line regulation and load regulation.

Big capacitor values improve the line regulation and in parallel with a ceramic capacitor archive good disturbance suppression.

V_{OUT} Load Capacitance

The regulator output V_{OUT} requires a minimum capacitor load of 4.7 μF. To insure stability, the capacitor ESR should fall in the stable region shown in the graph below. The use of tantalum capacitors is recommended. Tantalum capacitors exhibit low variance of capacitance and ESR required in most automotive applications.

The two examples below highlight typical capacitors available on the market.

Example 1:

The regulator is stablized using a 47 μF aluminum electrolytic capacitor load (ESR = 0.7 Ω @ 25°C). The capacitance decreases to 42 μF and the ESR increases to 8.9 Ω at an ambient temperature of −40°C. The ESR value is located in the unstable region. The regulator will be unstable at −40°C.

Example 2:

The regulator is stablized using a 47 μF tantalum capacitor load (ESR = 0.1 Ω @ 25°C). The capacitance decreases to 45 μF and the ESR increases to 0.11 Ω at an ambient temperature of −40°C. The ESR value is located in the stable region. The regulator will be stable at −40°C.

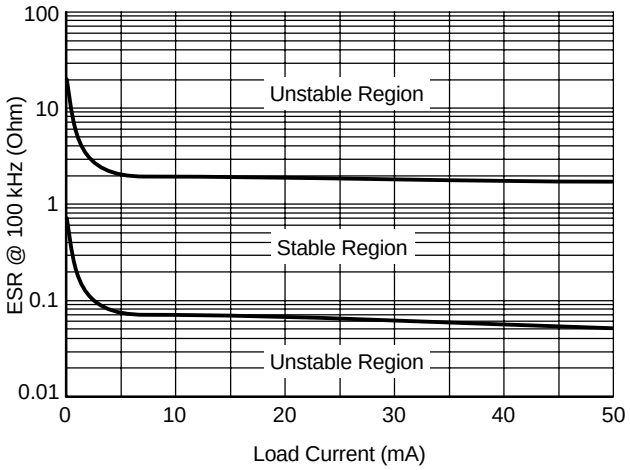


Figure 25. ESR Curves for 6.8 μF ≤ C_L ≤ 100 μF and Frequency of 100 kHz

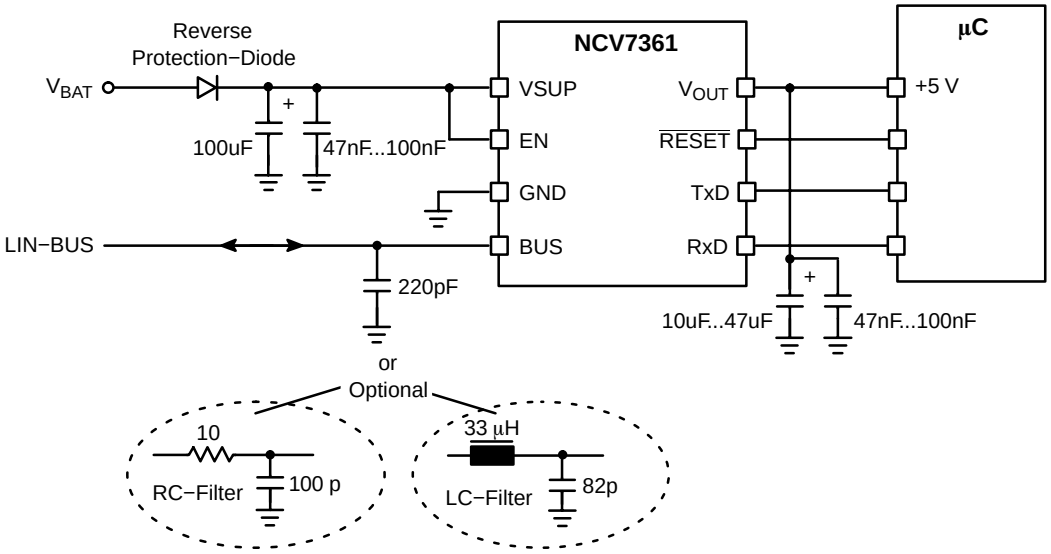


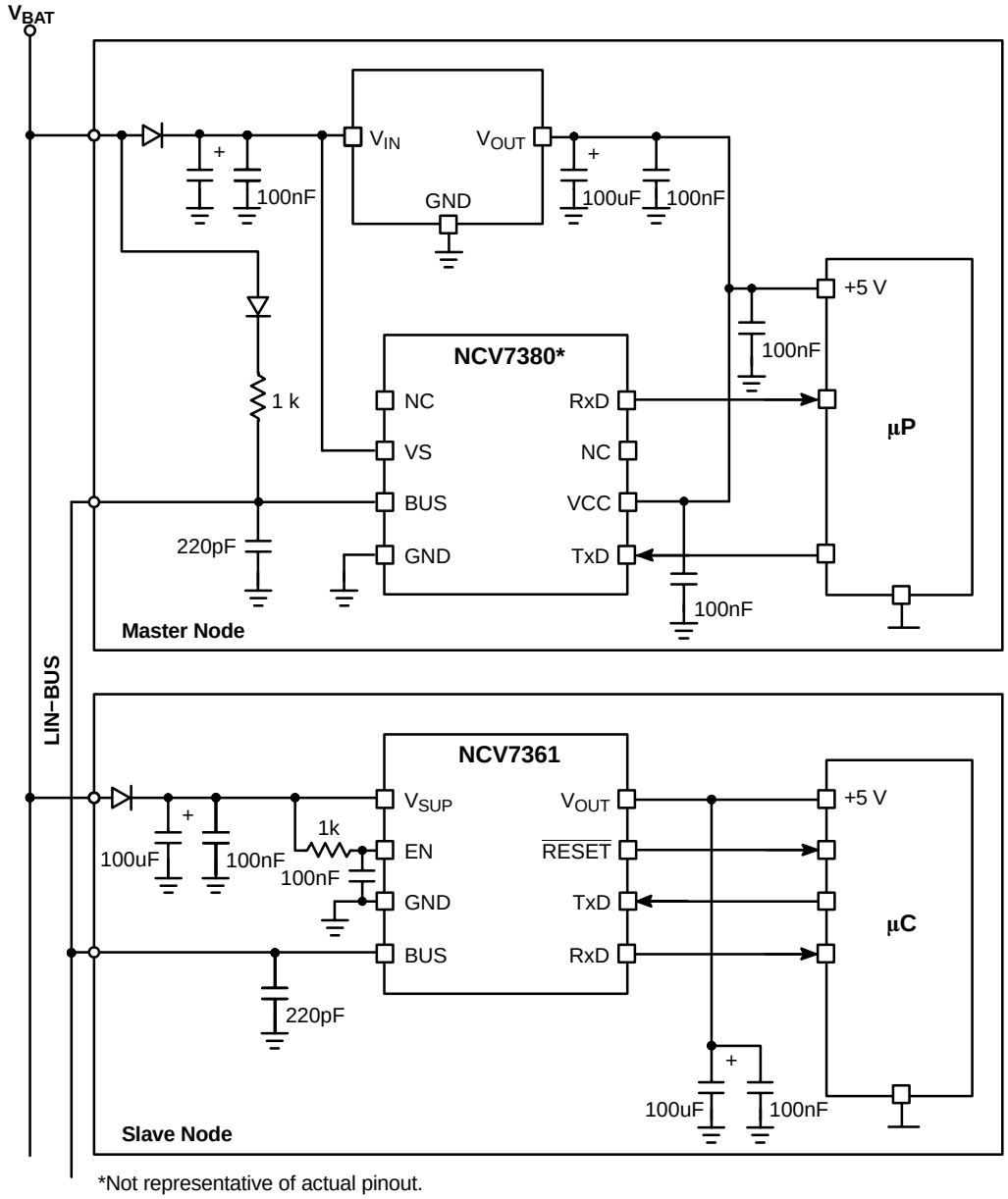
Figure 26. Application Circuit (Slave Node)

EMI Suppressing

To minimize the influence of EMI from the bus line, a 220 pF capacitor should be directly connected to the BUS pin (see Figure 26).

The value of the filter capacity can be adjusted to the size of the LIN network. 220 pF should be used for bigger networks. Values from 333 pF up to 1.0 nF should be used for middle to small LIN networks. Finally the size of the filter capacitor influences the effectiveness of the EMI suppressing in conformance to the maximum LIN bus capacity of 10 nF.

LC− or RC−filters can also be used. The value of C, L or R, depends on the corner frequency, the maximum LIN bus capacity (10 nF) and the compliance with the DC− and AC LIN bus parameters.



*Not representative of actual pinout.

Figure 27. Application Circuit for LIN Sub−Bus with NCV7361 as Slave Node

Connection to Flash−MCU

During programming of a flash MCU the NCV7361 should be disconnected from the MCU. This can be done by disconnecting the supply voltage of the NCV7361 or by turning off the NCV7361 with the EN pin. A blocking diode must be used between the MCU and the RxD pin to avoid loading of the programming data.

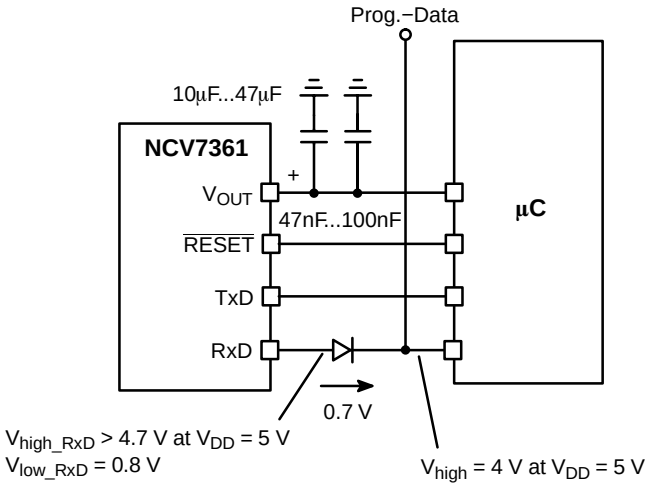


Figure 28. Example Circuitry for Connection of RxD to MCU for Flash Programming

Operating During Disturbance

Operating Without V_{SUP} or GND

The BUS pin is designed for voltages of GND − 24 V up to GND + 30 V. This helps to prevent loss of communication between other bus nodes with the loss of VSUP or loss of GND. The BUS pin will remain at V_{BAT} and current draw will be minimal with the loss of GND or VSUP.

Short Circuit BUS to V_{BAT}

- Recessive LIN bus is blocked, no influence to the NCV7361
- Dominant Current limit, thermal shutdown of NCV7361

Short Circuit BUS to GND

The LIN bus is blocked. There is no influence to the NCV7361.

Short Circuit TxD to GND

The LIN transceiver is permanent in the dominant state as is the LIN bus. This state can only be detected from the LIN controller. In this case the controller must switch off the LIN node via the EN input of the NCV7361 and look for a recessive state. A thermal shutdown of NCV7361 will appear if the thermal shutdown threshold is broken.

TxD Open

The internal pullup resistor forces the LIN node to the recessive state. The communication between the other bus−nodes will not be disturbed.

Short Circuit V_{OUT} to GND

The V_{OUT} pin is protected via a current limit. This state is comparable with the behavior in the sleep mode.

Overload of V_{OUT}

Thermal Switch Off

The power dissipation is increasing if the load current is between IV_{OUT_max} and I_LV_{OUT}. If the IC exceeds the thermal shutdown threshold, the transceiver will be switched off. The voltage regulator will also be switched off and a reset signal is forced.

Overcurrent

If the current limit is active the voltage on V_{OUT} drops down. If this voltage is below the threshold $V_{RES,}$ a reset will be forced.

Undervoltage V_{SUP}, V_{OUT}

The reset circuit guarantees the correct behavior of the driver during undervoltage. The BUS pin generates the recessive state if $V_{OUT} < V_{POR}$. The inputs EN and TxD have pull−down and pull−up circuits respectively.

If $V_{POR} \leq V_{OUT} \leq 4.5$ V the TxD signal is transmitted to the bus. The receive mode is also active.

Short Circuit RxD, RESET to GND or V_{OUT}

Both outputs are short circuit proof to V_{OUT} and ground.

ESD/EMC Remarks

General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

ESD Test

The NCV7361 is tested according to MIL883D (Human Body Model).

EMC

The test on EMC impacts is done according to ISO 7637−1 for power supply pins and ISO 7637−3 for data and signal pins.

POWER SUPPLY PIN V_{SUP}

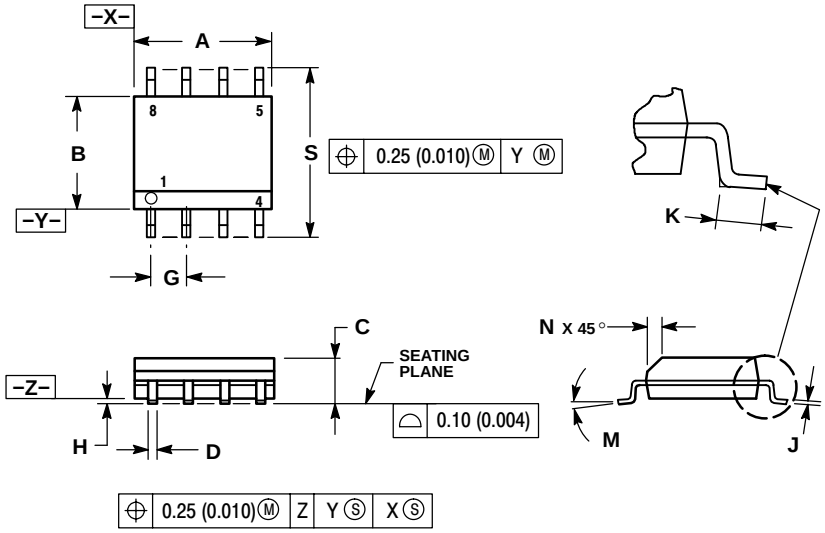
Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	5000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	5000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1 h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms/U_P + U_S = 40 V	10 Pulses Every 1 Min

DATA AND SIGNAL PINS EN, BUS

Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	1000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	1000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1000 Burst

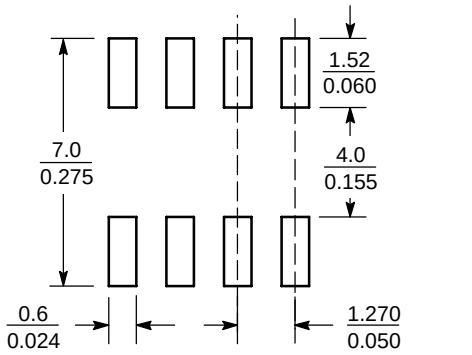
PACKAGE DIMENSIONS

SOIC−8 NB
D SUFFIX
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

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