

# NCV7462

## LIN/CAN SBC/System-IC

The NCV7462 is a monolithic LIN/CAN System-Basis-Chip with enhanced feature set useful in Automotive Body Control systems. Besides the bus interfaces the IC features two 5 V voltage regulators, high-side and low-side switches to control LED's and relays, and supervision functionality like a window watchdog. This allows a highly integrated solution by replacing external discrete components while maintaining the system flexibility. As a consequence, the board space and ECU weight can be minimized.

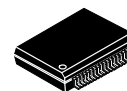
### Features

- Main Supply Functional Operating Range from 5 V to 28 V
- Main Supply Parametrical Operating Range 6 V to 18 V
- CAN High Speed Transceiver Compliant to ISO11898
- TxD Time-out on CAN
- LIN Physical Layer According to LIN 2.x and SAEJ2602
- Programmable TxD Time-out on LIN
- Power Management Through Operating Modes: Normal, Standby, Sleep and Flash
- Low Drop Voltage Regulator VR1: 5 V / 250 mA,  $\pm 2\%$  Output Tolerance
- Reverse Current Protected Low Drop Voltage Regulator VR2: 5 V / 50 mA,  $\pm 2\%$  Output Tolerance
- 3x Wake-up Inputs, e.g. For Contact Monitoring
- Wake-up Logic with Cyclic Contact Monitoring
- Wake-up Source Recognition
- Independent PWM Functionality for All Outputs (integrated PWM registers)
- Window Watchdog with Programmable Times
- 2x Low-Side Driver (typ. 3  $\Omega$ ) with Over-load Protection and Active Clamp; e.g. for Relays
- 1x High-Side Driver (typ. 1  $\Omega$ ) with Over- and Under-load Detection and Auto-Recovery; e.g. for Bulbs, LED's and Switches
- 1x High-Side Driver (Selectable Between Typ. 2  $\Omega$  and 7  $\Omega$ ) with Over- and Under-load Detection; e.g. for LED's and Switches
- 3x High-Side Driver (typ. 7  $\Omega$ ) with Over- and Under-load Detection; e.g. for LED's and Switches
- 2x Operational Amplifier for Current Sensing
- 24-Bit SPI Interface
- Protection Against Short Circuit, Over-voltage and Over-temperature
- SSOP36-EP Package
- AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



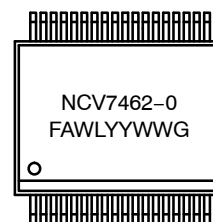
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SSOP36-EP  
DQ SUFFIX  
CASE 940AB

### MARKING DIAGRAM



NCV7462-0 = Specific Device Code  
F = Fab Location  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information on page 54 of this data sheet.

### Typical Applications like

- De-centralized Door Electronic Systems
- Body Control Units (BCUs)
- Climate Control Systems

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## BLOCK DIAGRAM

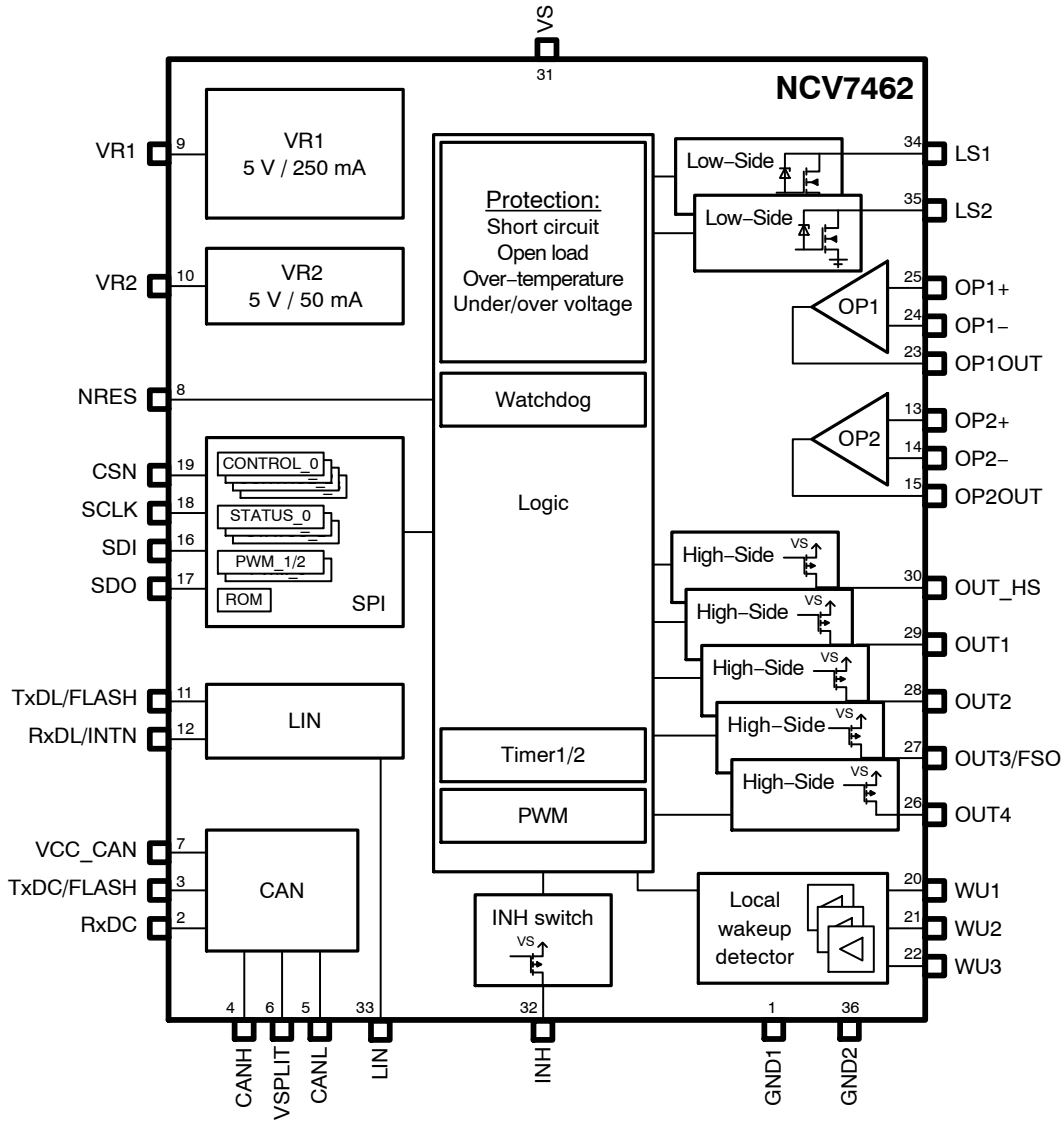


Figure 1. Block Diagram

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## PIN-OUT

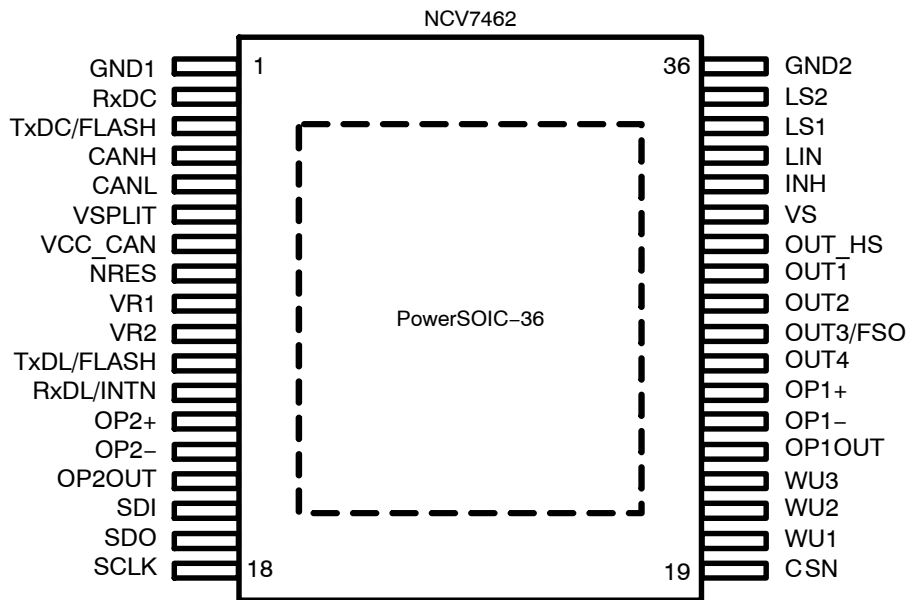


Figure 2. Package Pin-out

Table 1. PIN DESCRIPTION

| Pin # | Pin Name   | Description                                     | Comment  |
|-------|------------|---|--|
| 1     | GND1       | Ground  | Ground connection  |
| 2     | RxDC       | Digital push-pull output                        | Receiver output of the CAN transceiver                           |
| 3     | TxDC/FLASH | Digital input with pull-up                      | Transmitter data input of the CAN transceiver / Flash mode entry |
| 4     | CANH       | CAN bus interface                               | High-level CAN bus line (high during dominant)                   |
| 5     | CANL       | CAN bus interface                               | Low-level CAN bus line (low during dominant)                     |
| 6     | VSPLIT     | HV output                                       | CAN common-mode stabilization pin                                |
| 7     | VCC_CAN    | Supply input                                    | Supply for the CAN transceiver                                   |
| 8     | NRES       | Digital open-drain output with internal pull-up | Reset signal to the MCU  |
| 9     | VR1        | 5V regulator output                             | 2%, 250 mA   |
| 10    | VR2        | 5V regulator output                             | 2%, 50 mA, protected against short to VS                         |
| 11    | TxDL/FLASH | Digital input with pull-up                      | Transmitter data input of the LIN transceiver / Flash mode entry |
| 12    | RxDL/INTN  | Digital push-pull output                        | Receiver output of the LIN transceiver / Interrupt output        |
| 13    | OP2+       | Analog input                                    | Opamp input  |
| 14    | OP2-       | Analog input                                    | Opamp input  |
| 15    | OP2OUT     | HV analog output                                | Opamp output   |
| 16    | SDI        | Digital input with pull-down                    | SPI data input   |
| 17    | SDO        | Digital push-pull output, tristate              | SPI data output  |
| 18    | SCLK       | Digital input with pull-down                    | SPI clock input  |
| 19    | CSN        | Digital input with pull-up                      | SPI chip select input  |
| 20    | WU1        | HV input  | Voltage-sense input (threshold typ. VS/2), switched pull-up/down |
| 21    | WU2        | HV input  | Voltage-sense input (threshold typ. VS/2), switched pull-up/down |

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**Table 1. PIN DESCRIPTION**

| Pin # | Pin Name | Description          | Comment  |
|-------|----------|----------------------|--|
| 22    | WU3      | HV input             | Voltage-sense input (threshold typ. $V_S/2$ ), switched pull-up/down                                     |
| 23    | OP1OUT   | HV analog output     | Opamp output   |
| 24    | OP1-     | Analog input         | Opamp input  |
| 25    | OP1+     | Analog input         | Opamp input  |
| 26    | OUT4     | HS driver            | Resistive loads, $R_{on}$ 7 $\Omega$ typ, $I_{lim}$ > 140 mA   |
| 27    | OUT3/FSO | HS driver            | Resistive loads, $R_{on}$ 7 $\Omega$ typ, $I_{lim}$ > 140 mA / FSO output                                |
| 28    | OUT2     | HS driver            | Resistive loads, $R_{on}$ 7 $\Omega$ typ, $I_{lim}$ > 140 mA   |
| 29    | OUT1     | HS driver            | Resistive loads, $R_{on}$ 2 $\Omega$ /7 $\Omega$ typ, $I_{lim}$ > 250 mA/140 mA (two configurations)     |
| 30    | OUT_HS   | HS driver            | Resistive loads, $R_{on}$ 1 $\Omega$ typ, $I_{lim}$ > 1000 mA  |
| 31    | VS       | Battery supply input | Principle power-supply of the device   |
| 32    | INH      | HS output            | Battery related output to switch off the LIN master resistor or to control an external voltage regulator |
| 33    | LIN      | LIN bus interface    | LIN bus pin, low in dominant state   |
| 34    | LS1      | LS driver            | Relay driver, $R_{on}$ 3 $\Omega$ typ, $I_{lim}$ > 250 mA, active clamp to ground                        |
| 35    | LS2      | LS driver            | Relay driver, $R_{on}$ 3 $\Omega$ typ, $I_{lim}$ > 250 mA, active clamp to ground                        |
| 36    | GND2     | Ground/test pin      | Ground connection in the application / test pin in the production  |

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## APPLICATION CIRCUIT

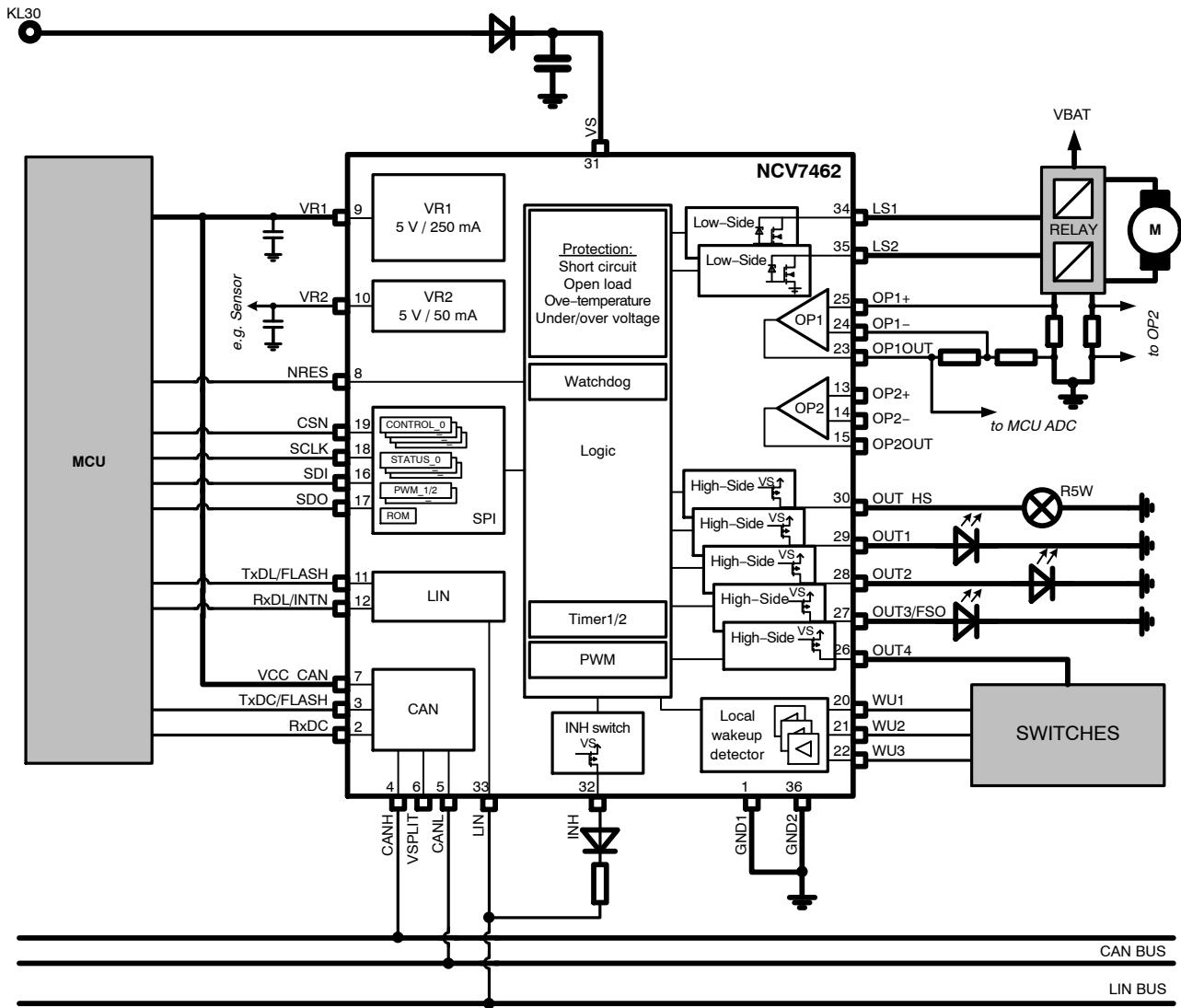


Figure 3. Application Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

| Symbol   | Parameter   | Min  | Max                    | Unit |
|--|---|------|------------------------|------|
| Vmax_VS  | Power supply voltage  | -0.3 | 40                     | V    |
| Vmax_WU1-3   | Wake pins DC and transient voltage  | -0.3 | VS + 0.3               | V    |
| Vmax_OPOUT1/2  | Opamp analog output voltage range   | -0.3 | VS + 0.3               | V    |
| Vmax_OUT1-4<br>Vmax_OUT_HS                                   | High-side output voltage range  | -0.3 | VS + 0.3               | V    |
| Vmax_LS1/2   | LS1/2 pin voltage range DC  | -0.3 | 40                     | V    |
|  | LS1/2 pin transient voltage range (during flyback)  | -0.3 | 65                     | V    |
| Vmax_LIN   | DC voltage on LIN pin   | -20  | 40                     | V    |
| Vmax_INH   | DC voltage on INH pin   | -0.3 | VS + 0.3               | V    |
| Vmax_CANH/L<br>Vmax_VSPLIT                                   | DC voltage on pin CANH, CANL and VSPLIT   | -40  | 40                     | V    |
| Vmax_VR1   | Stabilized supply voltage, logic supply   | -0.3 | min (5.5,<br>VS + 0.3) | V    |
| Vmax_VR2   | Stabilized supply voltage   | -0.3 | 28                     | V    |
| Vmax_VCC_CAN   | Supply input for the CAN transceiver  | -0.3 | 5.5                    | V    |
| Vmax_digIO   | DC voltage at digital pins (RxDC, NRES, RxDL/INTN, SDI, SDO, SCLK, CSN)   | -0.3 | VR1 + 0.3              | V    |
| Vmax_OP1/2(+/-)  | Opamp input voltage range   | -0.3 | VS + 0.3               | V    |
| Vmax_TxDL(C)/FLASH   | DC voltage at TxDL/FLASH and TxDC/FLASH inputs  | -0.3 | 28                     | V    |
| Wmax_LS1/2   | Maximum clamping energy on LS1/2  |      | 36                     | mJ   |
| Imax_LS1/2   | Maximum LS1/2 pin current   |      | 500                    | mA   |
|  | Maximum LS1/2 pin current, transient or without VS supply   | -120 |                        | mA   |
| Imax_input   | Current injection into Vs related input pins  |      | 5                      | mA   |
| ESD Human Body Model<br>(100pF, 1500Ω)                       | All pins  | -2   | +2                     | kV   |
|  | Pins LIN, CANH/L, VSPLIT and WU1-3 to GND   | -4   | +4                     |      |
|  | Pins OUT_HS, OUT1-4, LS1/2 to GND   | -4   | +4                     |      |
| ESD following IEC 61000-4-2<br>(150 pF, 330 Ω)               | Valid for pins VS, LIN, CANH/L, VSPLIT, WUx, OUT_HS, OUT1-4<br>- VS pin with reverse-protection and filtering capacitor<br>- VSPLIT pin stressed through split CAN termination<br>- WUx pins stressed through a serial resistor >10 kΩ<br>- OUT_HS, OUT1-4 pins with parallel capacitor 10 nF | -6   | +6                     | kV   |
| ESD Charged Device Model following JESD22-C101/AE C-Q100-011 | All pins  | -500 | +500                   | V    |
|  | Corner pins   | -750 | +750                   | V    |
| Tj_mr  | Junction temperature  | -40  | +170                   | °C   |
| Tstg   | Storage Temperature Range   | -55  | +150                   | °C   |
| MSL  | Moisture Sensitivity Level (max. 260°C processing)  | MSL3 |                        |      |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. RECOMMENDED OPERATING CONDITIONS**

| Symbol                   | Parameter  | Min    | Max      | Unit   |
|--------------------------|--|--------|----------|--------|
| Vop_VS_par               | Power supply voltage for valid parameter specifications                                | 6      | 18       | V      |
| Vop_VS_func              | Power supply for correct functional behavior   | 5      | 28       | V      |
| Vop_WU1-3                | Wake DC and transient voltage  | 0      | VS       | V      |
| Vop_OPOUT1/2             | Opamp analog output voltage range  | 0      | VS       | V      |
| Vop_OUT1-4<br>Vop_OUT_HS | High-side output voltage range   | 0      | VS       | V      |
| Vop_LS1/2                | LS1/2 pin voltage range DC<br>LS1/2 pin transient voltage range (during flyback)       | 0<br>0 | VS<br>65 | V<br>V |
| Vop_LIN<br>Vop_INH       | LIN and INH pin voltage range  | 0      | VS       | V      |
| Vop_CANH/L<br>Vop_VSPLIT | DC voltage on pin CANH, CANL and VSPLIT  | 0      | VCC_CAN  | V      |
| Vop_VR1                  | Stabilized supply voltage  | 4.9    | 5.1      | V      |
| Vop_VR2                  | Stabilized supply voltage  | 4.9    | 5.1      | V      |
| Vop_VCC_CAN_normal       | Supply input for the CAN transceiver for normal operation (transmission and reception) | 4.75   | 5.25     | V      |
| Vop_VCC_CAN_lowpower     | Supply input for the CAN transceiver for low-power operation (CAN wakeup detection)    | 0      | 5.25     | V      |
| Vop_digIO                | DC voltage at digital pins (RxDC, NRES, RxDL/INTN, SDI, SDO, SCLK, CSN)                | 0      | VR1      | V      |
| Vop_OP1/2(+/-)           | Opamp input voltage range  | -0.2   | 3        | V      |
| Vop_TxDL(C)/FLASH        | DC voltage at TxDL/FLASH and TxDC/FLASH inputs   | 0      | 18       | V      |
| Tj_op                    | Junction temperature   | -40    | +150     | °C     |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 4. THERMAL CHARACTERISTICS**

| Symbol                    | Parameter                              | Test Condition | Min              | Typ | Max | Unit |
|---------------------------|--|----------------|------------------|-----|-----|------|
| <b>THERMAL PROTECTION</b> |  |                |                  |     |     |      |
| Tjw                       | Thermal warning level                  |                | 120              | 130 | 140 | °C   |
| Tjw_hys                   | Thermal warning hysteresis             |                |                  | 5   |     | °C   |
| Tjwd1                     | Thermal shut-down level 1              |                | 130              | 140 | 150 | °C   |
| Tjwd1_hys                 | Thermal shut-down 1 hysteresis         |                |                  | 5   |     | °C   |
| Tjwd2                     | Thermal shut-down level 2              |                | 140              | 155 | 170 | °C   |
| Tjwd2_hys                 | Thermal shut-down 2 hysteresis         |                |                  | 5   |     | °C   |
| <b>THERMAL RESISTANCE</b> |  |                |                  |     |     |      |
| Rth_jc                    | Thermal resistance junction-to-case    |                |                  | 3.5 |     | °C/W |
| Rth_ja                    | Thermal resistance junction-to-ambient |                | see figure below |     |     | °C/W |

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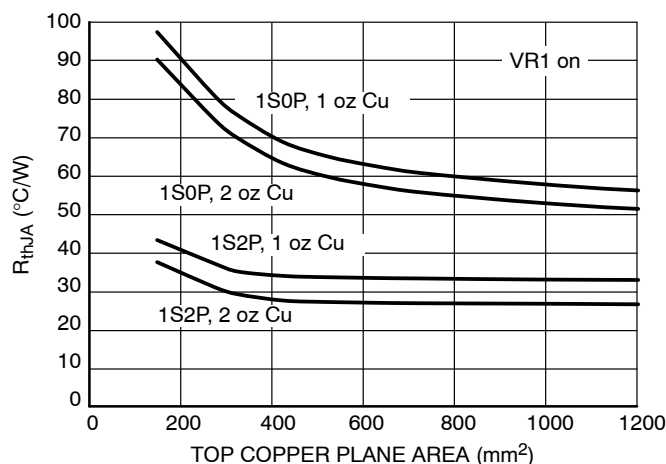


Figure 4. Thermal Resistance Junction-to-Ambient

## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

Table 5. VS SUPPLY

| Symbol        | Parameter  | Test Condition  | Min  | Typ                          | Max  | Unit |
|---------------|--|---|------|------------------------------|------|------|
| VS            | Supply Voltage                                     | Functional Voltage regulators with deteriorated performance   | 5    |                              | 28   | V    |
|               |  | Parameter specification   | 6    |                              | 18   |      |
| VS_POR        | VS POR threshold                                   |   | 2.8  | 3.45                         | 4.1  | V    |
| VS_UV         | VS UV-threshold voltage                            |   | 5.11 |                              | 5.81 | V    |
| VS_UV_hyst    | Undervoltage hysteresis                            |   | 0.04 | 0.1                          | 0.2  | V    |
| VS_OV         | VS OV-threshold voltage                            |   | 20   |                              | 22   | V    |
| VS_OV_hyst    | Overvoltage hysteresis                             |   | 0.5  | 1                            | 1.5  | V    |
| I_VS_sleep    | VS consumption in sleep mode                       | Sleep mode<br>VS = 12 V, VR1/2 are off, bus communication off<br>No wake-up request pending, OUTx = floating<br>T <sub>J</sub> = 85°C (Note 1)  | 10   | 30                           | 60   | μA   |
| I_VS_sleep_cs | VS consumption in sleep mode (with cyclic sense)   | Sleep mode<br>VS = 12 V, VR1/2 are off, bus communication off<br>T2_PER = 50 ms, T2_TON = 100 μs<br>No wake-up request pending<br>T <sub>J</sub> = 85°C (Note 1)  | 40   | 70                           | 130  | μA   |
| I_VS_stdby    | VS consumption in standby mode                     | Standby mode<br>VS = 12 V, VR1 not loaded, VR2 off<br>VR1 current comparator enabled<br>OUTx = floating<br>Bus communication off, no cyclic sensing<br>No wake-up request pending<br>T <sub>J</sub> = 85°C (Note 1) | 30   | 70                           | 80   | μA   |
| I_VS_stdby_cs | VS consumption in standby mode (with cyclic sense) | Standby mode<br>VS = 12 V, VR1 not loaded, VR2 off<br>VR1 current comparator enabled<br>T2_PER = 50 ms, T2_TON = 100 μs<br>Bus communication off<br>No wake-up request pending<br>T <sub>J</sub> = 85°C (Note 1)    |      | 100                          |      | μA   |
| I_VS_norm     | VS consumption in normal mode                      | Normal mode<br>VR1/2 are on (unloaded)<br>OUTx = floating, TxD LIN/CAN not active,<br>Opamp outputs not loaded  |      | 4.5                          | 10   | mA   |
| I_VS_add_VR1  | VR1 current consumption from VS                    | Normal/Standby mode, VR1 loaded   |      | 0.011 • I <sub>out_VR1</sub> |      | mA   |
| I_VS_add_VR2  | VR2 current consumption from VS                    | VR2 loaded  |      | 0.013 • I <sub>out_VR2</sub> |      | mA   |

1. Values based on design and characterization, not tested in production.



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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 6. VOLTAGE REGULATOR VR1**

| Symbol        | Parameter                                      | Test Condition  | Min   | Typ  | Max  | Unit |
|---------------|--|---|-------|------|------|------|
| V_VR1         | Regulator output voltage                       | $0\text{ mA} \leq I(\text{VR1}) \leq 250\text{ mA}$ ,<br>$6\text{ V} \leq V_S \leq 27\text{ V}$ | 4.9   | 5    | 5.1  | V    |
| Iout_VR1      | Regulator output current                       |   |       |      | -250 | mA   |
| Ilim_VR1      | Regulator current limitation                   |   | -1000 | -800 | -400 | mA   |
| Vdrop_VR1     | Dropout voltage                                | $I(\text{VR1}) = 100\text{ mA}$ , $V_S = 5\text{ V}$  |       | 0.25 | 0.4  | V    |
|               |  | $I(\text{VR1}) = 100\text{ mA}$ , $V_S = 4.5\text{ V}$  |       | 0.3  | 0.5  |      |
|               |  | $I(\text{VR1}) = 50\text{ mA}$ , $V_S = 4.5\text{ V}$   |       | 0.2  | 0.4  |      |
| Loadreg_VR1   | Load regulation                                | $1\text{ mA} \leq I(\text{VR1}) \leq 50\text{ mA}$  | -30   | 10   | 30   | mV   |
| Linereg_VR1   | Line regulation                                | $I(\text{VR1}) \leq 5\text{ mA}$ ,<br>$6\text{ V} \leq V_S \leq 18\text{ V}$                    | -30   | 10   | 30   | mV   |
| Ttsd_VR1      | VR1 deactivation time after thermal shutdown 2 |   | 0.85  | 1    | 1.15 | s    |
| Cload_VR1     | VR1 load capacitor                             | ESR < 200 mΩ , ceramic recommended  | 1     | 2.2  |      | μF   |
| Icmp_VR1_rise | Current comp. rising threshold                 | VR1 consumption increasing  | 0.7   | 1.7  | 3    | mA   |
| Icmp_VR1_fall | Current comp. falling threshold                | VR1 consumption decreasing<br>$T_J = -40 - 130^{\circ}\text{C}$                                 | 0.5   | 1.1  | 2    | mA   |
| Icmp_VR1_hys  | Current comp. hysteresis                       |   |       | 0.5  |      | mA   |
| Vfail_VR1     | VR1 fail threshold                             | VR1 forced  | 1.7   | 2    | 2.4  | V    |
| Tfail_VR1     | VR1 fail blanking time                         |   |       | 5    | 10   | μs   |
| Tshort_VR1    | VR1 short blanking time                        |   | 3.4   | 4    | 4.6  | ms   |

**Table 7. VOLTAGE REGULATOR VR2**

| Symbol      | Parameter                    | Test Condition   | Min  | Typ  | Max | Unit |
|-------------|------------------------------|--|------|------|-----|------|
| V_VR2       | Output voltage tolerance     | $0\text{ mA} \leq I(\text{VR1}) \leq 50\text{ mA}$ ,<br>$6\text{ V} \leq V_S \leq 18\text{ V}$ | 4.9  | 5    | 5.1 | V    |
| Iout_VR2    | Output current               |  |      |      | -50 | mA   |
| Ilim_VR2    | Short circuit output current |  | -200 | -110 | -80 | mA   |
| Vdrop_VR2   | Dropout voltage              | $I(\text{VR1}) = 30\text{ mA}$ , $V_S = 5\text{ V}$  |      | 0.3  | 0.4 | V    |
| Loadreg_VR2 | Load regulation              | $1\text{ mA} \leq I(\text{VR1}) \leq 50\text{ mA}$   | -30  | 10   | 30  | mV   |
| Linereg_VR2 | Line regulation              | $I(\text{VR1}) \leq 5\text{ mA}$ ,<br>$6\text{ V} \leq V_S \leq 18\text{ V}$                   | -30  | 10   | 30  | mV   |
| Cload_VR2   | Load capacitor               | ESR < 200 mΩ , ceramic recommended   | 0.22 | 1    |     | μF   |
| Vfail_VR2   | VR2 fail threshold           | VR2 forced   | 1.7  | 2    | 2.4 | V    |
| Tfail_VR2   | VR2 fail blanking time       |  |      | 2    | 10  | μs   |
| Tshort_VR2  | VR2 short blanking time      |  | 3.4  | 4    | 4.6 | ms   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 8. VR1 UNDER-VOLTAGE DETECTOR**

| Symbol       | Parameter  | Test Condition     | Min   | Typ | Max   | Unit          |
|--------------|--|--------------------|-------|-----|-------|---------------|
| VR1_RES1     | VR1 Reset threshold 1 (default)                            | SPI VR1_RES.x = 00 | 4.33  | 4.5 | 4.67  | V             |
| VR1_RES2     | VR1 Reset threshold 2                                      | SPI VR1_RES.x = 01 | 4.135 | 4.3 | 4.465 | V             |
| VR1_RES3     | VR1 Reset threshold 3                                      | SPI VR1_RES.x = 10 | 3.69  | 3.9 | 4.16  | V             |
| VR1_RES4     | VR1 Reset threshold 4                                      | SPI VR1_RES.x = 11 | 3.44  | 3.7 | 3.91  | V             |
| Tdel_VR1_RES | Reaction delay between VR1 undervoltage and NRES low pulse |                    | 6     |     | 40    | $\mu\text{s}$ |
| Tflt_VR1_RES | VR1 undervoltage filter time                               |                    |       | 16  |       | $\mu\text{s}$ |
| T_NRES       | NRES pulse length after VR1 undervoltage release           |                    | 1.7   | 2   | 2.3   | ms            |

**Table 9. VCC\_CAN SUPPLY INPUT**

| Symbol          | Parameter                    | Test Condition   | Min | Typ | Max  | Unit          |
|-----------------|------------------------------|--|-----|-----|------|---------------|
| IVCAN_norm_rec  | Consumption from VCC_CAN pin | CAN enabled; normal mode; recessive transmitted<br>$4.75\text{ V} < V_{CC\_CAN} < 5.25\text{ V}$   |     |     | 10   | mA            |
| IVCAN_norm_dom  |                              | CAN enabled; normal mode; dominant transmitted<br>$4.75\text{ V} < V_{CC\_CAN} < 5.25\text{ V}$<br>bus termination $60\ \Omega$  |     |     | 75   | mA            |
| IVCAN_lowpower  |                              | CAN wakeup detector active (supplied from VS); standby or sleep mode; no wakeup detected;<br>$0\text{ V} < V_{CC\_CAN} < 5.25\text{ V}$ ;<br>$T_J = 85^{\circ}\text{C}$ (Note 2) |     |     | 6    | $\mu\text{A}$ |
| Vfail_VCAN      | VCAN undervoltage threshold  |  | 4   | 4.3 | 4.65 | V             |
| Vfail_hyst_VCAN | VCC_CAN hysteresis           | normal mode  |     | 100 |      | mV            |
| Tfail_VCAN      | VCAN fail blanking time      |  |     | 2   | 10   | $\mu\text{s}$ |

2. Values based on design and characterization, not tested in production.

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 10. HIGH-SIDE OUTPUTS (OUT1-4)**

| Symbol             | Parameter   | Test Condition  | Min  | Typ  | Max  | Unit                   |
|--------------------|---|---|------|------|------|------------------------|
| Ron_OUT1_low       | On-resistance to VS, OUT1 in "low-ohmic" configuration                    | $T_J = 25^{\circ}\text{C}$ , $I(\text{OUT1}) = -100\text{ mA}$  |      | 2    |      | $\Omega$               |
|                    |   | $T_J = 125^{\circ}\text{C}$                                     |      |      | 3.3  | $\Omega$               |
| Ron_OUT1_high      | On-resistance to VS, OUT1 in "normal-ohmic" configuration                 | $T_J = 25^{\circ}\text{C}$ , $I(\text{OUT1}) = -60\text{ mA}$   |      | 7    |      | $\Omega$               |
|                    |   | $T_J = 125^{\circ}\text{C}$                                     |      |      | 13   | $\Omega$               |
| Ron_OUT2-4         | On-resistance to VS   | $T_J = 25^{\circ}\text{C}$ , $I(\text{OUT2-4}) = -60\text{ mA}$ |      | 7    |      | $\Omega$               |
|                    |   | $T_J = 125^{\circ}\text{C}$                                     |      |      | 13   | $\Omega$               |
| llim_OUT1_low      | Output current limitation to ground, OUT1 in "low-ohmic" configuration    | $V(\text{OUT1}) = 0\text{ V}$                                   | -500 | -375 | -250 | mA                     |
| llim_OUT1_high     | Output current limitation to ground, OUT1 in "normal-ohmic" configuration | $V(\text{OUT1}) = 0\text{ V}$                                   | -330 | -235 | -140 | mA                     |
| llim_OUT2-4        | Output current limitation to ground                                       | $V(\text{OUT2-4}) = 0\text{ V}$                                 | -330 | -235 | -140 | mA                     |
| luld_OUT1_low      | OUT1 underload threshold, OUT1 in "low-ohmic" configuration               |   | -30  | -16  | -4   | mA                     |
| luld_OUT1_high     | OUT1 underload threshold, OUT1 in "normal-ohmic" configuration            |   | -6.5 | -3.5 | -0.8 | mA                     |
| luld_OUT2-4        | OUT2-4 underload threshold  |   | -6.5 | -3.5 | -0.8 | mA                     |
| lleak_OUT1-4_norm  | Output leakage current, normal mode                                       | $V_S = 28\text{ V}$<br>$V(\text{OUT1-4}) = 0\text{ V}$          | -3   |      |      | $\mu\text{A}$          |
| lleak_OUT1-4_stdby | Output leakage current, standby or sleep mode                             | $V_S = 28\text{ V}$<br>$V(\text{OUT1-4}) = 0\text{ V}$          | -3   |      |      | $\mu\text{A}$          |
| Slew_OUT1_low      | Slew rate of OUT1, OUT1 in "low-ohmic" configuration                      | $V_S = 13.2\text{ V}$<br>250 mA resistive load                  | 0.2  | 0.5  | 0.8  | $\text{V}/\mu\text{s}$ |
| Slew_OUT1_high     | Slew rate of OUT1, OUT1 in "normal-ohmic" configuration                   | $V_S = 13.2\text{ V}$<br>140 mA resistive load                  | 0.2  | 0.5  | 0.8  | $\text{V}/\mu\text{s}$ |
| Slew_OUT2-4        | Slew rate of OUT2-4   | $V_S = 13.2\text{ V}$<br>140 mA resistive load                  | 0.2  | 0.5  | 0.8  | $\text{V}/\mu\text{s}$ |
| Tblank_ULD_OUT1-4  | Underload detection blanking delay  | After OUT1-4 activation   | 65   | 80   | 95   | $\mu\text{s}$          |
| Tfilt_ULD_OUT1-4   | Underload detection filter time   |   | 50   | 60   | 75   | $\mu\text{s}$          |
| Tfilt_OLD_OUT1-4   | Overload shutdown filter time   |   | 50   | 60   | 75   | $\mu\text{s}$          |

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 11. HIGH-SIDE OUTPUT (OUT\_HS)**

| Symbol             | Parameter                                     | Test Condition  | Min   | Typ   | Max   | Unit                   |
|--------------------|---|---|-------|-------|-------|------------------------|
| Ron_OUT_HS         | On-resistance to VS                           | $T_J = 25^{\circ}\text{C}$ , $I(\text{OUT\_HS}) = -150\text{ mA}$ |       | 1     | 1.5   | $\Omega$               |
|                    |   | $T_J = 125^{\circ}\text{C}$                                       |       | 1.6   | 3     | $\Omega$               |
| Ilim_OUT_HS        | Output current limitation to ground           | $V(\text{OUT\_HS}) = 0\text{ V}$                                  | -1900 | -1500 | -1000 | mA                     |
| Iuld_OUT_HS        | Underload detection threshold                 |   | -120  | -80   | -40   | mA                     |
| Ileak_OUT_HS_norm  | Output leakage current, normal mode           | $V(\text{OUT\_HS}) = 0\text{ V}$                                  | -3    |       |       | $\mu\text{A}$          |
| Ileak_OUT_HS_stdby | Output leakage current, standby or sleep mode | $V(\text{OUT\_HS}) = 0\text{ V}$                                  | -3    |       |       | $\mu\text{A}$          |
| Slew_OUT_HS        | Slew rate of OUT_HS                           | $V_S = 13.2\text{ V}$<br>Resistive load 480 mA                    | 0.2   | 0.5   | 0.8   | $\text{V}/\mu\text{s}$ |
| Tblank_ULD_OUT_HS  | Underload detection blanking delay            | After OUT_HS activation   | 65    | 80    | 95    | $\mu\text{s}$          |
| Tfilt_ULD_OUT_HS   | Underload detection filter time               |   | 50    | 60    | 75    | $\mu\text{s}$          |
| Tfilt_OLD_OUT_HS   | Overload shutdown filter time                 |   | 102   | 120   | 138   | $\mu\text{s}$          |
| Tfit_OCR           | Over-current recovery filter time             |   | 340   | 400   | 460   | $\mu\text{s}$          |

**Table 12. LOW-SIDE RELAY OUTPUT (LS1/2)**

| Symbol            | Parameter                                     | Test Condition   | Min | Typ | Max | Unit                   |
|-------------------|---|--|-----|-----|-----|------------------------|
| Ron_LS1/2         | On-resistance to ground                       | $T_J = 25^{\circ}\text{C}$ , $I(\text{LS1/2}) = 100\text{ mA}$ |     |     | 3.3 | $\Omega$               |
| Ilim_LS1/2        | Output current limitation                     | $\text{LS1/2} = V_S$   | 250 | 340 | 500 | mA                     |
| Vclamp_LS1/2      | Output clamp voltage                          | $I(\text{LS1/2}) = 100\text{ mA}$                              | 50  |     | 65  | V                      |
| Ileak_LS1/2_norm  | Output leakage current, normal mode           | $\text{LS1/2} = V_S = 16\text{ V}$                             |     |     | 3   | $\mu\text{A}$          |
| Ileak_LS1/2_stdby | Output leakage current, standby or sleep mode | $\text{LS1/2} = V_S = 16\text{ V}$                             |     |     | 3   | $\mu\text{A}$          |
| Slew_LS1/2        | Slew rate of LS1/2                            | $V_S = 13.2\text{ V}$  | 0.2 | 2   | 4   | $\text{V}/\mu\text{s}$ |
| Tfilt_OLD_LS1/2   | Overload shutdown filter time                 |  | 50  | 60  | 75  | $\mu\text{s}$          |

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 13. INH HIGH-SIDE SWITCH**

| Symbol     | Parameter               | Test Condition  | Min  | Typ  | Max  | Unit          |
|------------|-------------------------|-----------------|------|------|------|---------------|
| V_INH_DROP | High-level voltage drop | I(INH) = -15 mA | 0.1  | 0.35 | 0.75 | V             |
| I_INH_LEAK | Leakage current         |                 | -1   |      | 1    | $\mu\text{A}$ |
| I_INH_LIM  | Current limitation      |                 | -230 |      | -45  | mA            |

**Table 14. WAKE-UP (WU1-3)**

| Symbol          | Parameter                               | Test Condition  | Min       | Typ       | Max       | Unit          |
|-----------------|---|---|-----------|-----------|-----------|---------------|
| Vth_down_WU1-3  | Wake-up negative edge threshold voltage | WU1-3 configurable as Source/Sink via SPI             | 0.4<br>VS | 0.5<br>VS | 0.6<br>VS | V             |
| Vth_up_WU1-3    | Wake-up positive edge threshold voltage | WU1-3 configurable as Source/Sink via SPI             | 0.4<br>VS | 0.5<br>VS | 0.6<br>VS | V             |
| Vhyst_WU1-3     | Wake-up threshold hysteresis            |   | 100       | 300       | 500       | mV            |
| Ipullup_WU1-3   | Pullup current                          | $1.5\text{ V} < V(\text{WU1-3}) < (V_S - 3\text{ V})$ | -30       | -20       | -10       | $\mu\text{A}$ |
| Ipulldown_WU1-3 | Pulldown current                        | $1.5\text{ V} < V(\text{WU1-3}) < (V_S - 3\text{ V})$ | 10        | 20        | 30        | $\mu\text{A}$ |
| Twu_WU1-3       | Minimum time for wake-up                |   | 51        | 64        | 77        | $\mu\text{s}$ |

**Table 15. CURRENT AMPLIFIER OP1/2**

| Symbol         | Parameter  | Test Condition               | Min      | Typ | Max | Unit             |
|----------------|--|------------------------------|----------|-----|-----|------------------|
| GBW_OP         | GBW product  |                              | 1        | 3.5 | 7   | MHz              |
| AV_DC_OP       | DC open loop gain                                    |                              | 80       |     |     | dB               |
| PSRR_OP        | Power supply rejection                               | DC, $V_{in} = 150\text{ mV}$ | 80       |     |     | dB               |
| Voff_OP        | Input offset voltage                                 |                              | -6       |     | 6   | mV               |
| Vicr_OP        | Common mode input range                              |                              | -0.2     | 0   | 3   | V                |
| Voh_OP         | Output voltage range high                            | I(OPOUT1/2) = -1 mA          | VS - 0.2 |     | VS  | V                |
| Vol_OP         | Output voltage range low                             | I(OPOUT1/2) = +1 mA          | 0        |     | 0.2 | V                |
| Ilimp_OPOUT1/2 | Output current limitation+                           | DC                           | 5        | 10  | 15  | mA               |
| Ilimn_OPOUT1/2 | Output current limitation-                           | DC                           | -15      | -10 | -5  | mA               |
| Slewp_OP       | Slew rate positive                                   |                              | 1        | 4   | 10  | V/ $\mu\text{s}$ |
| Slewn_OP       | Slew rate negative                                   |                              | -10      | -4  | -1  | V/ $\mu\text{s}$ |
| Tsat_rec       | Output recovery time from saturation at $V_S$ or GND |                              |          |     | 4   | $\mu\text{s}$    |

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## ELECTRICAL CHARACTERISTICS

(-40°C ≤ T<sub>J</sub> ≤ 150°C, 6 V ≤ V<sub>S</sub> ≤ 18 V, unless otherwise specified)

**Table 16. MODE TRANSITION TIMING**

| Symbol           | Parameter  | Test Condition                    | Min | Typ | Max | Unit |
|------------------|--|-----------------------------------|-----|-----|-----|------|
| Tdel_powerup     | Transition from power-up to Init                             | VS reaching VS_POR to VR1 startup |     |     | 2.5 | ms   |
| Tdel_norm_stdby  | Transition time from normal to standby mode via SPI          |                                   |     |     | 300 | μs   |
| Tdel_norm_sleep  | Transition time from normal to sleep mode via SPI            |                                   |     |     | 750 | μs   |
| Tdel_stdby_norm  | Delay of INTN pulse in standby after wakeup                  |                                   |     |     | 300 | μs   |
| Tdel_sleep_norm  | Transition from sleep to normal mode via wakeup              |                                   |     |     | 300 | μs   |
| Tdel_norm_flash  | Transition time from normal to flash mode via TxDL(C)/FLASH  |                                   |     |     | 300 | μs   |
| Tdel_stdby_flash | Transition time from standby to flash mode via TxDL(C)/FLASH |                                   |     |     | 300 | μs   |
| Tdel_sleep_flash | Transition time from sleep to flash mode via TxDL(C)/FLASH   |                                   |     |     | 750 | μs   |
| Tdel_flash_norm  | Transition from flash to normal mode via TxDL(C)/FLASH       |                                   |     |     | 450 | μs   |

**Table 17. NRES AND INTN SIGNAL TIMING**

| Symbol | Parameter  | Test Condition | Min | Typ | Max | Unit |
|--------|--|----------------|-----|-----|-----|------|
| T_NRES | NRES low pulse duration, e.g. after a watchdog failure |                | 1.7 | 2   | 2.3 | ms   |
| T_INTN | INTN low pulse duration after a wake-up event          |                | 106 | 125 | 144 | μs   |

**Table 18. INTERNAL PWM AND TIMERS**

| Symbol   | Parameter  | Test Condition                                     | Min | Typ | Max | Unit |
|----------|--|--|-----|-----|-----|------|
| f_PWM_lo | PWM controller frequency, Low setting (default)                    | FSEL_OUTx/LSx = 0                                  | 127 | 150 | 173 | Hz   |
| f_PWM_hi | PWM controller frequency, High setting                             | FSEL_OUTx/LSx = 1                                  | 170 | 200 | 230 | Hz   |
| Ttim_acc | Timer1/2 period/on-time accuracy (see CONTROL_2 register settings) | T1_TPER.[2:0], T1_TON, T2_TPER.[2:0], T2_TON.[1:0] | -15 |     | +15 | %    |

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , unless otherwise specified)

**Table 19. DRIVERS/VR2 TIMING**

| Symbol          | Parameter   | Test Condition   | Min | Typ | Max | Unit          |
|-----------------|---|--|-----|-----|-----|---------------|
| Tdel_OUT_HS_on  | Activation delay of OUT_HS driver (from CSN rising edge)    | $V(\text{OUT\_HS}) > 0.2 \cdot V_S$                            |     |     | 60  | $\mu\text{s}$ |
| Tdel_OUT_HS_off | De-activation delay of OUT_HS driver (from CSN rising edge) | $V(\text{OUT\_HS}) < 0.8 \cdot V_S$                            |     |     | 60  | $\mu\text{s}$ |
| Tdel_OUT1-4_on  | Activation delay of OUT1-4 driver (from CSN rising edge)    | $V(\text{OUT1-4}) > 0.2 \cdot V_S$                             |     |     | 60  | $\mu\text{s}$ |
| Tdel_OUT1-4_off | De-activation delay of OUT1-4 driver (from CSN rising edge) | $V(\text{OUT1-4}) < 0.8 \cdot V_S$                             |     |     | 60  | $\mu\text{s}$ |
| Tdel_LS1/2_on   | Activation delay of LS1/2 driver (from CSN rising edge)     | $V(\text{LS1/2}) < 0.8 \cdot V_S$                              |     |     | 100 | $\mu\text{s}$ |
| Tdel_LS1/2_off  | De-activation delay of LS1/2 driver (from CSN rising edge)  | $V(\text{LS1/2}) > 0.2 \cdot V_S$                              |     |     | 100 | $\mu\text{s}$ |
| Tdel_VR2_on     | Activation delay of VR2 (from CSN rising edge)              | $I(\text{VR2}) = 50\text{ mA}$<br>$V(\text{VR2}) > 4\text{ V}$ |     | 270 |     | $\mu\text{s}$ |
| Tdel_VR2_off    | De-activation delay of VR2 (from CSN rising edge)           | $I(\text{VR2}) = 50\text{ mA}$<br>$V(\text{VR2}) < 4\text{ V}$ |     | 200 |     | $\mu\text{s}$ |

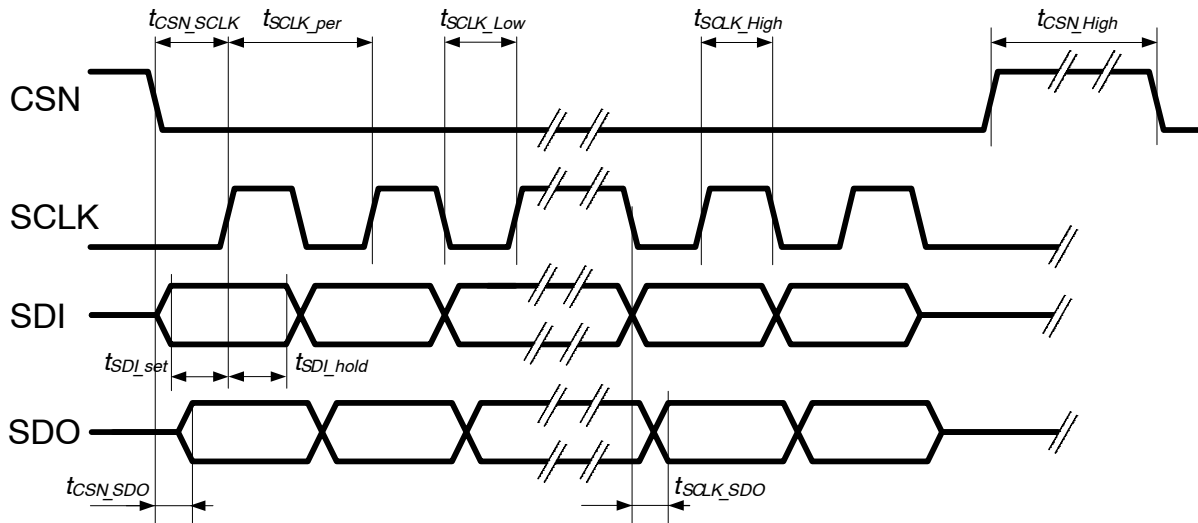
**ELECTRICAL CHARACTERISTICS**

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_s \leq 18\text{ V}$ , unless otherwise specified)

**Table 20. SPI TIMING**

| Symbol     | Parameter                                      | Test Condition | Min | Typ | Max | Unit          |
|------------|--|----------------|-----|-----|-----|---------------|
| tCSN_SCLK  | First SPI clock edge after CSN active          | (Note 3)       | 100 |     |     | ns            |
| tCSN_SDO   | SDO output stable after CSN active             | (Note 3)       |     |     | 80  | ns            |
| tCSN_High  | Inter-frame space (CSN inactive)               | (Note 3)       | 14  |     |     | $\mu\text{s}$ |
| tSCLK_High | Duration of SPI clock High level               | (Note 3)       | 250 |     |     | ns            |
| tSCLK_Low  | Duration of SPI clock Low level                | (Note 3)       | 250 |     |     | ns            |
| tSCLK_per  | SPI clock period                               | (Note 3)       | 1   |     |     | $\mu\text{s}$ |
| tSDI_set   | Setup time of SDI input towards SPI clock      | (Note 3)       | 100 |     |     | ns            |
| tSDI_hold  | Hold time of SDI input towards SPI clock       | (Note 3)       | 100 |     |     | ns            |
| tSCLK_SDO  | SDO output stable after SPI clock falling edge | (Note 3)       |     |     | 250 | ns            |

3. Values based on design and characterization, not tested in production.



**Figure 5. SPI Timing Parameters**



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## ELECTRICAL CHARACTERISTICS

(-40°C ≤ T<sub>J</sub> ≤ 150°C, 6 V ≤ V<sub>S</sub> ≤ 18 V, unless otherwise specified)

**Table 21. WINDOW WATCHDOG**

| Symbol     | Parameter  | Test Condition    | Min   | Typ  | Max   | Unit |
|------------|--|-------------------|-------|------|-------|------|
| Twd_acc    | Watchdog timing accuracy   |                   | -25   |      | 25    | %    |
| T_wd_TO    | Timeout watchdog period;<br>(watchdog is in the timeout mode after NRES release) |                   | 48.75 | 65   | 81.25 | ms   |
| T_wd_CW    | Window watchdog closed window  | SPI WD_PER.x = 00 |       | 6    |       | ms   |
|            |  | SPI WD_PER.x = 01 |       | 24   |       |      |
|            |  | SPI WD_PER.x = 10 |       | 60   |       |      |
|            |  | SPI WD_PER.x = 11 |       | 120  |       |      |
| T_wd_OW    | Window watchdog open window  | SPI WD_PER.x = 00 |       | 10   |       | ms   |
|            |  | SPI WD_PER.x = 01 |       | 40   |       |      |
|            |  | SPI WD_PER.x = 10 |       | 100  |       |      |
|            |  | SPI WD_PER.x = 11 |       | 200  |       |      |
| T_wd_trig  | Window watchdog trigger period via SPI<br>(the safe trigger area)                | SPI WD_PER.x = 00 | 7.5   | 9.75 | 12    | ms   |
|            |  | SPI WD_PER.x = 01 | 30    | 39   | 48    |      |
|            |  | SPI WD_PER.x = 10 | 75    | 97.5 | 120   |      |
|            |  | SPI WD_PER.x = 11 | 150   | 195  | 240   |      |
| T_wd_33_TO | WD_STATUS.0 bit threshold of timeout length<br>(in timeout mode)                 |                   |       | 31.5 |       | %    |
| T_wd_66_TO | WD_STATUS.1 bit threshold of timeout length<br>(in timeout mode)                 |                   |       | 63   |       | %    |
| T_wd_33_OW | WD_STATUS.0 bit threshold of open window length<br>(in open window mode)         | SPI WD_PER.x = 00 |       | 26.5 |       | %    |
|            |  | SPI WD_PER.x = 01 |       | 32   |       |      |
|            |  | SPI WD_PER.x = 10 |       | 33.3 |       |      |
|            |  | SPI WD_PER.x = 11 |       | 33.3 |       |      |
| T_wd_66_OW | WD_STATUS.1 bit threshold of open window length<br>(in open window mode)         | SPI WD_PER.x = 00 |       | 63   |       | %    |
|            |  | SPI WD_PER.x = 01 |       | 76.8 |       |      |
|            |  | SPI WD_PER.x = 10 |       | 66.6 |       |      |
|            |  | SPI WD_PER.x = 11 |       | 66.6 |       |      |

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( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $5\text{ V} \leq V_S \leq 28\text{ V}$ , Normal mode, unless otherwise specified); the following bus loads are considered: L1 = 1 k $\Omega$  / 1 nF; L2 = 660  $\Omega$  / 6.8 nF; L3 = 500  $\Omega$  / 10 nF.

**Table 22. LIN TRANSMITTER DC CHARACTERISTICS**

| Symbol         | Parameter                            | Test condition               | Min      | Typ | Max | Unit       |
|----------------|--------------------------------------|------------------------------|----------|-----|-----|------------|
| VLin_dom_LoSup | LIN dominant output voltage          | TxDL = low; VS = 7.3 V, L1   |          |     | 1.2 | V          |
| VLin_dom_HiSup | LIN dominant output voltage          | TxDL = low; VS = 18 V, L1    |          |     | 2   | V          |
| VLin_rec       | LIN recessive output voltage         | TxDL = high<br>I(LIN) = 0 mA | VS - 1.2 |     |     | V          |
| ILIN_lim       | LIN short circuit current limitation | V(LIN) = 18 V                | 40       |     | 200 | mA         |
| Rslave_LIN     | Internal pull-up resistance          |                              | 20       | 33  | 47  | k $\Omega$ |

**Table 23. LIN RECEIVER DC CHARACTERISTICS**

| Symbol           | Parameter                                  | Test condition                                      | Min      | Typ | Max      | Unit          |
|------------------|--|---|----------|-----|----------|---------------|
| Vbus_dom_LIN     | Bus voltage for dominant state             |   |          |     | 0.4      | VS            |
| Vbus_rec_LIN     | Bus voltage for recessive state            |   | 0.6      |     |          | VS            |
| Vrec_dom_LIN     | Receiver threshold                         | LIN bus recessive $\rightarrow$ dominant            | 0.4      |     | 0.5      | VS            |
| Vrec_rec_LIN     | Receiver threshold                         | LIN bus dominant $\rightarrow$ recessive            | 0.5      |     | 0.6      | VS            |
| Vrec_cnt_LIN     | Receiver threshold centre voltage          | $(V_{rec\_rec\_LIN} + V_{rec\_dom\_LIN}) / 2$       | 0.475    |     | 0.525    | VS            |
| Vrec_hys_LIN     | Receiver hysteresis                        | $(V_{rec\_rec\_LIN} - V_{rec\_dom\_LIN})$           | 0.05     |     | 0.175    | VS            |
| Vrec_rec_slp_LIN | LIN wake receiver threshold                | Sleep or standby mode                               | VS - 3.3 |     | VS - 1.1 | V             |
| ILIN_off_dom     | LIN output current, bus in dominant state  | Normal mode, driver off;<br>VS = 12 V; V(LIN) = 0 V | -1       |     |          | mA            |
| ILIN_off_dom_slp | LIN output current, bus in dominant state  | Sleep mode, driver off;<br>VS = 12 V; V(LIN) = 0 V  | -20      | -15 | -2       | $\mu\text{A}$ |
| ILIN_off_rec     | LIN output current, bus in recessive state | Driver off;<br>VS < 18 V; VS < V(LIN) < 18 V        |          |     | 20       | $\mu\text{A}$ |
| ILIN_no_GND      | LIN current with missing GND               | VS = GND = 12 V;<br>0 < V(LIN) < 18 V               | -1       |     | 1        | mA            |
| ILIN_no_VS       | LIN current with missing VS                | VS = GND = 0 V;<br>0 < V(LIN) < 18 V                |          |     | 100      | $\mu\text{A}$ |

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( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $5\text{ V} \leq V_S \leq 28\text{ V}$ , Normal Mode, unless otherwise specified); the following bus loads are considered: L1 = 1 k  $\Omega$  / 1 nF; L2 = 660  $\Omega$  / 6.8 nF; L3 = 500  $\Omega$  / 10 nF.

**Table 24. LIN TRANSMITTER DYNAMIC CHARACTERISTICS**

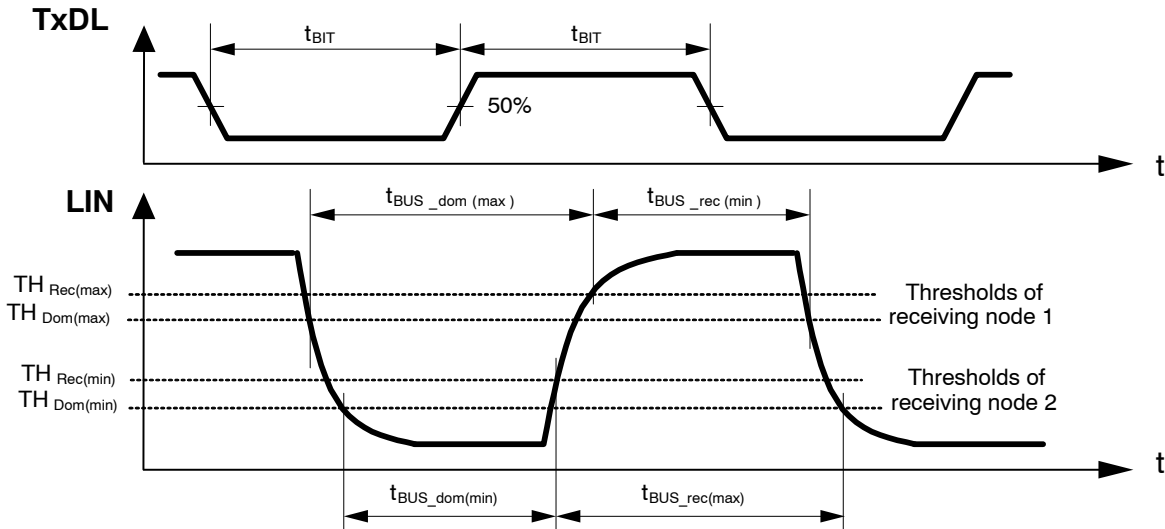
| Symbol          | Parameter   | Test condition  | Min      | Typ | Max   | Unit          |
|-----------------|---|---|----------|-----|-------|---------------|
| D1              | Duty Cycle 1 = $t_{\text{BUS\_REC}}(\text{min}) / (2 \times \text{TBit})$ | THREC(max) = 0.744 x VS<br>THDOM(max) = 0.581 x VS<br>TBIT = 50 $\mu\text{s}$<br>VS = 7 V to 18 V   | 0.396    |     | 0.5   | –             |
| D2              | Duty Cycle 2 = $t_{\text{BUS\_REC}}(\text{max}) / (2 \times \text{TBit})$ | THREC(min) = 0.422 x VS<br>THDOM(min) = 0.284 x VS<br>TBIT = 50 $\mu\text{s}$<br>VS = 7.6 V to 18 V | 0.5      |     | 0.581 | –             |
| D3              | Duty Cycle 3 = $t_{\text{BUS\_REC}}(\text{min}) / (2 \times \text{TBit})$ | THREC(max) = 0.788 x VS<br>THDOM(max) = 0.616 x VS<br>TBIT = 96 $\mu\text{s}$<br>VS = 7 V to 18 V   | 0.417    |     | 0.5   | –             |
| D4              | Duty Cycle 4 = $t_{\text{BUS\_REC}}(\text{max}) / (2 \times \text{TBit})$ | THREC(min) = 0.389 x VS<br>THDOM(min) = 0.251 x VS<br>TBIT = 96 $\mu\text{s}$<br>VS = 7.6 V to 18 V | 0.5      |     | 0.59  | –             |
| T_fall_LIN      | LIN falling edge  | VS = 12 V; L1, L2;<br>Normal slope mode   |          |     | 22.5  | $\mu\text{s}$ |
| T_rise_LIN      | LIN rising edge   | VS = 12 V; L1, L2;<br>Normal slope mode   |          |     | 22.5  | $\mu\text{s}$ |
| T_sym_LIN       | LIN slope symmetry  | VS = 12 V; L1, L2;<br>Normal slope mode   | –4       | 0   | 4     | $\mu\text{s}$ |
| T_fall_norm_LIN | LIN falling edge  | VS = 12 V; L3;<br>Normal slope mode   |          |     | 27    | $\mu\text{s}$ |
| T_rise_norm_LIN | LIN rising edge   | VS = 12 V; L3;<br>Normal slope mode   |          |     | 27    | $\mu\text{s}$ |
| T_sym_norm_LIN  | LIN slope symmetry  | VS = 12 V; L3;<br>Normal slope mode   | –5       | 0   | 5     | $\mu\text{s}$ |
| T_fall_low_LIN  | LIN falling edge  | VS = 12 V; L3;<br>Low slope mode  |          |     | 62    | $\mu\text{s}$ |
| T_rise_low_LIN  | LIN rising edge   | VS = 12 V; L3;<br>Low slope mode  |          |     | 62    | $\mu\text{s}$ |
| T_TxDL_timeout  | TxDL dominant time-out<br>Selected by SPI bits<br>TxDL_TO                 | SPI setting "00"  | 27       | 55  | 70    | ms            |
|                 |   | SPI setting "01"  | 6        | 13  | 20    |               |
|                 |   | SPI setting "1X"  | disabled |     |       |               |
| C_LIN           | Capacitance of the LIN pin  | Guaranteed by design;<br>not tested in production   |          | 15  | 25    | pF            |

**ELECTRICAL CHARACTERISTICS**

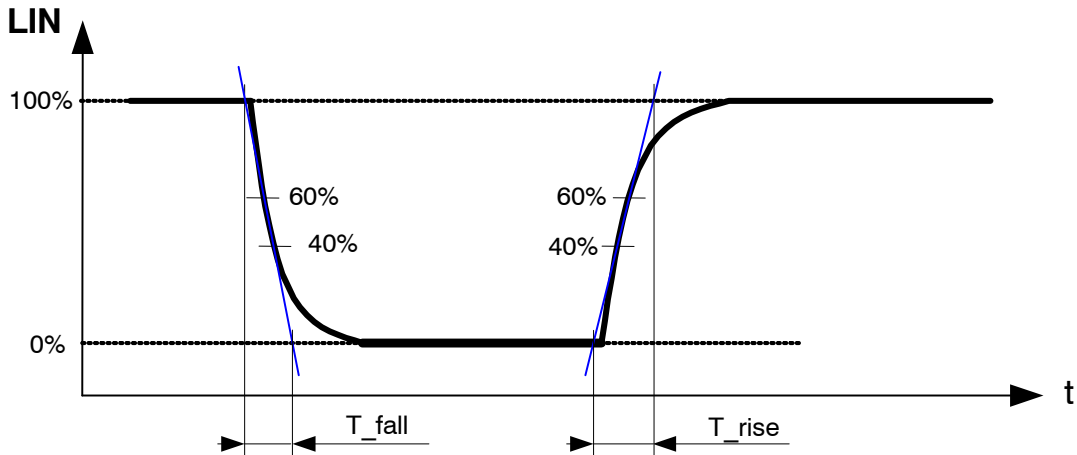
( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $5\text{ V} \leq V_s \leq 28\text{ V}$ , Normal mode, unless otherwise specified); the following bus loads are considered: L1 = 1 k  $\Omega$  / 1 nF; L2 = 660  $\Omega$  / 6.8 nF; L3 = 500  $\Omega$  / 10 nF.

**Table 25. LIN RECEIVER DYNAMIC CHARACTERISTICS**

| Symbol         | Parameter                                  | Test condition                | Min | Typ | Max | Unit          |
|----------------|--|-------------------------------|-----|-----|-----|---------------|
| Trec_prop_down | Propagation delay of receiver falling edge |                               |     |     | 6   | $\mu\text{s}$ |
| Trec_prop_up   | Propagation delay of receiver rising edge  |                               |     |     | 6   | $\mu\text{s}$ |
| Trec_sym       | Propagation delay symmetry                 | Trec_prop_down – Trec_prop_up | -2  |     | 2   | $\mu\text{s}$ |
| T_LIN_wake     | Dominant duration for wakeup               |                               | 30  | 90  | 150 | $\mu\text{s}$ |



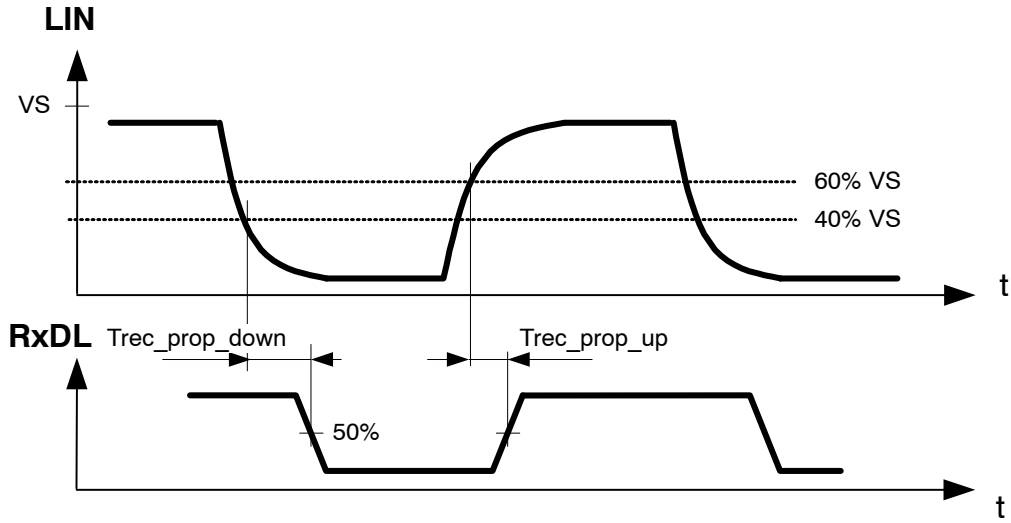
**Figure 6. LIN Dynamic Characteristics – Duty Cycles**



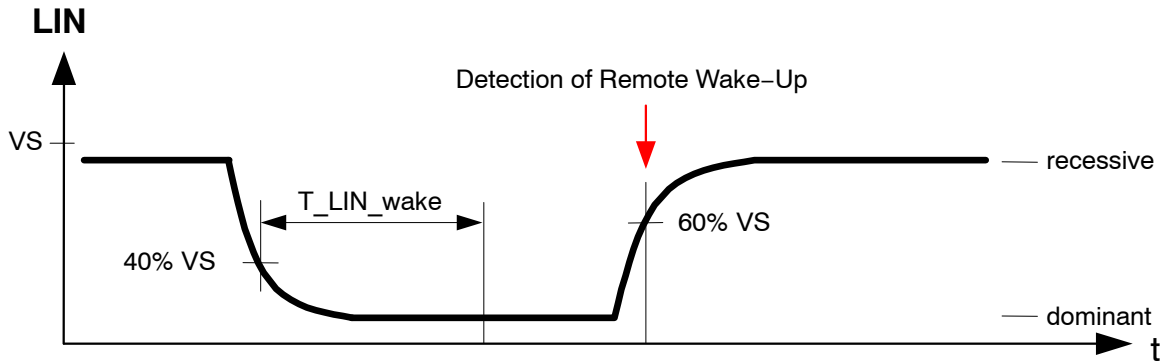
**Figure 7. LIN Dynamic Characteristics – Transmitter Slope**

**ELECTRICAL CHARACTERISTICS**

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $5\text{ V} \leq V_S \leq 28\text{ V}$ , Normal mode, unless otherwise specified); the following bus loads are considered: L1 = 1 k  $\Omega$  / 1 nF; L2 = 660  $\Omega$  / 6.8 nF; L3 = 500  $\Omega$  / 10 nF.



**Figure 8. LIN Dynamic Characteristics – Receiver**



**Figure 9. LIN Wakeup**

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , Normal mode, unless otherwise specified)

**Table 26. CAN TRANSMITTER DC CHARACTERISTICS**

| Symbol                               | Parameter   | Test condition  | Min  | Typ  | Max  | Unit |
|--------------------------------------|---|---|------|------|------|------|
| $V_{o(\text{reces})}(\text{CANH})$   | Recessive bus voltage at pin CANH                                       | $V(\text{TxDC}) = V_{R1}$<br>no load,<br>transmitter on                                     | 2    | 2.5  | 3    | V    |
| $V_{o(\text{reces})}(\text{CANH})$   | Recessive bus voltage at pin CANH                                       | no load,<br>transmitter off   | -0.1 | 0    | 0.1  | V    |
| $V_{o(\text{reces})}(\text{CANL})$   | Recessive bus voltage at pin CANL                                       | $V(\text{TxDC}) = V_{R1}$<br>no load,<br>transmitter on                                     | 2    | 2.5  | 3    | V    |
| $V_{o(\text{reces})}(\text{CANL})$   | Recessive bus voltage at pin CANL                                       | no load,<br>transmitter off   | -0.1 | 0    | 0.1  | V    |
| $I_{o(\text{reces})}(\text{CANH})$   | Recessive output current at pin CANH                                    | $-35\text{ V} < V(\text{CANH}) < 35\text{ V}$<br>$0\text{ V} < V_{CC\_CAN} < 5.25\text{ V}$ | -2.5 |      | 2.5  | mA   |
| $I_{o(\text{reces})}(\text{CANL})$   | Recessive output current at pin CANL                                    | $-35\text{ V} < V(\text{CANL}) < 35\text{ V}$<br>$0\text{ V} < V_{CC\_CAN} < 5.25\text{ V}$ | -2.5 |      | 2.5  | mA   |
| $V_{o(\text{dom})}(\text{CANH})$     | Dominant output voltage at pin CANH                                     | $V(\text{TxDC}) = 0\text{ V}$<br>$42.5\ \Omega < R_L < 60\ \Omega$                          | 3    | 3.6  | 4.25 | V    |
| $V_{o(\text{dom})}(\text{CANL})$     | Dominant output voltage at pin CANL                                     | $V(\text{TxDC}) = 0\text{ V}$<br>$42.5\ \Omega < R_L < 60\ \Omega$                          | 0.5  | 1.4  | 1.75 | V    |
| $V_{o(\text{dif})}(\text{bus\_dom})$ | Differential bus output voltage ( $V_{\text{CANH}} - V_{\text{CANL}}$ ) | $V(\text{TxDC}) = 0\text{ V}$<br>$42.5\ \Omega < R_L < 60\ \Omega$                          | 1.5  | 2.25 | 3    | V    |
| $V_{o(\text{dif})}(\text{bus\_rec})$ | Differential bus output voltage ( $V_{\text{CANH}} - V_{\text{CANL}}$ ) | $V(\text{TxDC}) = V_{R1}$<br>recessive, no load   | -120 | 0    | 50   | mV   |
| $I_{o(\text{SC})}(\text{CANH})$      | Short-circuit output current at pin CANH                                | $V(\text{CANH}) = 0\text{ V}$ ,<br>$V(\text{TxDC}) = 0\text{ V}$                            | -120 | -80  | -45  | mA   |
| $I_{o(\text{SC})}(\text{CANL})$      | Short-circuit output current at pin CANL                                | $V(\text{CANL}) = 36\text{ V}$ ,<br>$V(\text{TxDC}) = 0\text{ V}$                           | 45   | 80   | 120  | mA   |

**ELECTRICAL CHARACTERISTICS**

(-40°C ≤ T<sub>J</sub> ≤ 150°C, 6 V ≤ V<sub>S</sub> ≤ 18 V, Normal mode, unless otherwise specified)

**Table 27. CAN RECEIVER DC CHARACTERISTICS**

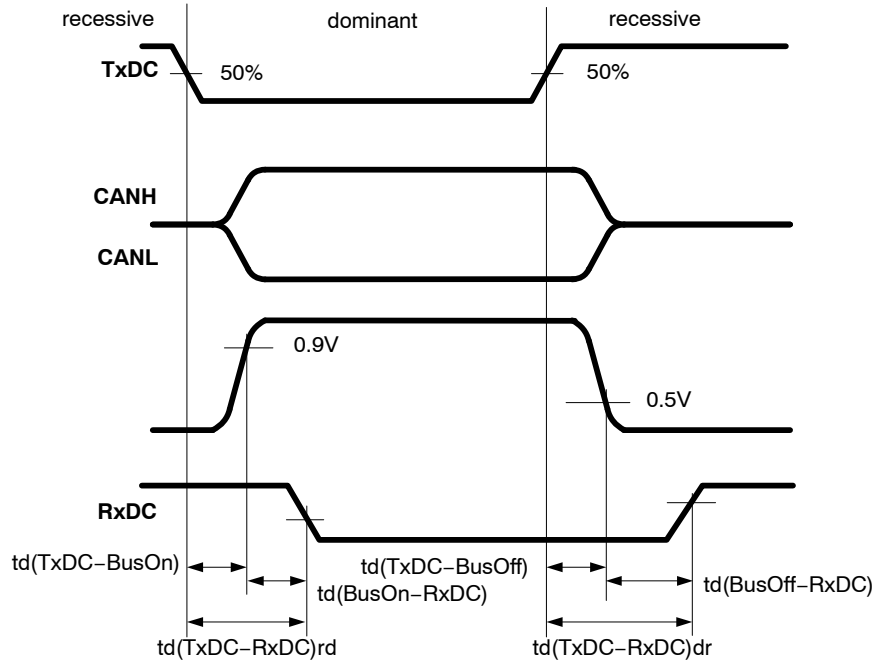
| Symbol                      | Parameter   | Test condition                                   | Min | Typ  | Max  | Unit |
|-----------------------------|---|--|-----|------|------|------|
| V <sub>i(dif)</sub> (th)    | Differential receiver threshold voltage                             | -5 V < V(CANH) < 12 V<br>-5 V < V(CANL) < 12 V   | 0.5 | 0.7  | 0.9  | V    |
| V <sub>ihcm(dif)</sub> (th) | Differential receiver threshold voltage for high common mode        | -35 V < V(CANH) < 35 V<br>-35 V < V(CANL) < 35 V | 0.4 | 0.7  | 1    | V    |
| R <sub>i(cm)</sub> CANH     | Common mode input resistance at pin CANH                            |  | 15  | 26   | 37   | kΩ   |
| R <sub>i(cm)</sub> CANL     | Common mode input resistance at pin CANL                            |  | 15  | 26   | 37   | kΩ   |
| R <sub>i(cm)</sub> (m)      | Matching between pin CANH and pin CANL common mode input resistance | V(CANH) = V(CANL)                                | -3  | 0    | 3    | %    |
| R <sub>i(dif)</sub>         | Differential input resistance                                       |  | 25  | 50   | 75   | kΩ   |
| C <sub>l</sub> (CANH)       | Input capacitance at pin CANH                                       | V(TxDC) = VCC_CAN<br>not tested in production    |     | 7.5  | 20   | pF   |
| C <sub>l</sub> (CANL)       | Input capacitance at pin CANL                                       | V(TxDC) = VCC_CAN<br>not tested in production    |     | 7.5  | 20   | pF   |
| C <sub>l</sub> (dif)        | Differential input capacitance                                      | V(TxDC) = VCC_CAN<br>not tested in production    |     | 3.75 | 10   | pF   |
| ILI                         | Input leakage current at pin CANH and CANL                          | VCC_CAN = 0 V<br>V(CANH) = 5 V<br>V(CANL) = 5 V  | -5  | 0    | 5    | μA   |
| V <sub>i(dif)</sub> (th)    | Differential receiver threshold voltage for the wakeup detection    | -12 V < V(CANH) < 12 V<br>-12 V < V(CANL) < 12 V | 0.4 | 0.8  | 1.15 | V    |

**ELECTRICAL CHARACTERISTICS**

(-40°C ≤ T<sub>J</sub> ≤ 150°C, 6 V ≤ V<sub>S</sub> ≤ 18 V, Normal mode, unless otherwise specified)

**Table 28. CAN DYNAMIC CHARACTERISTICS**

| Symbol            | Parameter                         | Test condition                  | Min | Typ | Max  | Unit |
|-------------------|-----------------------------------|---------------------------------|-----|-----|------|------|
| td(TxDC-BusOn)    | Delay TxDC to bus active          | CL = 100 pF between CANH - CANL | 10  |     | 110  | ns   |
| td(TxDC-BusOff)   | Delay TxDC to bus inactive        | CL = 100 pF between CANH - CANL | 10  |     | 110  | ns   |
| td(BusOn-RxDC)    | Delay bus active to RxDC          | C(RxDC) = 15 pF                 | 10  |     | 105  | ns   |
| td(BusOff-RxDC)   | Delay bus inactive to RxDC        | C(RxDC) = 15 pF                 | 10  |     | 105  | ns   |
| tdPD(TxDC-RxDC)dr | Propagation delay TxDC to RxDC    | CL = 100 pF between CANH - CANL | 45  |     | 245  | ns   |
| tdPD(TxDC-RxDC)rd | Propagation delay TxDC to RxDC    | CL = 100 pF between CANH - CANL | 45  |     | 230  | ns   |
| tdBUS-hovr        | Dominant time for wake-up via bus | LP mode Vdif(dom) > 1.4 V       | 0.5 | 2.5 | 5    | μs   |
| tdBUS-lovr        | Dominant time for wake-up via bus | LP mode Vdif(dom) > 1.2 V       | 0.5 | 3   | 5.8  | μs   |
| T_TxDC_timeout    | TxDC dominant time for time out   | V(TxDC) = 0 V                   | 300 | 650 | 1000 | μs   |



**Figure 10. CAN Dynamic Characteristics**



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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , Normal mode, unless otherwise specified)

**Table 29. VSPLIT CHARACTERISTICS**

| Symbol        | Parameter   | Test condition   | Min | Typ | Max | Unit          |
|---------------|---|--|-----|-----|-----|---------------|
| VSPLIT        | Reference output voltage at pin VSPLIT                              | Transmitter on<br>$-500\ \mu\text{A} < I_{\text{split}} < 500\ \mu\text{A}$                                | 0.3 | 0.5 | 0.7 | $V_{CC\_CAN}$ |
| ISPLIT(li100) | VSPLIT leakage current  | Transmitter off<br>$-40\text{ V} < \text{VSPLIT} < 40\text{ V}$<br>$T_{\text{junc}} < 100^{\circ}\text{C}$ | -1  | 0   | 1   | $\mu\text{A}$ |
| ISPLIT(li)    | VSPLIT leakage current  | Transmitter off<br>$-40\text{ V} < \text{VSPLIT} < 40\text{ V}$  | -5  | 0   | 5   | $\mu\text{A}$ |
| ISPLIT(lim)   | Absolute value of limitation current at $\pm 35\text{ V}$ on VSPLIT | Transmitter on   | 1.3 | 3   | 5   | mA            |

**Table 30. RxDL/INTN, RxDC, SDO Outputs**

| Symbol        | Parameter                         | Test condition  | Min | Typ | Max | Unit          |
|---------------|-----------------------------------|---|-----|-----|-----|---------------|
| loutL_pinx    | Low-level output driving current  | pinx is logical Low<br>forced $V(\text{pinx}) = 0.4\text{ V}$           | 2   | 5   | 12  | mA            |
| loutH_pinx    | High-level output driving current | pinx is logical High<br>forced $V(\text{pinx}) = V_{R1} - 0.4\text{ V}$ | -12 | -5  | -2  | mA            |
| lleak_HZ_pinx | Leakage in the tristate, pin SDO  | pinx in the HZ state<br>forced $0\text{ V} < V(\text{pinx}) < V_{R1}$   | -5  |     | 5   | $\mu\text{A}$ |

**Table 31. NRES Output**

| Symbol       | Parameter                             | Test condition   | Min | Typ | Max | Unit             |
|--------------|---------------------------------------|--|-----|-----|-----|------------------|
| VoutL_NRES   | Low-level output voltage              | $V_{R1} < 1\text{ V}$ , $I(\text{NRES}) = 1\text{ mA}$ |     | 0.2 | 0.4 | V                |
| Rpullup_NRES | Internal pull-up resistor to $V_{R1}$ |  | 55  | 100 | 185 | $\text{k}\Omega$ |

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## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ,  $6\text{ V} \leq V_S \leq 18\text{ V}$ , Normal mode, unless otherwise specified)

**Table 32. TxDx/FLASH, SDI, SCLK, CSN Inputs**

| Symbol         | Parameter  | Test condition   | Min       | Typ       | Max       | Unit       |
|----------------|--|------------------|-----------|-----------|-----------|------------|
| VinL_pinx      | Low-level input voltage  |                  | 0         |           | 0.8       | V          |
| VinH_pinx      | High-level input voltage   |                  | 2         |           | VR1       | V          |
| Vin_hys_pinx   | Input voltage hysteresis   |                  | 60        |           | 500       | mV         |
| Rpullup_pinx   | Internal pull-up resistor to VR1; pins TxDx/FLASH, CSN             |                  | 55        | 100       | 185       | k $\Omega$ |
| Rpulldown_pinx | Internal pull-down resistor to ground; pins SDI, SCLK              |                  | 55        | 100       | 185       | k $\Omega$ |
| VinL_FLASH     | Input low level for flash mode exit, pins TxDx/FLASH, TxDx/FLASH   | VR1 $\geq$ 2.5 V | VR1 + 1.5 | VR1 + 2.5 | VR1 + 3.5 | V          |
| VinH_FLASH     | Input high level for flash mode entry, pins TxDx/FLASH, TxDx/FLASH |                  | VR1 + 2.5 | VR1 + 3.3 | VR1 + 4.3 | V          |
| Vin_hys_FLASH  | Input hysteresis, pins TxDx/FLASH, TxDx/FLASH                      |                  | 0.4       | 0.8       | 1.1       | V          |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## FUNCTIONAL DESCRIPTION

The NCV7462 is a monolithic LIN/CAN System-Basis-Chip with enhanced feature set useful in automotive body control systems. Besides the bus interfaces the IC features two 5 V voltage regulators, several high-side and low-side switches to control LEDs and relays plus supervision functionality like a window watchdog. This allows a highly integrated solution by replacing external discrete components while maintaining the valuable flexibility. Due to this the board space and ECU weight can be minimized to the lowest level.

### Power Supply and Regulators

#### VS – Main Power Supply

VS pin is the main power supply of the device. In the application, it will be typically connected to the KL30 or KL15 car node. It is necessary to provide an external reverse-polarity protection and filtering capacitor on the VS supply – see Figure 3.

VS supply is monitored with respect to the following events:

- VS power-on reset is detected as a crossing of VS\_POR level (typ. 3.45 V). When VS remains below VS\_POR, the device is passive and provides no functionality, the SPI registers are reset to their default values. When VS rises above VS\_POR, the device starts following its state diagram through the power-up state. This event is latched in the SPI bit “COLD\_START” so that the application software can detect the VS connection.
- VS Under-Voltage is detected when VS falls below VS\_UV threshold (typ. 5.5 V). A VS under-voltage can be encountered, for example, with a discharged car battery or during engine cranking. The high-side and low-side drivers are typically forced off in order to protect the loads and LIN transmission is disabled. The exact driver reaction depends on the SPI control settings – see par. “VS Over- and Under-Voltage”. Under-voltage events are flagged through SPI bit “VS\_UV”.
- VS Over-Voltage is detected when VS rises over VS\_OV threshold (typ. 21 V). Similarly to the under-voltage, the high-side and low-side drivers are de-activated based on the SPI settings and the event is flagged through SPI bit “VS\_OV”.

#### GND1, GND2 – Ground Connections

The device ground connection is split to two pins – GND1 and GND2. Both pins have to be connected on the application PCB.

#### Regulator VR1

VR1 is a low-drop output regulator providing 5 V voltage derived from the VS main supply. It is able to deliver up to 250 mA and is primarily intended to supply the application microcontroller unit (MCU) and related 5 V loads (e.g. its

own MCU-related digital inputs/outputs). An external capacitor needs to be connected on VR1 pin in order to ensure the regulator’s stability and to filter the disturbances caused by the connected loads.

The VR1 pin can also be used in the application to supply the on-chip CAN transceiver through the dedicated input pin VCC\_CAN. The supply line must be carefully filtered by external components in this case so that the mutual disturbances between the CAN communication line and the other VR1 loads (mainly MCU) are limited.

VR1 voltage is supplying all digital low-voltage input/output pins.

The protection and monitoring of the VR1 regulator consist of the following features:

- VR1 Current Limitation – the current protection ensures fast enough charging of the external capacitor at start-up while protecting the regulator in case of shorts to ground
- Junction Temperature Monitor – the junction temperature is monitored and when it rises above the second shutdown level, the VR1 regulator is de-activated for a defined period of time (typ. 1 sec). In case of re-occurring thermal shutdowns, the device is forced to the sleep mode in order to protect the regulators and the full application. For details, see par. “Thermal Protection”.
- VR1 Failure Comparator – during the VR1 start-up and operation, the VR1 voltage is continuously compared with Vfail\_VR1 level (typ. 2 V). During startup, if VR1 does not rise above Vfail\_VR1 level within Tshort\_VR1 (typ. 4 ms), it’s considered shorted to ground and the device is forced to sleep mode. During the VR1 operation, any dip below Vfail\_VR1 level longer than Tfail\_VR1 (typ. 5  $\mu$ s) is considered a failure – temporary excursions of VR1 under the failure threshold can be caused, for example, by EMC, and can lead to memory data inconsistencies inside the MCU. Both the failure during VR1 startup and the operation are latched in the “VR1\_FAIL” SPI bit for subsequent software diagnostics.
- VR1 Reset Comparator – the VR1 regulator output is compared with a reset level VR1\_RES (programmable to typ. 74%, 79%, 87% and 91% of the nominal VR1 voltage). If the VR1 level drops below this level for longer than Tflt\_VR1\_RES (typ. 16  $\mu$ s), a reset towards the MCU is generated through the NRES pin and all outputs (OUT1–4, LS1/2, VR2) are switched off until NRES pin becomes high and watchdog is served correctly.
- VR1 Consumption Monitor (Icmp) – to ensure a safe transition into the standby mode, where VR1 remains active while the watchdog is off, the VR1 current consumption is monitored. The watchdog is really

disabled in the standby mode only when the VR1 consumption falls below  $I_{c\text{mp\_VR1\_fall}}$  (typ. 1.1 mA).

An increase of the VR1 consumption above the  $I_{c\text{mp\_VR1\_rise}}$  level activates the watchdog again.

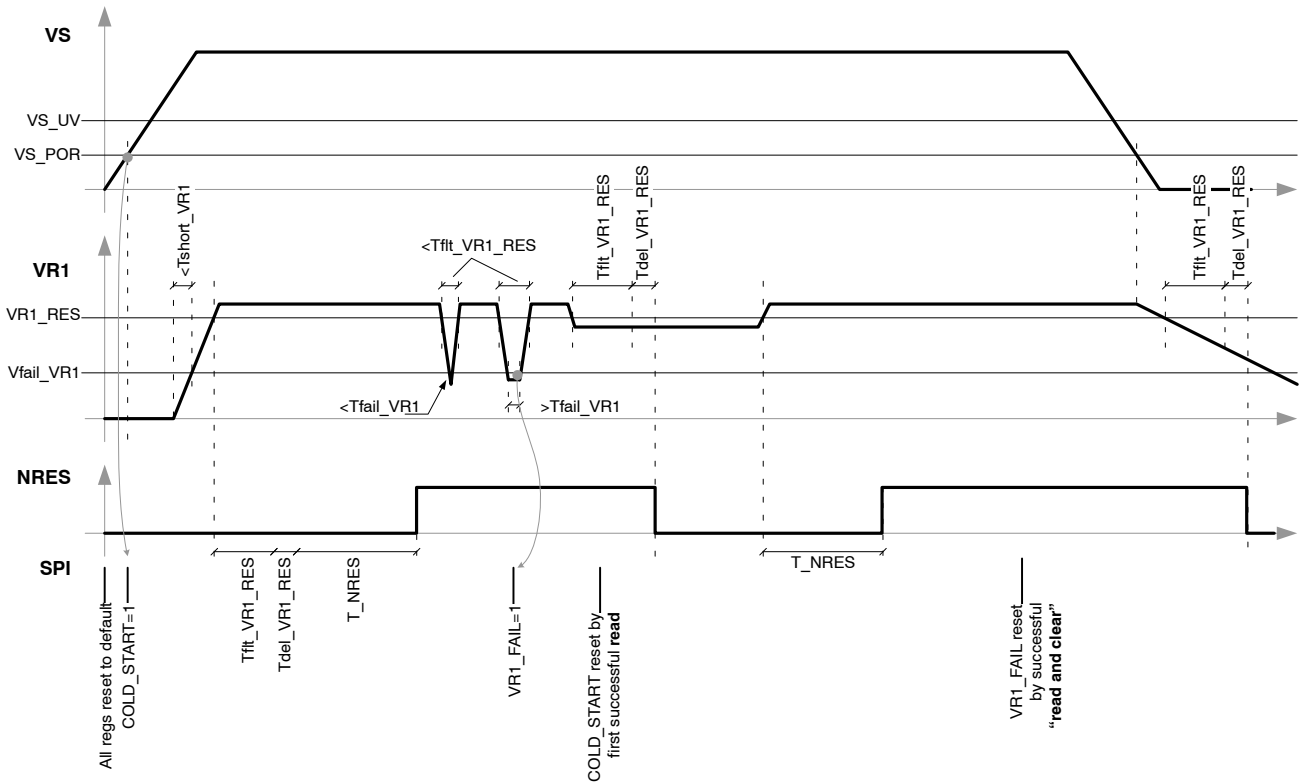


Figure 11. VR1 Monitoring

**Regulator VR2**

The device contains a second low-drop output regulator VR2, generating 5 V out of the VS main supply. The VR2 regulator can deliver up to 50 mA and is intended to supply additional 5 V loads – external sensors, potentiometers, logic etc. An external capacitor must be connected to the VR2 pin in order to provide stabilization and filtering.

It can also supply the on-chip CAN transceiver through the supply input pin VCC\_CAN. Because the VR2 current capability does not cover the worst-case CAN transceiver consumption (for dominant transmission and/or a short-circuit on the bus), the external filtering capacitor on VR2 must be carefully dimensioned with respect to the expected CAN bus traffic and relevant environmental conditions (bus terminations, possible cabling failures etc.).

VR2 is protected and monitored by:

- VR2 Current Limitation
- Junction Temperature Monitor – when the junction temperature exceeds the first shutdown level, all load drivers, including VR2, are disabled and the event is flagged through the corresponding SPI status bit – see par. “Thermal Protection” for details.
- VR2 Failure Monitor – during the VR2 start-up and operation in normal and cyclic-sense standby/sleep modes, the VR2 voltage is continuously compared with

$VR2\_FAIL$  level (typ. 2 V). Two types of events can be detected based on this comparison:

- ♦ During VR2 operation, any dip below  $VR2\_FAIL$  level longer than  $T_{fail\_VR2}$  (typ. 2  $\mu s$ ) is considered a transient failure. It is latched into the SPI bit “VR2\_FAIL” for subsequent software diagnosis. The regulator remains active.
- ♦ If VR2 does not rise above  $VR\_FAIL$  level within  $T_{short\_VR2}$  (typ. 4 ms) or dips below the failure level during operation for the same time, it’s considered shorted to ground and the regulator is disabled automatically. SPI bits “VR2\_FAIL” and “VR2\_SHORT” are both set. Read/clear access to both of them is needed before the regulator can be enabled again. The VR2-related control bits remain unchanged.
- Short circuit and Reverse-Biasing Protection – the internal topology of VR2 regulator sustains VR2 shorts to ground and to the VS supply including reverse polarization between VR2 and VS nodes (when the VR2 short is combined with missing supply of the application module). VR2 can be therefore used to supply also loads connected to the module via external cabling.

### CAN Transceiver Supply VCC\_CAN

The on-chip CAN transceiver block uses two supply paths:

- From the VCC\_CAN supply input: in the normal mode, when the transceiver is ready for transmission/reception.
- From the VS supply through internal pre-regulators – in standby and sleep modes, the transceiver monitors bus for remote wakeups. The VCC\_CAN supply is not used.

For correct CAN transceiver function in the normal mode, the VCC\_CAN pin must be decoupled with an external capacitor to ground.

In the normal operating mode, VCC\_CAN supply input is monitored with an under-voltage comparator with level Vfail\_VCAN (typ. 4.3 V). The output of the under-voltage detector can be read through SPI status bit “VCAN\_UV”. This bit is a direct read-out (without latching) of the comparator’s output. When the CAN transceiver is enabled, a VCC\_CAN under-voltage is additionally latched in the SPI status bit “VCAN\_FAIL” for subsequent diagnostics. CAN transceiver functionality is disabled during VCC\_CAN under-voltage.

### Communication Transceivers

#### LIN Transceiver

The NCV7462 on-chip LIN transceiver is an interface between a physical LIN bus and the LIN protocol controller. It is compatible to LIN2.x and J2602 specifications.

Unlike the CAN transceiver, the LIN is supplied solely from the VS pin and its state control is therefore simpler:

- In the normal mode of the device, LIN transceiver transmits dominant or recessive symbols on the LIN bus based on the logical level on TxDL pin. The signal received from the bus is indicated on RxDL pin. Both logical pins are referred to the VR1 supply. A resistive pull-up path of typ. 30 kΩ is internally connected between LIN and VS. LIN pin remains recessive regardless the TxDL pin state during VS under-voltage. See par “VS Over- and Under-Voltage” for details.
- In the standby and sleep modes of the device, the LIN transceiver is in its wakeup detection state. Logical level on TxDL is ignored and pin RxDL is kept high until it’s used as an interrupt request signal. A LIN bus wakeup corresponds to a dominant symbol at least T\_LIN\_wake long (typ. 90 μs) followed by a rising edge (i.e. transition to recessive) – see Figure 9. In this way, false wakeups due to permanent LIN dominant failures are avoided. Only a pull-up current of typ. 15 μA is connected between VS and LIN instead of the 30 kΩ pull-up path. The LIN wakeup detection is by default active in the standby and sleep modes and can be disabled via SPI control registers.

The LIN transceiver features SPI-configurable TxDL dominant time-out timer. This circuit, if enabled, prevents

the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxDL is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxDL. If the duration of the low-level on pin TxDL exceeds the internal timer value T\_TxDL\_timeout, the transmitter is disabled, driving the bus into a recessive state and the event is latched in the SPI status bit “TO\_TxDL”. The transmission is de-blocked when “TO\_TxDL” bit is reset by the corresponding register “read and clear”.

The LIN transceiver provides two LIN slope control modes, configured by SPI bit “LIN\_SLOPE”.

In normal slope mode the transceiver can transmit and receive data via LIN bus with speed up to 20 kBaud according LIN2.x specification. This mode is used by default.

In low slope mode the slew rate of the signal on the LIN bus is reduced (rising and falling edges of the LIN bus signal are longer). This further reduces the EMC emission. As a consequence the maximum speed on the LIN bus is reduced to 10 kBaud. This mode is suited for applications where the communication speed is not critical. The low slope mode can be configured by setting SPI bit “LIN\_SLOPE”.

#### CAN Transceiver

NCV7462 contains a high-speed CAN transceiver compliant with ISO11898-2 and ISO11898-5. It consists of the following sub-blocks: transmitter, receiver, wakeup detector, and common-mode stabilization pin VSPLIT

CAN transceiver control in the normal mode of the device is shown in Table 33. By default, the CAN transceiver is ready to provide the full-speed interface between the bus and a CAN controller connected on pins RxDC (received data) and TxDC (data to transmit). Through two dedicated SPI control bits, the CAN transceiver can be fully disabled or configured to “listen-only” functionality (RxDC pin continues to signal the received data while the logical level on TxDC is ignored and the transmitter remains in recessive).

The bus common mode can be additionally stabilized by using a split termination with the central tap connected to the VSPLIT pin. The transceiver and the VSPLIT are supplied from VCC\_CAN supply input. In order to prevent a faulty node from blocking the bus traffic, the maximum length of the transmitted dominant symbol is limited by a time-out counter to t\_TxDC\_timeout (typ. 650 μs). In case the TxDC Low signal exceeds the timeout value, the transmitter returns automatically to recessive and the event is latched in the SPI bit “TO\_TxDC”. The transmission is again de-blocked when “TO\_TxDC” bit is reset by the corresponding register “read and clear”.

When the CAN transceiver is enabled in the normal operating mode, an under-voltage of VCC\_CAN automatically blocks transmission and reception (recessive sent to the bus and RxDC remains High regardless the real CAN bus state). When the VCC\_CAN returns above the

under-voltage level, the logical path between the transceiver and the RxDC/TxDC pins is immediately restored.

**Table 33. CAN TRANSCEIVER CONTROL IN NORMAL MODE**

| Conditions and SPI Control |         |          | CAN Transceiver Behavior and SPI Flags |           |                  |               |         |                                       |
|----------------------------|---------|----------|--|-----------|------------------|---------------|---------|---------------------------------------|
| VCC_CAN                    | CAN_DIS | CAN_LSTO | Transceiver                            | VSPLIT    | TxDC             | RxDC          | VCAN_UV | VCAN_FAIL                             |
| >Vfail_VCAN                | 0       | 0        | on                                     | VCC_CAN/2 | data to transmit | received data | 0       | keeps previous state until read&clear |
|                            | 0       | 1        | on                                     | VCC_CAN/2 | ignored          | received data |         |                                       |
|                            | 1       | X        | powered-down                           | HZ        | ignored          | 1             |         |                                       |
| <Vfail_VCAN                | 0       | X        | on                                     | VCC_CAN/2 | ignored          | 1             | 1       | set to 1                              |
|                            | 1       | X        | powered-down                           | HZ        | ignored          | 1             |         |                                       |

In the standby and sleep modes of the device, the CAN transceiver is switched to a low-power state, in which only bus wakeup detection is possible. CANH/L pins are biased to ground via the input stage and the VSPLIT pin is kept high-impedant. A valid wakeup on the CAN bus is detected when two consecutive dominants at least t<sub>DBUS\_dom</sub> long (typ. 2.5 μs) are received, each of them followed by a recessive symbol at least t<sub>DBUS\_rec</sub> long (typ. 2.5 μs). RxDC signal remains logically connected to the low-power receiver – it therefore indicates the immediate bus state without waiting for the wakeup pattern. In the standby and sleep modes of the device, the CAN wakeup detection is by default enabled and can be disabled via SPI control registers prior to enter the respective low-power mode.

### High- and Low-Side Drivers

#### High-Side Drivers OUT1-4

High-side drivers OUT1-OUT4 are designed to supply mainly LED's or switches (for cyclic monitoring). When switched on, they connect the corresponding pin to the VS supply. Driver OUT1 can be configured to have two distinct levels of on-resistance: typically 2 Ω in “low-ohmic” and typically 7 Ω in “normal-ohmic” configuration (default). Drivers OUT2-4 have always a typical on-resistance of 7 Ω.

At the VS power-up or wakeup from the sleep mode, all OUT1-4 drivers are off. Immediately after the device enters the normal mode, they can be set to one of the following states via the corresponding SPI bits:

- Driver is off in all modes (default)
- Driver is on in all modes, except forced sleep mode
- Driver is activated periodically in all modes, except forced sleep mode. The periodicity is driven either by Timer 1 (period from 0.5 sec to 4 sec, on time 10 ms or 20 ms) or Timer 2 (period from 10 ms to 200 ms, on time 100 μs, 200 μs or 1 ms). Periodical activation can be used, for example, for LED flashing or cyclic contact monitoring.
- Driver is controlled by the on-chip PWM controller in the normal mode and standby or sleep mode with cyclic

sense active. Each OUTx driver has a dedicated 7-bit PWM duty cycle and the base frequency selectable through individual SPI settings.

The SPI settings for the drivers are applied immediately after the SPI frame is successfully completed (CSN rising edge). This can be done even immediately after the device initialization before the first watchdog service. If the watchdog trigger fails or VR1 under-voltage is detected, all drivers are immediately disabled and the SPI settings will be again applied once the watchdog is triggered correctly.

All OUTx outputs are protected by the following features in the normal and cyclic-sense standby and sleep modes:

- Over-current protection and current limitation: if the driver current exceeds the over-current limit for longer than T<sub>filt\_OLD\_OUTx</sub> (typ. 60 μs), the event is latched into the SPI status bits and the driver is disabled. It will be again enabled only when the corresponding SPI flag is read and cleared.
- Under-load detection: during the on-time of the driver, a too low current indicates missing load. The under-load event is latched into the corresponding SPI status bits; however, the driver is not disabled and is controlled according the SPI bits. The under-load detection threshold of OUT1 driver depends on its selected on-resistance.
- Thermal protection and VS under/over-voltage protection: through monitoring of the junction temperature and the VS supply voltage; all loads are protected as described in par. “Protection”.

OUT3 output is also intended for failure indication. By default, OUT3 switch is not controlled by the SPI settings but by the internal FSO signal – see section “Fail-Safe (FSO) Signal”. Only when the FSO signal is disconnected from OUT3 by setting SPI bit “FSO\_DIS”, OUT3 acts identically to OUT1, 2 and 4.

#### High-Side Driver OUT\_HS

OUT\_HS high-side driver is intended for LED's, switch monitoring as well as bulbs (5 W). The typical on resistance of OUT\_HS is 1 Ω. Its configuration and protection features

are identical to the OUTx high-side drivers, only with different parametrical values.

At the VS power-up or wakeup from the sleep mode, OUT\_HS driver is off. Immediately after the device enters the normal mode, it can be set to one of the following states via the corresponding SPI bits:

- Off in all modes (default)
- On in all modes, except forced sleep mode
- Periodical activation controlled by Timer 1 or Timer 2 in all modes, except forced sleep mode
- PWM control in normal mode and standby or sleep mode with cyclic sense active

OUT\_HS output is protected by the following features in normal and cyclic-sense standby and sleep modes:

- Over-current protection and current limitation
- Under-load detection
- Thermal protection and VS under/over-voltage protection

Additionally, OUT\_HS can be configured to bypass the over-current protection in case the connected load requires an important initial driving current (typically the inrush current with incandescent bulbs). This feature is referred to as over-current auto-recovery. An over-current on OUT\_HS longer than Tblank\_OLD\_OUT\_HS (typ. 120  $\mu$ s) will be latched to the SPI status bit and the driver will be switched off. However, if the SPI control bit "OUT\_HS\_OCR" is set high, OUT\_HS will be automatically re-activated after Tflt\_OCR (typ. 400  $\mu$ s) and no SPI status bit "OUT\_HS\_OC" is set. If the over-current condition persists, the driver enters into oscillations with typ. 120  $\mu$ s on, 400  $\mu$ s off (exact values depending on the load character). Typically, the MCU software will disable the auto-recovery once the load is supposed to settle (e.g. the bulb is heated up).

#### Low-Side Drivers LS1/2

NCV7462 offers two low-side drivers LS1 and LS2 primarily intended to drive relays, typically:

- R = 160  $\Omega \pm 10\%$ , L = 240/300 mH
- R = 220  $\Omega \pm 10\%$ , L = 330/420 mH

For the relay demagnetization, LS1/2 drivers feature active flyback clamps towards ground (no diode to VS) allowing to keep the load off even under load-dump condition on VS. Alternatively, LS1/2 can drive LED's.

LS1/2 can be configured in one of the following states:

- Off in all modes (default)
- On in the normal mode; off in all other modes
- Controlled by individual PWM in the normal mode; off in all other modes

LS1/2 is protected by:

- Over-current protection and current limitation: if the driver current exceeds the over-current limit for longer than Tflt\_OLD\_LS1/2 (typ. 60  $\mu$ s), the event is latched

into the SPI status bits and the driver is disabled. It will be again enabled only when the corresponding SPI flag is read and cleared.

- Thermal protection and VS under/over-voltage protection: through monitoring of the junction temperature and the VS supply voltage; all loads are protected as described in par. "Protection".

#### INH Output

INH high-side output is primarily intended to control an external regulator or the LIN master pull-up (see Figure 3). When the driver is active, it connects INH pin to the VS supply through a switch (on resistance typ. 23  $\Omega$ ).

By default, INH is on in the normal mode and off in the standby and sleep modes. It can be switched off in all modes by setting SPI control bit "INH\_OFF" high.

INH driver is neither over-current nor under-load protected – the output current is limited but INH will not be automatically switched off in case a current limitation is encountered. In the normal mode, it will be always switched off in case of the second thermal shutdown.

#### Wake-up Inputs WU1-3

NCV7462 offers three independent contact-monitoring inputs WU1-3 which can be used either for normal-mode contact polling or for contact change detection during the standby and sleep modes. In any mode, every WUx input can be configured into one of the following modes of operation:

- Static sense: the corresponding WUx input is constantly monitored by an input comparator and a filter of typ. 64  $\mu$ s. In the normal mode, the result of the comparison (the input high/low state) can be polled any time through the SPI status bits. In the standby and sleep modes, a change of the WUx polarity (in any direction) is recognized as a wakeup event. The MCU can then recognize the exact WUx wakeup source by reading "WU\_WUx" SPI status bits.
- Cyclic sense: the WUx state detection is performed periodically as fostered by one of the internal timers: Timer 1 (period from 0.5 sec to 4 sec, WUx is left to settle for 800  $\mu$ s and the state detection is then done through a filter of typ. 16  $\mu$ s) or Timer 2 (period from 10 ms to 200 ms, on WUx is left to settle for 80  $\mu$ s or 800  $\mu$ s and the state detection is then done through a filter of typ. 16  $\mu$ s). The result of the periodical state detection is latched into the SPI status register and is not updated until the next period of the selected timer. A wakeup is detected in case sample of the WUx state changes in any direction.

Additionally, each WU1-3 input can be internally pre-biased by a pull-up or pull-down current source through individual control bits. If corresponding WUx wakeup is disabled, the pull-up current source is active in the normal mode only.

**Table 34. WU1–3 PULL–DOWN / PULL–UP CONFIGURATION**

| Mode    | WUx_DIS = 0 |             | WUx_DIS=1   |             |
|---------|-------------|-------------|-------------|-------------|
|         | WUx_PUD = 0 | WUx_PUD = 1 | WUx_PUD = 0 | WUx_PUD = 1 |
| Normal  | pull-down   | pull-up     | pull-down   | pull-up     |
| Standby | pull-down   | pull-up     | pull-down   | floating    |
| Sleep   | pull-down   | pull-up     | pull-down   | floating    |

In case cyclic sense is used, the WUx timer settings must be correctly chosen together with the high-side output settings. The driver physically ensuring the periodical contact supply must be set for the same timer as the contact monitor by the MCU software.

**Operating Modes**

NCV7462 can be configured to different operating modes in function of the application needs and the external conditions. The device resources can be enabled/disabled and the overall power consumption can be adapted to the electronic module state – ranging from full power mode down to a very low quiescent current “sleep” mode. The principal operating modes of NCV7462 are shown in Figure 12.

**Un–Powered and Init Modes**

As long as VS remains below the VS\_POR level (typ. 3.45 V), the device is held in power-up reset. All outputs except NRES are in high–impedant state, the linear regulator outputs are off.

As soon as the VS main supply exceeds the power-on reset level, the device enters an initialization sequence represented by a transient “init” mode. All SPI registers are set to their default values, “COLD\_START” SPI bit is set high for subsequent diagnostics and the VR1 regulator is started. After a successful start of the VR1 regulator (i.e. VR1 exceeds the VR1\_FAIL level in less than Tshort\_VR1 – typ. 4 ms), NRES is still kept low until VR1 reaches its reset level. After another 2 ms (parameter T\_NRES), NRES is released to high and the device enters Normal mode with timeout watchdog.

In case VR1 does not start within Tshort\_VR1, it’s again disabled, SPI “VR1\_FAIL” bit is set and the device is forced into sleep mode. The forced sleep mode can be exited via any valid wakeup event or by VS re-connection. The initialization sequence is shown in Figure 11.

**Normal Mode**

In this mode the device provides full functionality, all resources are available. The voltage regulator VR1 is able to source 250 mA. MCU can enable/disable the device features via SPI as well as monitor the status of the device.

VR1 level is monitored through reset and failure comparators – see Figure 11. When the normal mode is entered, the watchdog is started in a timeout mode; a window watchdog mode is applied after the first correct watchdog service. The watchdog has to be correctly

triggered; otherwise a watchdog failure is detected resulting in reset signal to the MCU. Afterwards the watchdog is re-started in the timeout mode. After eight consecutive watchdog failures, the VR1 regulator is disabled for 200 ms and then re-started again. If the watchdog service still fails seven more times, the device is forced into sleep mode – the forced sleep mode can then be exited either via a wakeup or VS re-connection.

Through SPI bits “MOD\_STBY” and “MOD\_SLEEP”, the MCU can either keep the device in the normal mode, or request transition into one of the low-power modes – standby or sleep.

**Standby Mode**

Standby mode is the first low-power mode. The voltage regulator VR1 remains active while the watchdog is disabled. The standby mode is mainly intended to keep the application powered (e.g. for RAM content preservation) while the MCU is in a halt-state (software not running).

In order to make a safe transition into the standby mode, the watchdog will remain enabled even in the standby mode until the consumption from VR1 decreases below Icmp\_VR1\_fall level (typ. 1.1 mA). When the VR1 consumption increases back above Icmp\_VR1\_rise level (typ. 1.7 mA), the device will perform a wakeup from the standby mode to ensure supervision of the MCU software. The current supervision of VR1 can be disabled via SPI by setting the bit “ICMP\_STBY”. VR1 also continues to be monitored by the reset circuit, which will generate a low NRES pulse in case the regulator output drops below the reset level.

During the standby mode, several types of wakeup events can be signaled to the MCU through INTN pin: timer1 or timer2 expiration, wakeup on CAN or LIN buses, change on WUx pin (as per the SPI settings), or SPI activity. Increased consumption from VR1 is not signaled through INTN pin. After a wakeup, the watchdog is started in timeout mode and MCU can request a mode transition afterwards.

**Sleep Mode**

Sleep mode is the mode with the lowest consumption. VR1 regulator and the watchdog are inactive. The device maintains minimum operation allowing reception of wake-up events generated by the pins WUx (as per SPI settings), LIN and CAN bus line or driven by timer1 or timer2. In case of a wake-up event the device switches from



the sleep mode to the normal mode (through the init mode, as the VR1 must be started similarly to the VS power-up).

### Forced Sleep Mode

Forced sleep mode is the mode equal to the sleep mode, but all peripherals (VR1/2, OUT\_HS, OUT1–4, LS1/2) and the watchdog are inactive.

Forced sleep mode is entered after following failure conditions:

- VR1 did not reach Vfail\_VR1 level (typ. 2 V) within Tshort\_VR1 during startup (VS connection or wakeup from sleep mode)
- Fifteen consecutive watchdog failures occur
- The device junction temperature exceeded thermal shutdown level Tsd2 (typ. 155°C) for eight times within one minute

### Flash Mode

Flash mode is identical to the normal mode with the exception of the watchdog which is disabled. Neither the standby nor sleep mode can be entered (the corresponding SPI requests will be ignored). The purpose of the flash mode is to enable transfer of bigger bulk of data between the MCU and a programming interface – typically during the module-level production. The flash mode will be entered if the voltage applied on TxDL or TxDC pin exceeds the corresponding comparison level VinH\_FLASH (typ. VR1 + 3.3 V).

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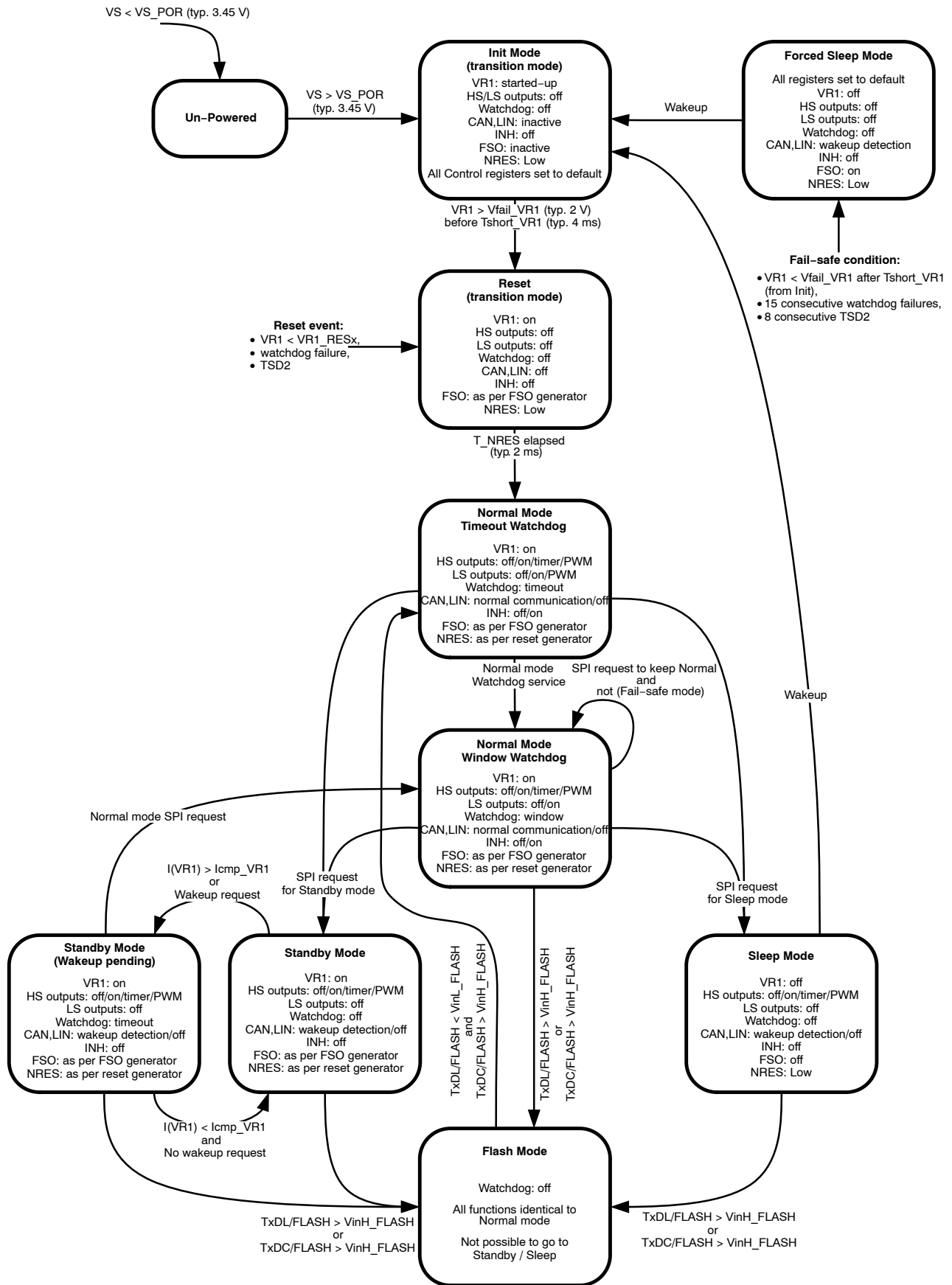


Figure 12. Principal Operating Modes

**Wake-up Events**

In the standby and sleep modes, NCV7462 can detect several types of wake-up events summarized in Table 35:

- In the sleep modes, a wakeup will cause a reset (low signal at NRES pin) and initialization of VR1 regulator. After the release of the NRES signal, the timeout watchdog will be started and the device enters the normal mode and SPI registers will be set into their default values. The following events will cause wakeup from the sleep mode:
  - ◆ Bus wakeups through CAN or LIN – can be enabled/disabled through SPI
  - ◆ Switch monitoring on WUx inputs – can be configured and enabled/disabled through SPI
  - ◆ Timer wakeup – timer1 and timer2 can be configured to cause a wakeup after a fixed time period – the selected timer is started at the moment the sleep mode is requested and causes wakeup immediately when the selected time period expires. The timer wakeup can be configured and enabled/disabled by SPI.
- From the standby mode, where VR1 remains active, a wakeup event will cause watchdog startup in timeout mode:
  - ◆ SPI wakeup (CSN low and rising edge on SCLK). Interrupt request is generated.
  - ◆ VR1 consumption wakeup (VR1 consumption exceeds the Icmp\_VR1\_rise level; can be disabled by SPI control). No interrupt request is generated. If

VR1 consumption falls below the Icmp\_VR1\_fall level within the timeout period, the watchdog is disabled again.

- ◆ Bus wakeups through CAN or LIN, switch monitoring on WUx and timer wakeups have the same meaning as in the sleep mode. Any of them will cause an interrupt request.

Every valid wakeup event starts the timeout watchdog, which then must be correctly triggered. If another wakeup event occurs during the initial timeout watchdog, it will be only registered into the SPI status and will not cause an interrupt or re-start of the watchdog. E.g., an increase of the VR1 consumption will start the watchdog timeout timer while the device remains in the standby mode. If, for example, a CAN wakeup is then detected, it will be latched into the SPI registers, but no new interrupt will be generated and the watchdog will keep running.

In all wakeup cases in the standby mode the device remains in the standby mode until it is changed. SPI settings for drivers and VR2 are applied after the correct watchdog service.

In case all wakeup sources are disabled while the standby or sleep mode is entered through a SPI request, LIN and CAN wakeups are automatically enabled (SPI bits “WU\_LIN\_DIS” and “WU\_CAN\_DIS” are ignored). If all the wakeup sources are disabled prior to the standby mode entry and CAN or LIN wakeup occurs in the standby mode, the watchdog is started and has to be served within typ. 1.5 ms. Otherwise, NRES pulse is generated and all the SPI registers are set into their default states.

**Table 35. WAKEUP EVENTS**

| Device Mode  | Wakeup Event            | SPI Default | SPI Control                           | NRES Pulse | INTN Pulse |
|--------------|-------------------------|-------------|---------------------------------------|------------|------------|
| Standby      | SPI                     | N/A         | cannot be disabled                    | no         | yes        |
|              | I(VR1) > Icmp           | enabled     | can be enabled/disabled               |            | no         |
|              | Bus wakeup (CAN or LIN) | enabled     |                                       |            | yes        |
|              | WU1-3 change            | enabled     |                                       |            |            |
|              | Timer1/2 wakeup         | disabled    |                                       |            |            |
| Sleep        | Bus wakeup (CAN or LIN) | enabled     | can be enabled/disabled               | yes        | no         |
|              | WU1-3 change            | enabled     |                                       |            |            |
|              | Timer1/2 wakeup         | disabled    |                                       |            |            |
| Forced Sleep | Bus wakeup (CAN or LIN) | enabled     | previous SPI configuration maintained | yes        | no         |
|              | WU1-3 change            | enabled     |                                       |            |            |
|              | Timer1/2 wakeup         | disabled    |                                       |            |            |

**Watchdog**

The on-chip watchdog requires that the MCU software sends specific SPI messages (watchdog “triggers” or “services”) in a specified time frame. A correct watchdog trigger/service consists of a write access to SPI register CONTROL\_0 with “WD\_TRIG” bit inverted compared to its previous state. The watchdog timer re-starts immediately after a successful trigger is received.

A read access to the CONTROL\_0 register or a write access with “WD\_TRIG” bit unchanged does not trigger the watchdog. The moment of the watchdog trigger corresponds to the rising edge of the CSN signal (end of the SPI frame). The watchdog can work in the following modes (see Figures 13 and 14):

- Off; the watchdog is always off in the sleep and flash modes. It is also off in the standby mode, provided that the VR1 consumption stays below the Icmp limit, or when the Icmp comparator is disabled.
- Timeout: the watchdog works as a timeout timer. The MCU software must serve the watchdog any time before the time-out expiration (typ. 65 ms). Timeout watchdog is started after reset events (power-up, watchdog failure, VR1 under-voltage in normal mode, thermal shutdown 2) and by any wakeup event from both standby and sleep mode. The timeout watchdog is started regardless if the wakeup is or is not accompanied by a reset. Watchdog counter position is reflected in SPI status bits “WD\_STATUS[1:0]”.

- Window: the watchdog time is split to two distinct parts – a closed window, where the watchdog may not be triggered, is followed by an open window where the MCU must send a valid watchdog trigger. Window watchdog is used during the normal operating mode of the device after the initial timeout watchdog is correctly triggered. Position of the watchdog counter inside the open window is reflected in SPI status bits “WD\_STATUS[1:0]”.
- Failure: If the watchdog is not triggered correctly (trigger not sent during timeout or open window; or sent during the closed window), reset is generated on pin NRES and the “WD\_TRIG” bit is reset to low. After the NRES release, the watchdog always starts in the timeout mode. Watchdog failures are counted and their number can be read from the SPI status registers. After eight watchdog failures in sequence, the VR1 regulator is switched off for 200 ms. In case of seven more watchdog failures, VR1 is completely turned off and the device goes into forced sleep mode until a wake-up occurs (e.g. via the LIN or CAN bus). First successful watchdog trigger resets the failure counter. The watchdog time for window mode is selectable from four different values by SPI bits “WD\_PER[1:0]”. The watchdog time setting is applied only if it’s contained in an SPI frame representing a correct watchdog trigger message. The setting is ignored otherwise.

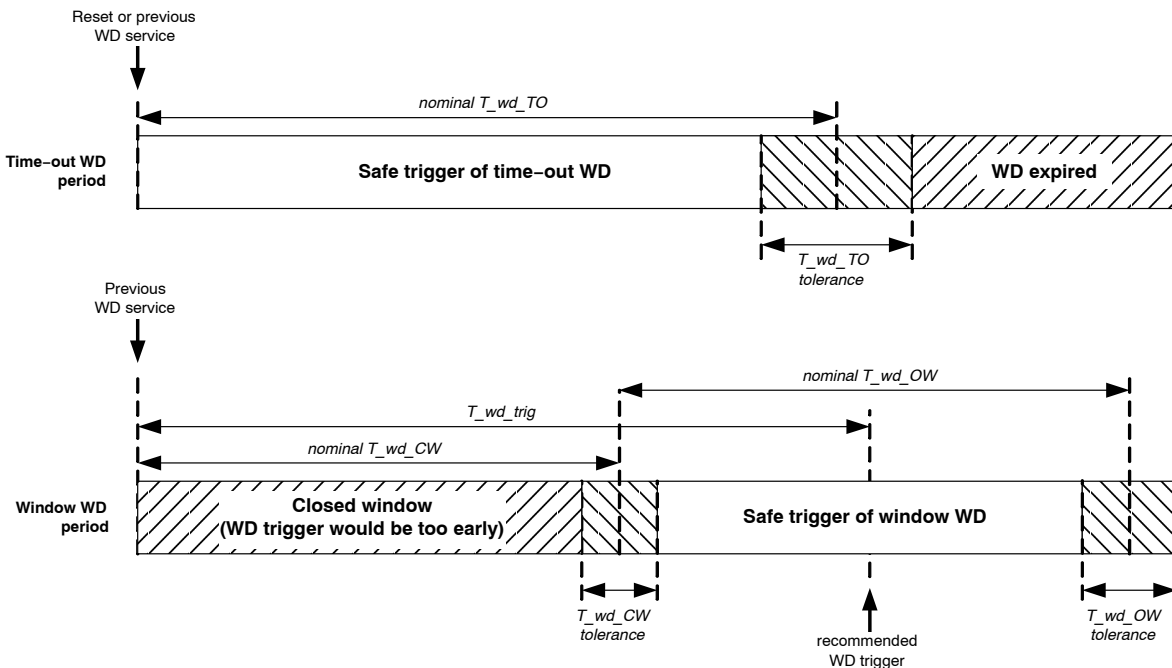


Figure 13. Watchdog Modes Timing

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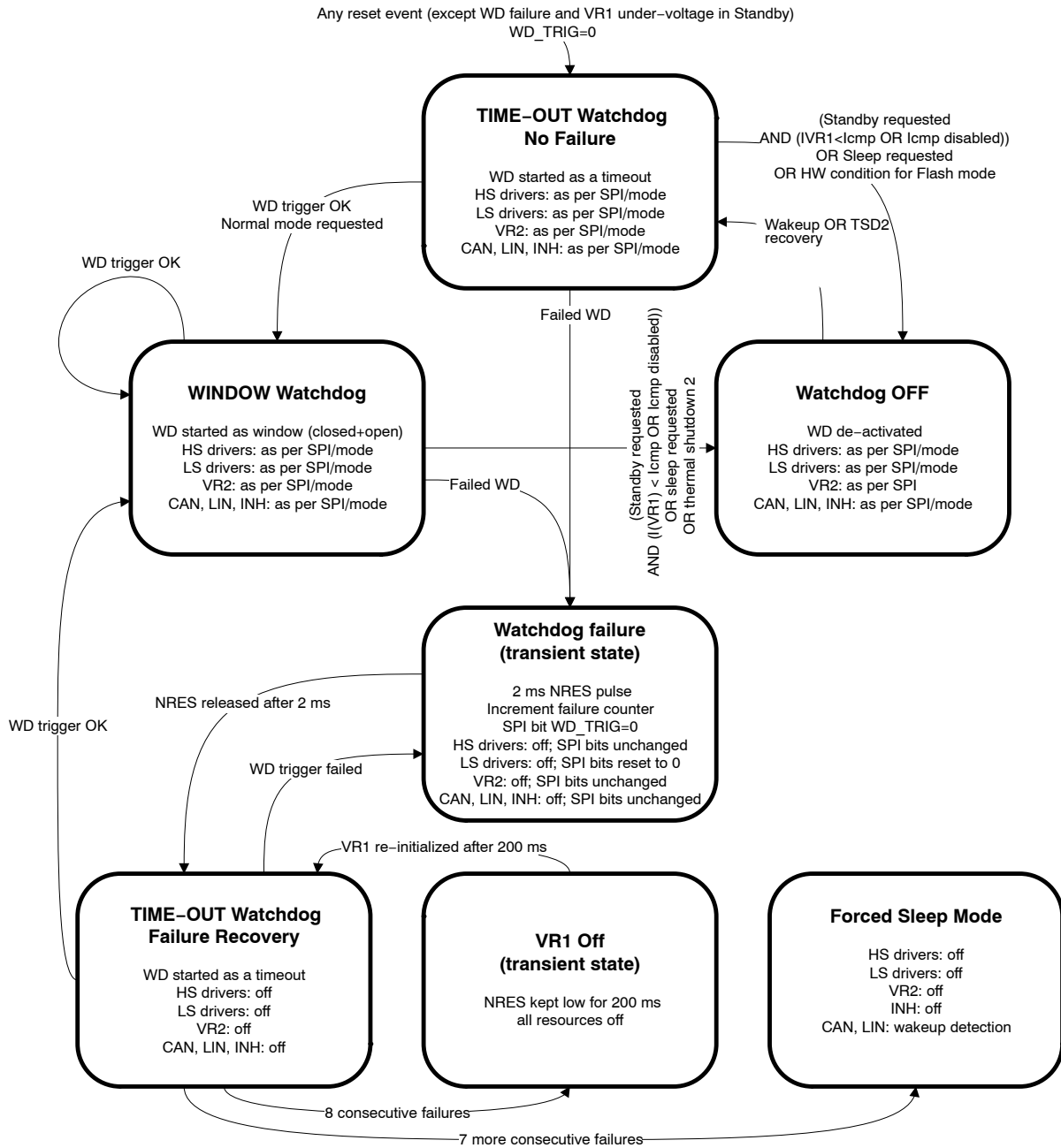


Figure 14. Watchdog Operation

**Protection**

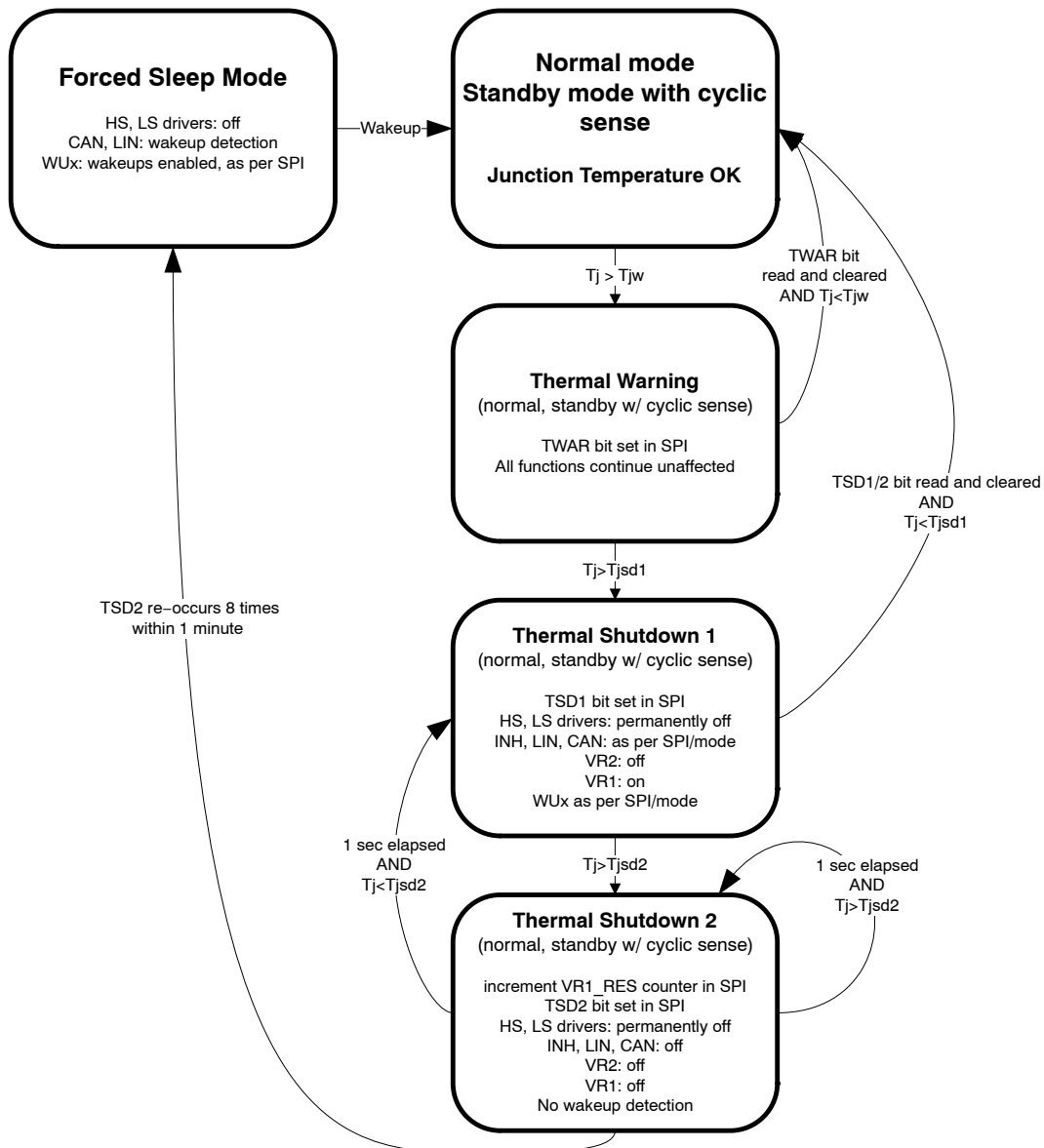
**Thermal Protection**

The device junction temperature is monitored in order to avoid permanent degradation or damage. Three distinct junction temperature levels are provided – thermal warning level  $T_{jw}$  (typ.  $130^{\circ}\text{C}$ ), thermal shutdown level 1  $T_{j\text{sd}1}$  (typ.  $140^{\circ}\text{C}$ ) and thermal shutdown level 2  $T_{j\text{sd}2}$  (typ.  $155^{\circ}\text{C}$ ). The thermal protection circuit is always active in the normal mode. It is also active in the standby and sleep modes if any of the high-side outputs is used for cyclic switch monitoring.

When the junction temperature exceeds the warning level, the event is only latched into the SPI for subsequent diagnostics without any direct effect on the device

configuration. When the first thermal shutdown level is exceeded, most of the power-consuming functions are disabled (high- and low- side drivers, VR2) while VR1 keeps running so that the MCU can still take appropriate actions. Junction temperature above the second shutdown level leads to complete device de-activation, VR1 included. VR1 is re-started after a waiting time of one second in case the junction temperature drops below the second shutdown level. If the second thermal shutdown then re-occurs eight times within 1 minute, the device is forced into the sleep mode.

The details of the thermal protection handling are shown in Figure 15 (for normal mode and standby mode with cyclic sense) and in Figure 16 (for sleep mode with cyclic sense).



**Figure 15. Thermal Protection in Normal and Standby Modes**

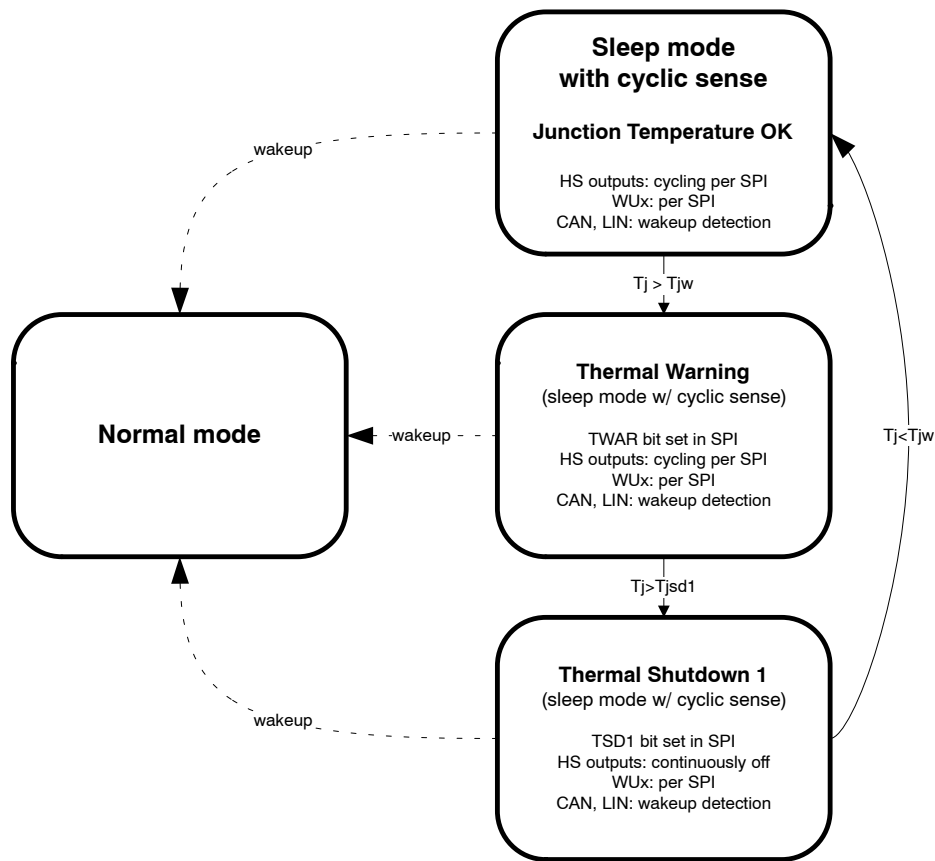


Figure 16. Thermal Protection in Sleep Mode

**VS Over- and Under-Voltage**

In order to protect the loads connected to the high- and low- side drivers, the VS (car battery) supply is compared against two levels – under-voltage level VS\_UV (typ. 5.5 V) and VS\_OV (typ. 21 V). The VS monitoring circuitry is active in normal mode as well as in the standby and sleep modes when any high-side output is used for cyclic switch monitoring.

Whenever VS falls below the VS\_UV level or rises above VS\_OV level, all high-side drivers are disabled. The under/over-voltage event is latched in the corresponding SPI status bit. If the SPI control bit “LS\_OVUV” is low, the same action is taken for the low-side drivers. After the VS under/over-voltage condition disappears, it remains flagged in the SPI status. If the SPI control bit “VS\_LOCKOUT\_DIS” is low, the drivers will remain deactivated until the corresponding flag is not read and

cleared. If “VS\_LOCKOUT\_DIS” is high, the drivers will return to their state defined by SPI registers settings. The details of the VS monitoring are shown in Figure 17.

SPI control bit “VS\_LOCKOUT\_DIS” is ignored by OUT3 driver in case it is controlled by FSO signal. OUT3 will return to the previous state immediately after VS under/over-voltage disappears.

Whenever VS falls below the VS\_UV level, the LIN transmitter is disabled. If VS under-voltage condition disappears and SPI control bit “VS\_LOCKOUT\_DIS” is low, LIN transmission is blocked until SPI flag “VS\_UV” is not read and cleared. If “VS\_LOCKOUT\_DIS” is high, LIN transmission is possible immediately when VS voltage returns above VS\_UV threshold. A falling edge on TxDL pin is needed to start LIN transmission, to prevent unwanted glitches on LIN bus.

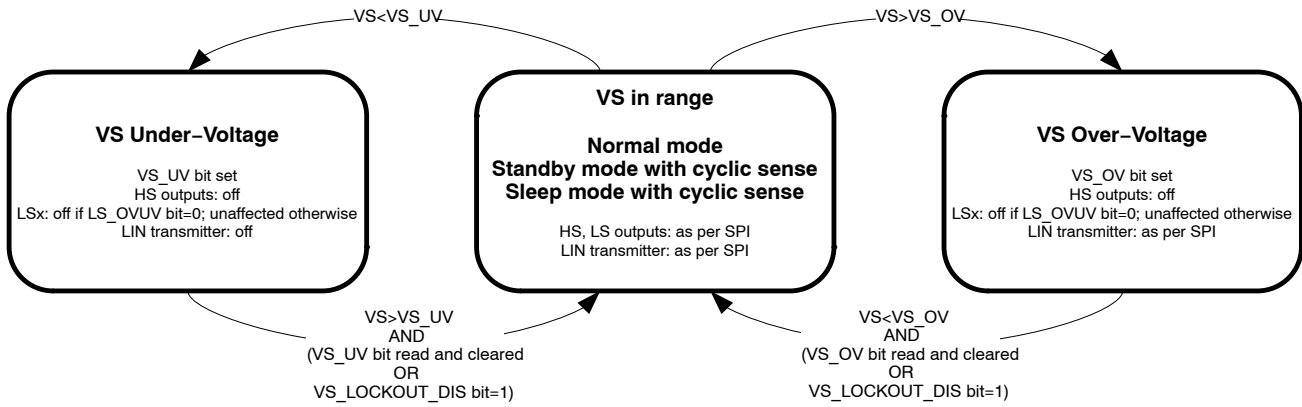


Figure 17. Under- and Over-voltage on VS Supply

### Reset Signal NRES

NRES is an open-drain output with an internal pull-up resistor connected to VR1. It signals reset to the MCU as a consequence of several specific events:

- VR1 under-voltage (including VS power-up)
- Watchdog failure
- Thermal shutdown level 2
- Wakeup (in case the wakeup is accompanied by reset – see Table 35)
- (Forced) Sleep mode

The low-level pulse on NRES pins always extends  $T_{NRES}$  (typ. 2 ms) beyond the reset event – e.g. a watchdog failure causes a 2 ms NRES low pulse; a VR1 under-voltage causes NRES pulse extending 2 ms beyond the under-voltage disappearance.

After NRES pulse, which was caused by VR1 under-voltage or watchdog failure, all outputs (OUT1–4, LS1/2 and VR2) are inactive. SPI registers content is preserved. Outputs follow relevant SPI register settings after the correct watchdog setting again.

LIN and CAN transmission is blocked during NRES pulse. CAN and LIN receivers are enabled if NRES pulse was caused by VR1 undervoltage, disabled otherwise. A recessive-to-dominant edge on TxDL pin after NRES pulse is required to start transmission to LIN bus.

### Interrupt Signal

An interrupt request is used in the standby mode to indicate some of the wakeup events to the MCU – see section “Wake-up Events”. Interrupt is signaled through RxDL pin by pulling it Low for typically 125  $\mu$ s. Beside the 125  $\mu$ s Low pulse, RxDL remains High throughout the standby mode.

During normal mode, RxDL assumes its normal function (LIN received data).

### Operational Amplifiers

Two operating amplifiers are provided for, mainly, current sensing (see Figure 3). The operating amplifiers are on (i.e.

biased) in the normal mode. They are powered-down in all other modes.

The input voltage common mode covers the range from –0.2 V to 3 V. The rail-to-rail (VS) output voltage allows using them together with an external pass element as additional voltage regulator.

### Fail-Safe (FSO) Signal

A fail-safe signal is internally generated reflecting some critical system failures and events. By default, the signal is connected to the OUT3 output and over-rides the OUT3 SPI settings – active FSO signal switches OUT3 on, inactive FSO signal switches OUT3 off. In case the SPI bit “FSO\_DIS” is set, OUT3 acts as a general-purpose high-side driver identically to OUT1, 2 and 4. FSO remains then only an internal signal not visible to the application.

FSO internal signal is active in the following cases:

- During the Init phase:
  - ♦ VR1 short: FSO is active when VR1 is below its failure level ( $V_{fail\_VR1}$ ) for more than  $T_{short\_VR1}$  (typ. 4 ms) during VR1 regulator startup and VS is above  $VS_{UV}$  threshold (typ. 5.5 V).
- In the normal and standby modes:
  - ♦ VR1 under-voltage: FSO is active when VR1 is below its reset level ( $VR1\_RES$ ).
  - ♦ Watchdog: FSO is immediately activated in case of failed watchdog trigger. It is deactivated only when the watchdog is correctly triggered again.
  - ♦ Thermal shutdown: FSO is active when the junction temperature is above the second shutdown threshold ( $T_{jsd2}$ ).
- In the forced sleep modes: FSO is active if the forced sleep mode was entered because of a failure condition, like non-starting VR1, repeated thermal shutdown or repeated watchdog failures. If the sleep mode is entered by a correct SPI mode-transition request, FSO remains inactive.



SPI CONTROL

Serial Peripheral Interface (SPI) is the main communication channel between the application MCU and NCV7462. The structure of a SPI frame is shown in Figure 18. MCU starts the frame by sending an 8-bit header consisting of two bits of register access mode type followed by a six-bit address. During the header transmission, NCV7462 sends out eight bits of status information regardless the address. After the header, sixteen bits of data are exchanged. A correct SPI frame has either no bits (no SCLK edges during CSN low; serves to read out the global status information) or exactly twenty-four bits. If another amount of clock edges occurs during CSN low, the frame is considered incorrect and the input data are always ignored.

Depending on the access type, the transmitted/received data are treated differently:

- ◆ During a write access, SDO signals current content of the register while new data for the same register are received on SDI. The register is refreshed with the new data after a successful completion of the

frame (rising edge on CSN). Only the bits eligible for write access are refreshed, the input data are ignored for the others (e.g. a write access to status registers).

- ◆ For read access, the data on SDI are ignored; SDO signals data content of the register addressed by the header. After the frame completion, the register content remains unchanged regardless the type of the individual bits.
- ◆ For read and clear access, a normal register read is performed. When the frame is completed (CSN rising edge), the register bits eligible for read/clear access are reset to 0.
- ◆ Device ROM access switches the address space to sixteen-bit constant data memorized in the NCV7462 (indicating the device version, SPI frame format and other information). Input data are ignored.

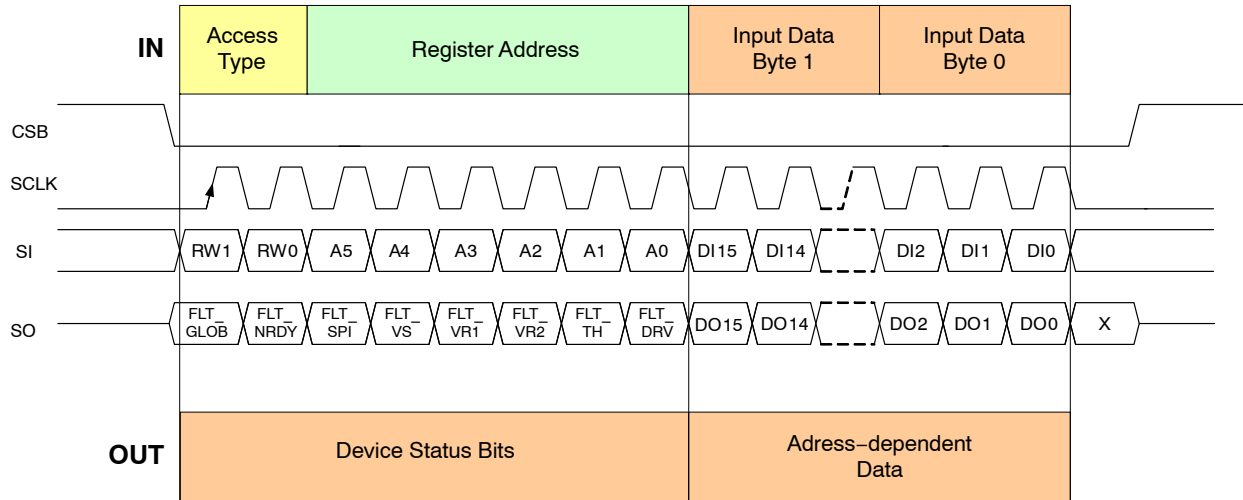


Figure 18. SPI Frame

## NCV7462

### SPI Frame Format

|             |          |          |         |        |         |         |        |         |      |     |     |
|-------------|----------|----------|---------|--------|---------|---------|--------|---------|------|-----|-----|
|             | D23      | D22      | D21     | D20    | D19     | D18     | D17    | D16     | D15  | ... | D0  |
| NCV7462 IN  | RW1      | RW0      | A5      | A4     | A3      | A2      | A1     | A0      | D15  | ... | D10 |
| NCV7462 OUT | FLT_GLOB | FLT_NRDY | FLT_SPI | FLT_VS | FLT_VR1 | FLT_VR2 | FLT_TH | FLT_DRV | DO15 | ... | DO0 |

### Inframe:

| SPI Access Type | RW1 | RW0 | Description                 |
|-----------------|-----|-----|-----------------------------|
|                 | 0   | 0   | Write to SPI register       |
|                 | 0   | 1   | Read only from SPI register |
|                 | 1   | 0   | Read and clear SPI register |
|                 | 1   | 1   | Access device ROM           |

| SPI Registers | A5 | A4 | A3 | A2 | A1 | A0 | Register   |
|---------------|----|----|----|----|----|----|------------|
|               | 0  | 0  | 0  | 0  | 0  | 0  | CONTROL_0  |
|               | 0  | 0  | 0  | 0  | 0  | 1  | CONTROL_1  |
|               | 0  | 0  | 0  | 0  | 1  | 0  | CONTROL_2  |
|               | 0  | 0  | 0  | 0  | 1  | 1  | CONTROL_3  |
|               | 0  | 0  | 0  | 1  | 0  | 0  | CONTROL_4  |
|               | 0  | 0  | 0  | 1  | 0  | 1  | PWM_HS     |
|               | 0  | 0  | 0  | 1  | 1  | 0  | PWM_OUT1/2 |
|               | 0  | 0  | 0  | 1  | 1  | 1  | PWM_OUT3/4 |
|               | 0  | 0  | 1  | 0  | 0  | 0  | PWM_LS     |
|               | 0  | 0  | 1  | 0  | 0  | 1  | STATUS_0   |
|               | 0  | 0  | 1  | 0  | 1  | 0  | STATUS_1   |
|               | 0  | 0  | 1  | 0  | 1  | 1  | STATUS_2   |
|               | 0  | 0  | 1  | 1  | X  | X  | reserved   |
|               | 0  | 1  | X  | X  | X  | X  | reserved   |
|               | 1  | X  | X  | X  | X  | X  | reserved   |

| Device ROM | A5  | A4  | A3  | A2  | A1  | A0  | Data content     | Comment         |
|------------|-----|-----|-----|-----|-----|-----|------------------|-----------------|
|            | 0   | 0   | 0   | 0   | 0   | 0   | \$4300           | ID_HEADER       |
|            | 0   | 0   | 0   | 0   | 0   | 1   | \$4404 or \$5104 | PRODUCT VERSION |
|            | 0   | 0   | 0   | 0   | 1   | 0   | \$7400           | PRODUCT CODE 1  |
|            | 0   | 0   | 0   | 0   | 1   | 1   | \$6200           | PRODUCT CODE 2  |
|            | 0   | 0   | 0   | 1   | 0   | 0   | reserved         |                 |
|            | ... | ... | ... | ... | ... | ... | reserved         |                 |
|            | 1   | 1   | 1   | 1   | 0   | 1   | reserved         |                 |
|            | 1   | 1   | 1   | 1   | 1   | 0   | \$0200           | SPI_FRAME_ID    |
|            | 1   | 1   | 1   | 1   | 1   | 1   | reserved         |                 |

**Outframe:**

| General Device Status Info | SDO bit | Bit Name | Bit Content  |
|----------------------------|---------|----------|--|
|                            | D23     | FLT_GLOB | Logical combination (OR) of all following flags  |
|                            | D22     | FLT_NRDY | reserved   |
|                            | D21     | FLT_SPI  | Previous SPI frame faulty – wrong number of clocks or addressing a nonexistent address |
|                            | D20     | FLT_VS   | VS_OV OR VS_UV   |
|                            | D19     | FLT_VR1  | Equal to VR1_FAIL bit  |
|                            | D18     | FLT_VR2  | VR2_FAIL OR VR2_SHORT  |
|                            | D17     | FLT_TH   | TSD2 OR TSD1 OR TWAR   |
|                            | D16     | FLT_DRV  | OR combination of all overcurrent and underload bits of OUT_HS, OUTx and LSx           |

**SPI Registers Overview**

In the below register overview, each bit is marked with the available SPI access. Every bit can be read. Those marked “RW” can be additionally written to; bits marked “R/RC” can be additionally read and cleared.

**SPI REGISTERS OVERVIEW**

| CONTROL_0 | D15       | D14       | D13     | D12      | D11       | D10       | D9        | D8       |
|-----------|-----------|-----------|---------|----------|-----------|-----------|-----------|----------|
|           | RW        | RW        | RW      | RW       | RW        | RW        | RW        | RW       |
|           | MOD_STBY  | MOD_SLEEP | WD_TRIG | WD_PER.1 | WD_PER.0  | ICMP_STBY | VR2_ON.1  | VR2_ON.0 |
| CONTROL_0 | D7        | D6        | D5      | D4       | D3        | D2        | D1        | D0       |
|           | RW        | RW        | RW      | RW       | RW        | RW        | RW        | RW       |
|           | VR1_RES.1 | VR1_RES.0 | CAN_DIS | CAN_LSTO | LIN_SLOPE | TXDL_TO.1 | TXDL_TO.0 | FSO_DIS  |

| CONTROL_1 | D15        | D14        | D13         | D12         | D11     | D10     | D9      | D8      |
|-----------|------------|------------|-------------|-------------|---------|---------|---------|---------|
|           | RW         | RW         | RW          | RW          | RW      | RW      | RW      | RW      |
|           | WU_CAN_DIS | WU_LIN_DIS | WU_TIM_EN.1 | WU_TIM_EN.0 | WU3_DIS | WU2_DIS | WU1_DIS | WU3_PUD |
| CONTROL_1 | D7         | D6         | D5          | D4          | D3      | D2      | D1      | D0      |
|           | RW         | RW         | RW          | RW          | RW      | RW      | RW      | RW      |
|           | WU2_PUD    | WU1_PUD    | WU3_T.1     | WU3_T.0     | WU2_T.1 | WU2_T.0 | WU1_T.1 | WU1_T.0 |

| CONTROL_2 | D15       | D14       | D13      | D12      | D11       | D10       | D9        | D8       |
|-----------|-----------|-----------|----------|----------|-----------|-----------|-----------|----------|
|           | RW        | RW        | RW       | RW       | RW        | RW        | RW        | RW       |
|           | reserved  | reserved  | reserved | reserved | reserved  | reserved  | reserved  | reserved |
| CONTROL_2 | D7        | D6        | D5       | D4       | D3        | D2        | D1        | D0       |
|           | RW        | RW        | RW       | RW       | RW        | RW        | RW        | RW       |
|           | T2_TPER.1 | T2_TPER.0 | T2_TON.1 | T2_TON.0 | T1_TPER.2 | T1_TPER.1 | T1_TPER.0 | T1_TON   |

| CONTROL_3 | D15            | D14      | D13      | D12      | D11      | D10      | D9       | D8         |
|-----------|----------------|----------|----------|----------|----------|----------|----------|------------|
|           | RW             | RW       | RW       | RW       | RW       | RW       | RW       | RW         |
|           | reserved       | reserved | reserved | reserved | reserved | reserved | reserved | reserved   |
| CONTROL_3 | D7             | D6       | D5       | D4       | D3       | D2       | D1       | D0         |
|           | RW             | RW       | RW       | RW       | RW       | RW       | RW       | RW         |
|           | VS_LOCKOUT_DIS | LS_OVUV  | LS2_ON.1 | LS2_ON.0 | LS1_ON.1 | LS1_ON.0 | INH_OFF  | OUT_HS_OCR |

SPI REGISTERS OVERVIEW

|           |           |           |           |           |             |             |             |           |
|-----------|-----------|-----------|-----------|-----------|-------------|-------------|-------------|-----------|
| CONTROL_4 | D15       | D14       | D13       | D12       | D11         | D10         | D9          | D8        |
|           | RW        | RW        | RW        | RW        | RW          | RW          | RW          | RW        |
|           | OUT1_LOWR | OUT4_ON.2 | OUT4_ON.1 | OUT4_ON.0 | OUT3_ON.2   | OUT3_ON.1   | OUT3_ON.0   | OUT2_ON.2 |
|           |           |           |           |           |             |             |             |           |
|           | D7        | D6        | D5        | D4        | D3          | D2          | D1          | D0        |
|           | RW        | RW        | RW        | RW        | RW          | RW          | RW          | RW        |
| OUT2_ON.1 | OUT2_ON.0 | OUT1_ON.2 | OUT1_ON.1 | OUT1_ON.0 | OUT_HS_ON.2 | OUT_HS_ON.1 | OUT_HS_ON.0 |           |

|         |          |          |          |          |          |          |          |          |
|---------|----------|----------|----------|----------|----------|----------|----------|----------|
| PWM_HS  | D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       |
|         | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
|         | reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved |
|         |          |          |          |          |          |          |          |          |
|         | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       |
|         | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
| FSEL_HS | PW_HS.6  | PW_HS.5  | PW_HS.4  | PW_HS.3  | PW_HS.2  | PW_HS.1  | PW_HS.0  |          |

|            |           |           |           |           |           |           |           |           |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| PWM_OUT1/2 | D15       | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT1 | PW_OUT1.6 | PW_OUT1.5 | PW_OUT1.4 | PW_OUT1.3 | PW_OUT1.2 | PW_OUT1.1 | PW_OUT1.0 |
|            |           |           |           |           |           |           |           |           |
|            | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
| FSEL_OUT2  | PW_OUT2.6 | PW_OUT2.5 | PW_OUT2.4 | PW_OUT2.3 | PW_OUT2.2 | PW_OUT2.1 | PW_OUT2.0 |           |

|            |           |           |           |           |           |           |           |           |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| PWM_OUT3/4 | D15       | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT3 | PW_OUT3.6 | PW_OUT3.5 | PW_OUT3.4 | PW_OUT3.3 | PW_OUT3.2 | PW_OUT3.1 | PW_OUT3.0 |
|            |           |           |           |           |           |           |           |           |
|            | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
| FSEL_OUT4  | PW_OUT4.6 | PW_OUT4.5 | PW_OUT4.4 | PW_OUT4.3 | PW_OUT4.2 | PW_OUT4.1 | PW_OUT4.0 |           |

|          |          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| PWM_LS   | D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       |
|          | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
|          | FSEL_LS1 | PW_LS1.6 | PW_LS1.5 | PW_LS1.4 | PW_LS1.3 | PW_LS1.2 | PW_LS1.1 | PW_LS1.0 |
|          |          |          |          |          |          |          |          |          |
|          | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       |
|          | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
| FSEL_LS2 | PW_LS2.6 | PW_LS2.5 | PW_LS2.4 | PW_LS2.3 | PW_LS2.2 | PW_LS2.1 | PW_LS2.0 |          |

|          |          |          |            |          |           |           |           |        |
|----------|----------|----------|------------|----------|-----------|-----------|-----------|--------|
| STATUS_0 | D15      | D14      | D13        | D12      | D11       | D10       | D9        | D8     |
|          | R        | R        | R          | R/RC     | R/RC      | R/RC      | R/RC      | R/RC   |
|          | OPMOD.1  | OPMOD.0  | COLD_START | WU_TIM   | WU_LIN    | WU_CAN    | WU_WU3    | WU_WU2 |
|          |          |          |            |          |           |           |           |        |
|          | D7       | D6       | D5         | D4       | D3        | D2        | D1        | D0     |
|          | R/RC     | R        | R          | R        | R         | R/RC      | R/RC      | R/RC   |
| WU_WU1   | WD_CNT.3 | WD_CNT.2 | WD_CNT.1   | WD_CNT.0 | VR1_RES.2 | VR1_RES.1 | VR1_RES.0 |        |

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## SPI REGISTERS OVERVIEW

|                 |            |            |            |            |            |            |           |           |
|-----------------|------------|------------|------------|------------|------------|------------|-----------|-----------|
| <b>STATUS_1</b> | <b>D15</b> | <b>D14</b> | <b>D13</b> | <b>D12</b> | <b>D11</b> | <b>D10</b> | <b>D9</b> | <b>D8</b> |
|                 | N/A        | R          | R          | R          | R/RC       | R          | R/RC      | R/RC      |
|                 | reserved   | WU3        | WU2        | WU1        | VCAN_FAIL  | VCAN_UV    | VR1_FAIL  | VR2_FAIL  |
|                 |            |            |            |            |            |            |           |           |
|                 | <b>D7</b>  | <b>D6</b>  | <b>D5</b>  | <b>D4</b>  | <b>D3</b>  | <b>D2</b>  | <b>D1</b> | <b>D0</b> |
|                 | R/RC       | R/RC       | R/RC       | R/RC       | R/RC       | R/RC       | R/RC      | R/RC      |
|                 | VR2_SHORT  | VS_OV      | VS_UV      | TSD2       | TSD1       | TWAR       | TO_TXDL   | TO_TXDC   |

|                 |            |            |             |             |            |            |           |           |
|-----------------|------------|------------|-------------|-------------|------------|------------|-----------|-----------|
| <b>STATUS_2</b> | <b>D15</b> | <b>D14</b> | <b>D13</b>  | <b>D12</b>  | <b>D11</b> | <b>D10</b> | <b>D9</b> | <b>D8</b> |
|                 | N/A        | N/A        | R           | R           | R/RC       | R/RC       | R/RC      | R/RC      |
|                 | reserved   | reserved   | WD_STATUS.1 | WD_STATUS.0 | LS2_OC     | LS1_OC     | OUT_HS_OC | OUT4_OC   |
|                 |            |            |             |             |            |            |           |           |
|                 | <b>D7</b>  | <b>D6</b>  | <b>D5</b>   | <b>D4</b>   | <b>D3</b>  | <b>D2</b>  | <b>D1</b> | <b>D0</b> |
|                 | R/RC       | R/RC       | R/RC        | R/RC        | R/RC       | R/RC       | R/RC      | R/RC      |
|                 | OUT3_OC    | OUT2_OC    | OUT1_OC     | OUT_HS_UL   | OUT4_UL    | OUT3_UL    | OUT2_UL   | OUT1_UL   |

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## SPI REGISTERS DETAILS

### CONTROL\_0

|           |           |           |          |           |           |           |          |          |
|-----------|-----------|-----------|----------|-----------|-----------|-----------|----------|----------|
| CONTROL_0 | D15       | D14       | D13      | D12       | D11       | D10       | D9       | D8       |
|           | RW        | RW        | RW       | RW        | RW        | RW        | RW       | RW       |
|           | MOD_STBY  | MOD_SLEEP | WD_TRIG  | WD_PER.1  | WD_PER.0  | ICMP_STBY | VR2_ON.1 | VR2_ON.0 |
|           |           |           |          |           |           |           |          |          |
|           | D7        | D6        | D5       | D4        | D3        | D2        | D1       | D0       |
|           | RW        | RW        | RW       | RW        | RW        | RW        | RW       | RW       |
| VR1_RES.1 | VR1_RES.0 | CAN_DIS   | CAN_LSTO | LIN_SLOPE | TXDL_TO.1 | TXDL_TO.0 | FSO_DIS  |          |

|              |          |           |         |                             |
|--------------|----------|-----------|---------|-----------------------------|
| Mode Control | MOD_STBY | MOD_SLEEP |         |                             |
|              | 0        | 0         | default | Normal Mode                 |
|              | 0        | 1         |         | Go to Sleep Mode            |
|              | 1        | 0         |         | Go to Standby Mode          |
|              | 1        | 1         |         | Go to Sleep Mode (dominant) |

|                      |         |  |                           |
|----------------------|---------|--|---------------------------|
| Watchdog Trigger Bit | WD_TRIG |  |                           |
|                      | 0       |  | Watchdog trigger set to 0 |
|                      | 1       |  | Watchdog trigger set to 1 |

|                       |          |          |         |   |
|-----------------------|----------|----------|---------|---|
| Watchdog Trigger Time | WD_PER.1 | WD_PER.0 |         | <b>Configuration of the Watchdog Trigger Time</b> |
|                       | 0        | 0        | default | Trigger time = 9.75 ms                            |
|                       | 0        | 1        |         | Trigger time = 39 ms                              |
|                       | 1        | 0        |         | Trigger time = 97.5 ms                            |
|                       | 1        | 1        |         | Trigger time = 195 ms                             |

|                        |           |         |  |
|------------------------|-----------|---------|--|
| Standby VR1 Comparator | ICMP_STBY |         | <b>Disables the VR1 Current Comparator</b> |
|                        | 0         | default | Comparator is Enabled                      |
|                        | 1         |         | Comparator is Disabled                     |

|             |          |          |         |  |
|-------------|----------|----------|---------|--|
| VR2 Control | VR2_ON.1 | VR2_ON.0 |         | <b>VR2 Behavior in Different Modes</b>                   |
|             | 0        | 0        | default | VR2 is off in all modes                                  |
|             | 0        | 1        |         | VR2 is on in normal mode; off in standby and sleep modes |
|             | 1        | 0        |         | VR2 is on in normal and standby mode; off in sleep mode  |
|             | 1        | 1        |         | VR2 is on in all modes                                   |

|                 |           |           |         |   |
|-----------------|-----------|-----------|---------|---|
| VR1 Reset Level | VR1_RES.1 | VR1_RES.0 |         | <b>Adjustment of the VR1 Reset Level</b>    |
|                 | 0         | 0         | default | Set the reset threshold to typ. 4.5 V (91%) |
|                 | 0         | 1         |         | Set the reset threshold to typ. 4.3 V (87%) |
|                 | 1         | 0         |         | Set the reset threshold to typ. 3.9 V (79%) |
|                 | 1         | 1         |         | Set the reset threshold to typ. 3.7 V (74%) |

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| CAN Transceiver Control | CAN_DIS | CAN_LSTO |         | CAN Transceiver In Normal Mode                              |
|-------------------------|---------|----------|---------|---|
|                         | 0       | 0        | default | CAN Transmitter and Receiver Enabled                        |
|                         | 0       | 1        |         | CAN Listen Only (Transmitter will not react to TxDC signal) |
|                         | 1       | X        |         | CAN Transceiver Disabled                                    |

| LIN Slope Control | LIN_SLOPE |         | Change of the LIN Slope                   |
|-------------------|-----------|---------|---|
|                   | 0         | default | High slew rate (as per LIN specification) |
|                   | 1         |         | Low slew rate                             |

| TxDL Time-out Timer | TxDL_TO.1 | TxDL_TO.0 |         | Dominant TxD Time-out Configuration of the LIN Interface |
|---------------------|-----------|-----------|---------|--|
|                     | 0         | 0         | default | Set the timer to typ. 55 ms                              |
|                     | 0         | 1         |         | Set the timer to typ. 13 ms                              |
|                     | 1         | X         |         | Time-out timer disabled                                  |

| FSO Function Disable | FSO_DIS |         | OUT3/FSO Function                               |
|----------------------|---------|---------|---|
|                      | 0       | default | OUT3 pin is driven by internal FSO signal       |
|                      | 1       |         | OUT3 pins is a general-purpose high-side driver |

### CONTROL\_1

|           |            |            |             |             |         |         |         |         |
|-----------|------------|------------|-------------|-------------|---------|---------|---------|---------|
| CONTROL_1 | D15        | D14        | D13         | D12         | D11     | D10     | D9      | D8      |
|           | RW         | RW         | RW          | RW          | RW      | RW      | RW      | RW      |
|           | WU_CAN_DIS | WU_LIN_DIS | WU_TIM_EN.1 | WU_TIM_EN.0 | WU3_DIS | WU2_DIS | WU1_DIS | WU3_PUD |
|           |            |            |             |             |         |         |         |         |
|           | D7         | D6         | D5          | D4          | D3      | D2      | D1      | D0      |
|           | RW         | RW         | RW          | RW          | RW      | RW      | RW      | RW      |
| WU2_PUD   | WU1_PUD    | WU3_T.1    | WU3_T.0     | WU2_T.1     | WU2_T.0 | WU1_T.1 | WU1_T.0 |         |

| CAN Wakeup Disable | WU_CAN_DIS |         | Disables CAN Wakeup in Standby or Sleep Mode |
|--------------------|------------|---------|--|
|                    | 0          | default | CAN Wakeup Enabled                           |
|                    | 1          |         | CAN Wakeup Disabled                          |

| LIN Wakeup Disable | WU_LIN_DIS |         | Disables LIN Wakeup in Standby or Sleep Mode |
|--------------------|------------|---------|--|
|                    | 0          | default | LIN Wakeup Enabled                           |
|                    | 1          |         | LIN Wakeup Disabled                          |

| Timer Wakeup Control | WU_TIM_EN.[1:0] |   |         | Enables Cyclic (timer controlled) Wakeup from Standby or Sleep Mode |
|----------------------|-----------------|---|---------|---|
|                      | 0               | 0 | default | Timers 1/2 are not used as wakeup sources                           |
|                      | 0               | 1 |         | Wakeup generated based on Timer 1                                   |
|                      | 1               | 0 |         | Wakeup generated based on Timer 2                                   |
|                      | 1               | 1 |         | Wakeup generated based on Timer 1                                   |

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| WUx Wakeup Disable | WU3_DIS | WU2_DIS | WU1_DIS |         | WUx Configuration                |
|--------------------|---------|---------|---------|---------|----------------------------------|
|                    | 0       | 0       | 0       | default | All wake-up inputs are enabled   |
|                    | X       | X       | 1       |         | Input WU1 is disabled as wake-up |
|                    | X       | 1       | X       |         | Input WU2 is disabled as wake-up |
|                    | 1       | X       | X       |         | Input WU3 is disabled as wake-up |

| WUx Sink/Source | WU3_PUD | WU2_PUD | WU1_PUD |         | WUx Sink/Source Configuration                            |
|-----------------|---------|---------|---------|---------|--|
|                 | 0       | 0       | 0       | default | Default: All WUx configured as current sink in all modes |
|                 | X       | X       | 1       |         | WU1 configured as current source in Normal mode          |
|                 | X       | 1       | X       |         | WU2 configured as current source in Normal mode          |
|                 | 1       | X       | X       |         | WU3 configured as current source in Normal mode          |

| WUx Filter Time | WUx_T.1 | WUx_T.0 |         | Defines the Filter configuration for Wake-ups WU1-3  |
|-----------------|---------|---------|---------|--|
|                 | 0       | 0       | default | Default: Filter with 64 $\mu$ s filter time (static sense)                                 |
|                 | 0       | 1       |         | Enables Filter after 80 $\mu$ s with a filter time of 16 $\mu$ s (cyclic sensing); Timer2  |
|                 | 1       | 0       |         | Enables Filter after 800 $\mu$ s with a filter time of 16 $\mu$ s (cyclic sensing); Timer2 |
|                 | 1       | 1       |         | Enables Filter after 800 $\mu$ s with a filter time of 16 $\mu$ s (cyclic sensing); Timer1 |

### CONTROL\_2

| CONTROL_2 | D15       | D14       | D13      | D12      | D11       | D10       | D9        | D8       |
|-----------|-----------|-----------|----------|----------|-----------|-----------|-----------|----------|
|           | RW        | RW        | RW       | RW       | RW        | RW        | RW        | RW       |
|           | reserved  | reserved  | reserved | reserved | reserved  | reserved  | reserved  | reserved |
|           |           |           |          |          |           |           |           |          |
|           | D7        | D6        | D5       | D4       | D3        | D2        | D1        | D0       |
|           | RW        | RW        | RW       | RW       | RW        | RW        | RW        | RW       |
|           | T2_TPER.1 | T2_TPER.0 | T2_TON.1 | T2_TON.0 | T1_TPER.2 | T1_TPER.1 | T1_TPER.0 | T1_TON   |

| Timer2 Period | T2_TPER.1 | T2_TPER.0 |         | Defines the Period of the Cyclic Sense Timer2 |
|---------------|-----------|-----------|---------|---|
|               | 0         | 0         | default | Period: 200 ms                                |
|               | 0         | 1         |         | Period: 50 ms                                 |
|               | 1         | 0         |         | Period: 20 ms                                 |
|               | 1         | 1         |         | Period: 10 ms                                 |

| Timer2 On-time | T2_TON.1 | T2_TON.0 |         | Defines the On Time for the Cyclic Sense Timer2                       |
|----------------|----------|----------|---------|---|
|                | 0        | 0        | default | ON time 100 $\mu$ s   |
|                | 0        | 1        |         | ON time 200 $\mu$ s   |
|                | 1        | 0        |         | ON time 1 ms  |
|                | 1        | 1        |         | reserved – if used, will be equal to the default value of 100 $\mu$ s |



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| Timer1 Period | T1_TPER.2 | T1_TPER.1 | T1_TPER.0 |         | Defines the Period of the Cyclic Sense Timer1 |
|---------------|-----------|-----------|-----------|---------|---|
|               | 0         | 0         | 0         | default | Period: 0.5 s                                 |
|               | 0         | 0         | 1         |         | Period: 1.0 s                                 |
|               | 0         | 1         | 0         |         | Period: 1.5 s                                 |
|               | 0         | 1         | 1         |         | Period: 2.0 s                                 |
|               | 1         | 0         | 0         |         | Period: 2.5 s                                 |
|               | 1         | 0         | 1         |         | Period: 3.0 s                                 |
|               | 1         | 1         | 0         |         | Period: 3.5 s                                 |
|               | 1         | 1         | 1         |         | Period: 4.0 s                                 |

| Timer1 On-time | T1_TON |         | Defines the On Time for the Cyclic Sense Timer1 |
|----------------|--------|---------|---|
|                | 0      | default | ON time 10 ms                                   |
|                | 1      |         | ON time 20 ms                                   |

### CONTROL\_3

|                |          |          |          |          |          |          |            |          |
|----------------|----------|----------|----------|----------|----------|----------|------------|----------|
| CONTROL_3      | D15      | D14      | D13      | D12      | D11      | D10      | D9         | D8       |
|                | RW       | RW       | RW       | RW       | RW       | RW       | RW         | RW       |
|                | reserved | reserved | reserved | reserved | reserved | reserved | reserved   | reserved |
|                |          |          |          |          |          |          |            |          |
|                | D7       | D6       | D5       | D4       | D3       | D2       | D1         | D0       |
|                | RW       | RW       | RW       | RW       | RW       | RW       | RW         | RW       |
| VS_LOCKOUT_DIS | LS_OVUV  | LS2_ON.1 | LS2_ON.0 | LS1_ON.1 | LS1_ON.0 | INH_OFF  | OUT_HS_OCR |          |

| VS UV/OV Lockout | VS_LOCKOUT_DIS |         | Disables the Automatic VS Lockout                                  |
|------------------|----------------|---------|--|
|                  | 0              | default | Outputs will be reactivated only when the VS UV/OV flag is cleared |
|                  | 1              |         | Outputs will be reactivated when VS UV/OV condition disappears     |

| LSx Active in VS UV/OV | LS_OVUV |         | Enables LSx in Case of VS OV/UV                                       |
|------------------------|---------|---------|---|
|                        | 0       | default | Disabled – LSx will be disabled in case of VS UV/OV                   |
|                        | 1       |         | Enabled – LSx will remain in their previous state in case of VS UV/OV |

| LSx Driver Control | LSx_ON.1 | LSx_ON.0 |         | Defines the Configuration of the Low-Side LS1/2                     |
|--------------------|----------|----------|---------|---|
|                    | 0        | 0        | default | Driver is off in all modes  |
|                    | 0        | 1        |         | Driver is on in normal mode (off in standby/sleep mode)             |
|                    | 1        | 0        |         | Driver is controlled by its PWM setting in normal mode              |
|                    | 1        | 1        |         | reserved – if used, LSx will be off in all modes (equal to default) |

| Inhibit Output | INH_OFF |         | LIN Pull-up for Master or Control Output for External Voltage Regulator |
|----------------|---------|---------|---|
|                | 0       | default | INH output active in normal mode  |
|                | 1       |         | INH output off (master resistor disabled)                               |

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|  |                   |         |  |
|--|-------------------|---------|--|
| <b>Overcurrent Recovery<br/>OUT_HS</b> | <b>OUT_HS_OCR</b> |         | <b>Enables Overcurrent Recovery Mode at OUT_HS</b> |
|  | 0                 | default | Overcurrent recovery disabled                      |
|  | 1                 |         | Overcurrent recovery enabled                       |

### CONTROL\_4

|                  |            |            |            |            |            |             |             |             |
|------------------|------------|------------|------------|------------|------------|-------------|-------------|-------------|
| <b>CONTROL_4</b> | <b>D15</b> | <b>D14</b> | <b>D13</b> | <b>D12</b> | <b>D11</b> | <b>D10</b>  | <b>D9</b>   | <b>D8</b>   |
|                  | RW         | RW         | RW         | RW         | RW         | RW          | RW          | RW          |
|                  | OUT1_LOWR  | OUT4_ON.2  | OUT4_ON.1  | OUT4_ON.0  | OUT3_ON.2  | OUT3_ON.1   | OUT3_ON.0   | OUT2_ON.2   |
|                  |            |            |            |            |            |             |             |             |
|                  | <b>D7</b>  | <b>D6</b>  | <b>D5</b>  | <b>D4</b>  | <b>D3</b>  | <b>D2</b>   | <b>D1</b>   | <b>D0</b>   |
|                  | RW         | RW         | RW         | RW         | RW         | RW          | RW          | RW          |
|                  | OUT2_ON.1  | OUT2_ON.0  | OUT1_ON.2  | OUT1_ON.1  | OUT1_ON.0  | OUT_HS_ON.2 | OUT_HS_ON.1 | OUT_HS_ON.0 |

|                             |                  |         |   |
|-----------------------------|------------------|---------|---|
| <b>OUT1 Switch Strength</b> | <b>OUT1_LOWR</b> |         | <b>Enables Stronger Switch on OUT1 Output</b>   |
|                             | 0                | default | "Normal ohmic" configuration: typical 7 Ohm Ron; parameters equal to OUT2-4                         |
|                             | 1                |         | "Low ohmic" configuration: typical 2 Ohm Ron; higher underload threshold; higher current limitation |

|                          |                        |   |   |   |   |
|--------------------------|------------------------|---|---|---|---|
| <b>HS Driver Control</b> | <b>OUT_HS_ON.[2:0]</b> |   |   |   | <b>Defines the Configuration of the High-side OUT_HS</b>  |
|                          | <b>OUTx_ON.[2:0]</b>   |   |   |   | <b>Defines the Configuration of the High-side OUT1..4</b>                                       |
|                          | 0                      | 0 | 0 | default   | Driver is off in all modes  |
|                          | 0                      | 0 | 1 |   | Driver is on in normal, standby and sleep mode  |
|                          | 0                      | 1 | 0 |   | Driver is cyclic on with the timing of Timer1 in normal, standby and sleep mode                 |
|                          | 0                      | 1 | 1 |   | Driver is cyclic on with the timing of Timer2 in normal, standby and sleep mode                 |
|                          | 1                      | 0 | 0 |   | Driver is controlled by the corresponding PWM unit in normal, cyclic-sense standby / sleep mode |
|                          | 1                      | 0 | 1 |   | reserved – if used, the driver is off in all modes (equal to default)                           |
|                          | 1                      | 1 | 0 |   | reserved – if used, the driver is off in all modes (equal to default)                           |
| 1                        | 1                      | 1 |   | reserved – if used, the driver is off in all modes (equal to default) |   |

### PWM\_HS

|               |            |            |            |            |            |            |           |           |
|---------------|------------|------------|------------|------------|------------|------------|-----------|-----------|
| <b>PWM_HS</b> | <b>D15</b> | <b>D14</b> | <b>D13</b> | <b>D12</b> | <b>D11</b> | <b>D10</b> | <b>D9</b> | <b>D8</b> |
|               | RW         | RW         | RW         | RW         | RW         | RW         | RW        | RW        |
|               | reserved   | reserved   | reserved   | reserved   | reserved   | reserved   | reserved  | reserved  |
|               |            |            |            |            |            |            |           |           |
|               | <b>D7</b>  | <b>D6</b>  | <b>D5</b>  | <b>D4</b>  | <b>D3</b>  | <b>D2</b>  | <b>D1</b> | <b>D0</b> |
|               | RW         | RW         | RW         | RW         | RW         | RW         | RW        | RW        |
|               | FSEL_HS    | PW_HS.6    | PW_HS.5    | PW_HS.4    | PW_HS.3    | PW_HS.2    | PW_HS.1   | PW_HS.0   |

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## PWM\_OUT1/2

|            |           |           |           |           |           |           |           |           |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| PWM_OUT1/2 | D15       | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT1 | PW_OUT1.6 | PW_OUT1.5 | PW_OUT1.4 | PW_OUT1.3 | PW_OUT1.2 | PW_OUT1.1 | PW_OUT1.0 |
|            |           |           |           |           |           |           |           |           |
|            | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT2 | PW_OUT2.6 | PW_OUT2.5 | PW_OUT2.4 | PW_OUT2.3 | PW_OUT2.2 | PW_OUT2.1 | PW_OUT2.0 |

## PWM\_OUT3/4

|            |           |           |           |           |           |           |           |           |
|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| PWM_OUT3/4 | D15       | D14       | D13       | D12       | D11       | D10       | D9        | D8        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT3 | PW_OUT3.6 | PW_OUT3.5 | PW_OUT3.4 | PW_OUT3.3 | PW_OUT3.2 | PW_OUT3.1 | PW_OUT3.0 |
|            |           |           |           |           |           |           |           |           |
|            | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        |
|            | RW        | RW        | RW        | RW        | RW        | RW        | RW        | RW        |
|            | FSEL_OUT4 | PW_OUT4.6 | PW_OUT4.5 | PW_OUT4.4 | PW_OUT4.3 | PW_OUT4.2 | PW_OUT4.1 | PW_OUT4.0 |

## PWM\_LS

|        |          |          |          |          |          |          |          |          |
|--------|----------|----------|----------|----------|----------|----------|----------|----------|
| PWM_LS | D15      | D14      | D13      | D12      | D11      | D10      | D9       | D8       |
|        | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
|        | FSEL_LS1 | PW_LS1.6 | PW_LS1.5 | PW_LS1.4 | PW_LS1.3 | PW_LS1.2 | PW_LS1.1 | PW_LS1.0 |
|        |          |          |          |          |          |          |          |          |
|        | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       |
|        | RW       | RW       | RW       | RW       | RW       | RW       | RW       | RW       |
|        | FSEL_LS2 | PW_LS2.6 | PW_LS2.5 | PW_LS2.4 | PW_LS2.3 | PW_LS2.2 | PW_LS2.1 | PW_LS2.0 |

|               |                                  |         |  |
|---------------|----------------------------------|---------|--|
| PWM Frequency | FSEL_HS<br>FSEL_OUTx<br>FSEL_LSx |         | PWM Frequency Selector   |
|               | 0                                | default | Base frequency of PWM on the corresponding output $f(\text{PWM}) = 150 \text{ Hz}$ |
|               | 1                                |         | Base frequency of PWM on the corresponding output $f(\text{PWM}) = 200 \text{ Hz}$ |

|                   |   |         |  |
|-------------------|---|---------|--|
| Output Duty Cycle | PW_HS[6:0]<br>PW_OUTx[6:0]<br>PW_LSx[6:0] |         | Duty Cycle Selector  |
|                   | 0   | default | Corresponding output is active with duty cycle 1 / 128                           |
|                   | 1 .. \$7F                                 |         | Corresponding output is active with duty cycle $(\text{PW\_xxx}[6:0] + 1) / 128$ |

## STATUS\_0

|          |         |          |            |          |          |           |           |           |
|----------|---------|----------|------------|----------|----------|-----------|-----------|-----------|
| STATUS_0 | D15     | D14      | D13        | D12      | D11      | D10       | D9        | D8        |
|          | R       | R        | R          | R/RC     | R/RC     | R/RC      | R/RC      | R/RC      |
|          | OPMOD.1 | OPMOD.0  | COLD_START | WU_TIM   | WU_LIN   | WU_CAN    | WU_WU3    | WU_WU2    |
|          |         |          |            |          |          |           |           |           |
|          | D7      | D6       | D5         | D4       | D3       | D2        | D1        | D0        |
|          | R/RC    | R        | R          | R        | R        | R/RC      | R/RC      | R/RC      |
|          | WU_WU1  | WD_CNT.3 | WD_CNT.2   | WD_CNT.1 | WD_CNT.0 | VR1_RES.2 | VR1_RES.1 | VR1_RES.0 |

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| Operating Mode | OPMOD.1 | OPMOD.0 | Operating Mode              |
|----------------|---------|---------|-----------------------------|
|                | 0       | 0       | Standby                     |
|                | 0       | 1       | Normal                      |
|                | 1       | 0       | Flash                       |
|                | 1       | 1       | reserved – will not be used |

| Cold Start | COLD_START | Power on Reset Status  |
|------------|------------|--|
|            | 0          | Cold start (=VS connection) not occurred   |
|            | 1          | Cold start (=VS connection) occurred – cleared after first successful access of the register |

| Wake-up Source Recognition | WU_TIM | WU_LIN | WU_CAN | Remote Wake-up Source                 |
|----------------------------|--------|--------|--------|---------------------------------------|
|                            | 0      | 0      | 0      | no timer, CAN nor LIN wakeup occurred |
|                            | X      | X      | 1      | CAN wake-up occurred                  |
|                            | X      | 1      | X      | LIN wake-up occurred                  |
|                            | 1      | X      | X      | Timer wakeup occurred                 |

| Wake-up Source Recognition | WU_WUx | Local Wake-up Source (Wux Pins) |
|----------------------------|--------|---------------------------------|
|                            | 0      | No WUx pin wake-up occurred     |
|                            | 1      | WUx pin wake-up occurred        |

| Watchdog Failure Counter | WD_CNT.[3:0] | Number of Watchdog Failures                      |
|--------------------------|--------------|--|
|                          | 0            | default<br>No watchdog failure encountered       |
|                          | \$1 .. \$F   | Non-zero number of watchdog failures encountered |

| VR1 Restart Counter | VR1_RES.[2:0] | Number of Unsuccessful Restarts of VR1 After Thermal Shutdown |
|---------------------|---------------|---|
|                     | 0             | default<br>No unsuccessful VR1 restart encountered            |
|                     | \$1 .. \$7    | Non-zero number of unsuccessful VR1 restarts encountered      |

### STATUS\_1

| STATUS_1 | D15       | D14   | D13   | D12  | D11       | D10     | D9       | D8       |
|----------|-----------|-------|-------|------|-----------|---------|----------|----------|
|          | N/A       | R     | R     | R    | R/RC      | R       | R/RC     | R/RC     |
|          | reserved  | WU3   | WU2   | WU1  | VCAN_FAIL | VCAN_UV | VR1_FAIL | VR2_FAIL |
|          | D7        | D6    | D5    | D4   | D3        | D2      | D1       | D0       |
|          | R/RC      | R/RC  | R/RC  | R/RC | R/RC      | R/RC    | R/RC     | R/RC     |
|          | VR2_SHORT | VS_OV | VS_UV | TSD2 | TSD1      | TWAR    | TO_TXDL  | TO_TXDC  |

| Status of WUx Inputs | WUx | Status of Wux Input in Normal Mode |
|----------------------|-----|------------------------------------|
|                      | 0   | WUx is Low                         |
|                      | 1   | WUx is High                        |

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|                     |                  |         |  |
|---------------------|------------------|---------|--|
| <b>VCAN Failure</b> | <b>VCAN_FAIL</b> |         | <b>VCC_CAN Supply Input Failure</b>  |
|                     | 0                | default | no VCC_CAN failure occurred  |
|                     | 1                |         | VCC_CAN fails for at least 2 $\mu$ s (VCC_CAN < Vfail_VCAN for > 2 $\mu$ s), latched bit |

|                          |                |         |  |
|--------------------------|----------------|---------|--|
| <b>VCAN Undervoltage</b> | <b>VCAN_UV</b> |         | <b>VCC_CAN Supply Input Undervoltage</b> |
|                          | 0              | default | no VCC_CAN failure occurred              |
|                          | 1              |         | VCC_CAN < Vfail_VCAN                     |

|                    |                 |         |   |
|--------------------|-----------------|---------|---|
| <b>VR1 Failure</b> | <b>VR1_FAIL</b> |         | <b>Voltage Regulator VR1 Failure</b>  |
|                    | 0               | default | no VR1 failure occurred   |
|                    | 1               |         | VR1 fails for at least 5 $\mu$ s (VR1 < 2 V for > 5 $\mu$ s) OR (VR1 < 2 V at 4 ms after turn-on) |

|                    |                 |         |   |
|--------------------|-----------------|---------|---|
| <b>VR2 Failure</b> | <b>VR2_FAIL</b> |         | <b>Voltage Regulator VR2 Failure</b>  |
|                    | 0               | default | No VR2 failure occurred   |
|                    | 1               |         | VR2 fails for at least 2 $\mu$ s (VR2 < 2 V for > 2 $\mu$ s) OR (VR2 < 2 V at 4 ms after turn-on) |

|                          |                  |         |   |
|--------------------------|------------------|---------|---|
| <b>VR2 Short Circuit</b> | <b>VR2_SHORT</b> |         | <b>Indicates a Short Circuit at VR2</b>                     |
|                          | 0                | default | No short circuit  |
|                          | 1                |         | VR2 short to GND at turn on; (VR2 < 2 V for more than 4 ms) |

|                       |              |         |                                   |
|-----------------------|--------------|---------|-----------------------------------|
| <b>VS Overvoltage</b> | <b>VS_OV</b> |         | <b>Overvoltage on VS Pin</b>      |
|                       | 0            | default | VS is below the overvoltage limit |
|                       | 1            |         | VS exceeded the overvoltage limit |

|                        |              |         |                                      |
|------------------------|--------------|---------|--------------------------------------|
| <b>VS Undervoltage</b> | <b>VS_UV</b> |         | <b>Undervoltage on VS Pin</b>        |
|                        | 0            | default | VS is above the undervoltage limit   |
|                        | 1            |         | VS fell below the undervoltage limit |

|                           |             |             |             |         |                                 |
|---------------------------|-------------|-------------|-------------|---------|---------------------------------|
| <b>Thermal Protection</b> | <b>TSD2</b> | <b>TSD1</b> | <b>TWAR</b> |         | <b>Thermal Warning/Shutdown</b> |
|                           | 0           | 0           | 0           | default | No thermal limit exceeded       |
|                           | X           | X           | 1           |         | Thermal warning encountered     |
|                           | X           | 1           | X           |         | Thermal shutdown 1 encountered  |
|                           | 1           | X           | X           |         | Thermal shutdown 2 encountered  |

|                                      |                |                |         |                                     |
|--------------------------------------|----------------|----------------|---------|-------------------------------------|
| <b>Permanent Dominant Protection</b> | <b>TO_TxDL</b> | <b>TO_TxDC</b> |         |                                     |
|                                      | 0              | 0              | default | No transmitter timeout encountered  |
|                                      | 1              | X              |         | LIN transmitter timeout encountered |
|                                      | X              | 1              |         | CAN transmitter timeout encountered |

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## STATUS\_2

|          |          |          |             |             |         |         |           |         |
|----------|----------|----------|-------------|-------------|---------|---------|-----------|---------|
| STATUS_2 | D15      | D14      | D13         | D12         | D11     | D10     | D9        | D8      |
|          | N/A      | N/A      | R           | R           | R/RC    | R/RC    | R/RC      | R/RC    |
|          | reserved | reserved | WD_STATUS.1 | WD_STATUS.0 | LS2_OC  | LS1_OC  | OUT_HS_OC | OUT4_OC |
|          |          |          |             |             |         |         |           |         |
|          | D7       | D6       | D5          | D4          | D3      | D2      | D1        | D0      |
|          | R/RC     | R/RC     | R/RC        | R/RC        | R/RC    | R/RC    | R/RC      | R/RC    |
|          | OUT3_OC  | OUT2_OC  | OUT1_OC     | OUT_HS_UL   | OUT4_UL | OUT3_UL | OUT2_UL   | OUT1_UL |

|   |                 |   |  |
|---|-----------------|---|--|
| Watchdog Counter Status                                     | WD_STATUS.[1:0] |   | Watchdog Counter Status  |
|   | 0               | 0 | Watchdog counter below 33% of acceptable interval*               |
|   | 0               | 1 | Watchdog counter above 33% and below 66% of acceptable interval* |
|   | 1               | 0 | Reserved – will not be used                                      |
|   | 1               | 1 | Watchdog counter above 66% of acceptable interval*               |
| * acceptable interval means timeout or open window interval |                 |   |  |

|                    |                                 |         |  |
|--------------------|---------------------------------|---------|--|
| Driver Overcurrent | LSx_OC<br>OUT_HS_OC<br>OUT_x_OC |         | Overcurrent Status of the Corresponding Output |
|                    | 0                               | default | No overcurrent encountered                     |
|                    | 1                               |         | Overcurrent encountered                        |

|                  |                       |         |  |
|------------------|-----------------------|---------|--|
| Driver Underload | OUT_HS_UL<br>OUT_x_UL |         | Underload Status of the Corresponding Output |
|                  | 0                     | default | No underload encountered                     |
|                  | 1                     |         | Underload encountered                        |

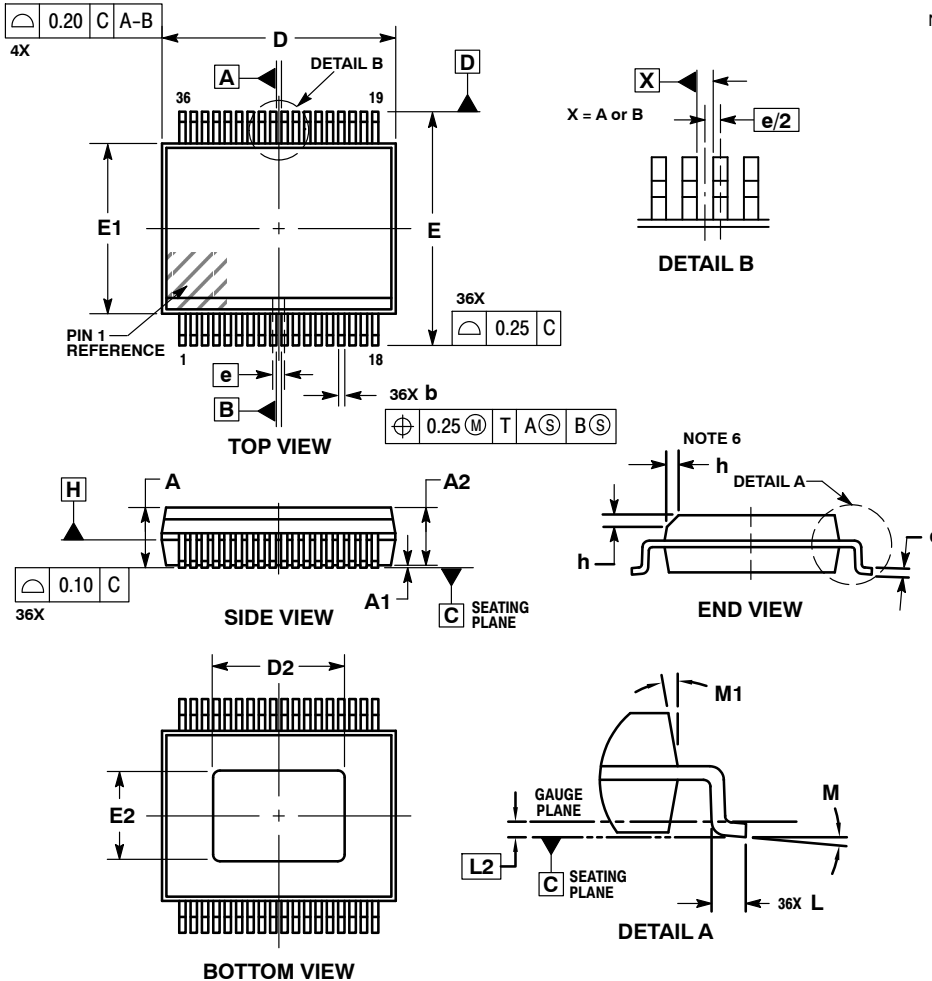
## DEVICE ORDERING INFORMATION

| Part Number   | Package Type           | Shipping <sup>†</sup>              |
|---------------|------------------------|------------------------------------|
| NCV7462DQ0R2G | SSOP36-EP<br>(Pb-Free) | 1500 / Tape & Reel<br>(24 mm Tape) |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SSOP36 EP  
CASE 940AB  
ISSUE A

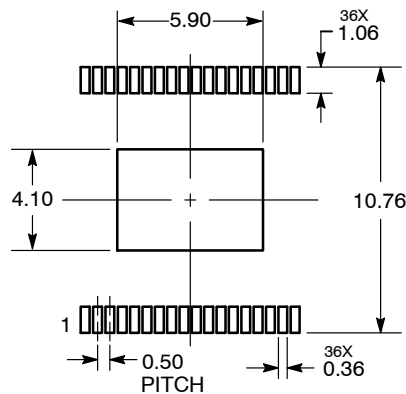


NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOCATED WITHIN THE INDICATED AREA.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | ---         | 2.65 |
| A1  | ---         | 0.10 |
| A2  | 2.15        | 2.60 |
| b   | 0.18        | 0.30 |
| c   | 0.23        | 0.32 |
| D   | 10.30 BSC   |      |
| D2  | 5.70        | 5.90 |
| E   | 10.30 BSC   |      |
| E1  | 7.50 BSC    |      |
| E2  | 3.90        | 4.10 |
| e   | 0.50 BSC    |      |
| h   | 0.25        | 0.75 |
| L   | 0.50        | 0.90 |
| L2  | 0.25 BSC    |      |
| M   | 0°          | 8°   |
| M1  | 5°          | 15°  |

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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