NCV81598

Product Preview

High Precision 4-Switch Buck Boost Controller

The NCV81598 is a 4 switch high precision synchronous buck boost controller that is optimized for converting battery voltage or adaptor voltage into power supply rails. NCV81598 is designed for applications requiring an output voltage that is either higher or lower than the input voltage. The Buck Boost Controller operates with a supply input range of 3.8 V to 32 V.

Features

- Wide Input Voltage Range: from 3.8 V to 32 V
- Operate Down to 3.5 V (Falling) for Cold Crank Conditions
- Adjustable Output Voltage from 0.5 V to 20 V
- 450 kHz Operating Frequency
- Real Time Power Good Indication
- Feedback Pin with Internally Programmed Reference
- 2 Independent Current Sensing Inputs
- Over Temperature Protection
- Adaptive Non−Overlap Gate Drivers
- Filter Capacitor Switch Control
- Over−Voltage and Over−Current Protection
- 5 x 5 mm QFN32 Package with Wettable Flanks
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Grade 1 Qualified and PPAP Capable

Typical Application

- Automotive Lighting Engine Control Unit

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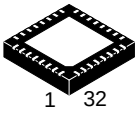
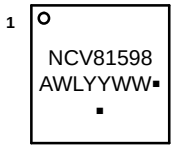


QFN32 5x5, 0.5P
CASE 485CE

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCV81598MWTXG	QFN32 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

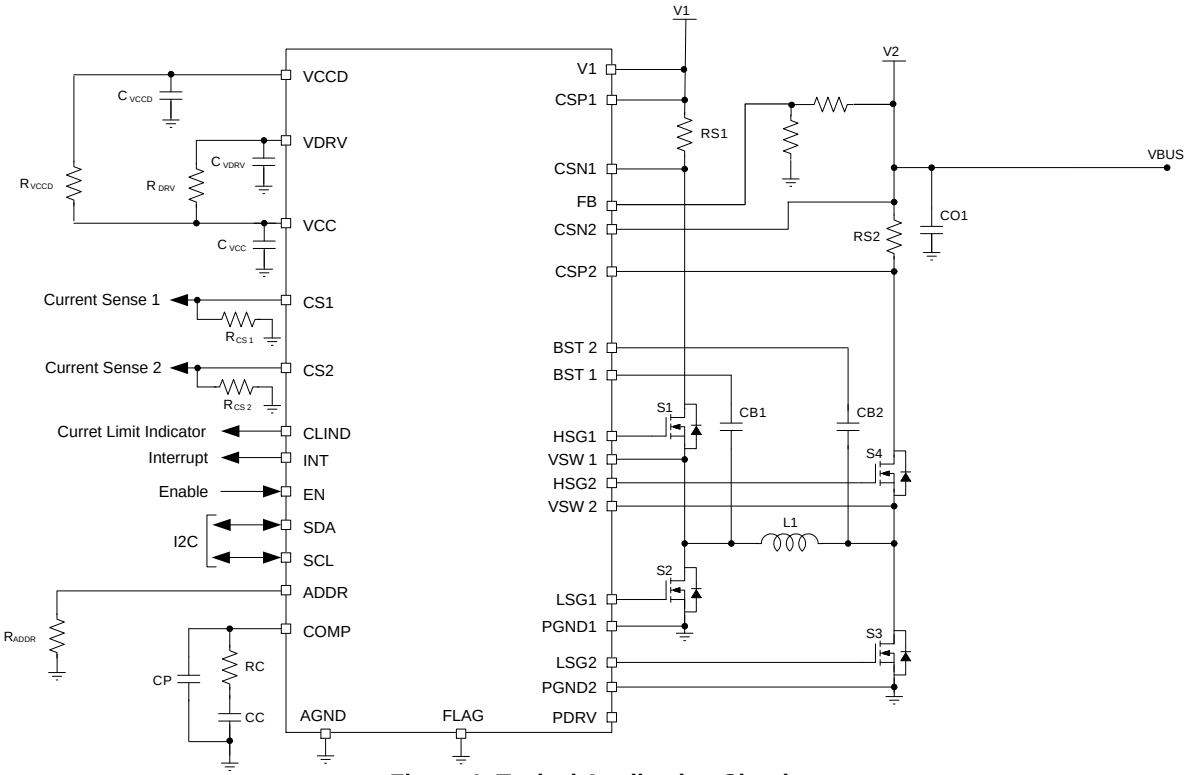


Figure 1. Typical Application Circuit

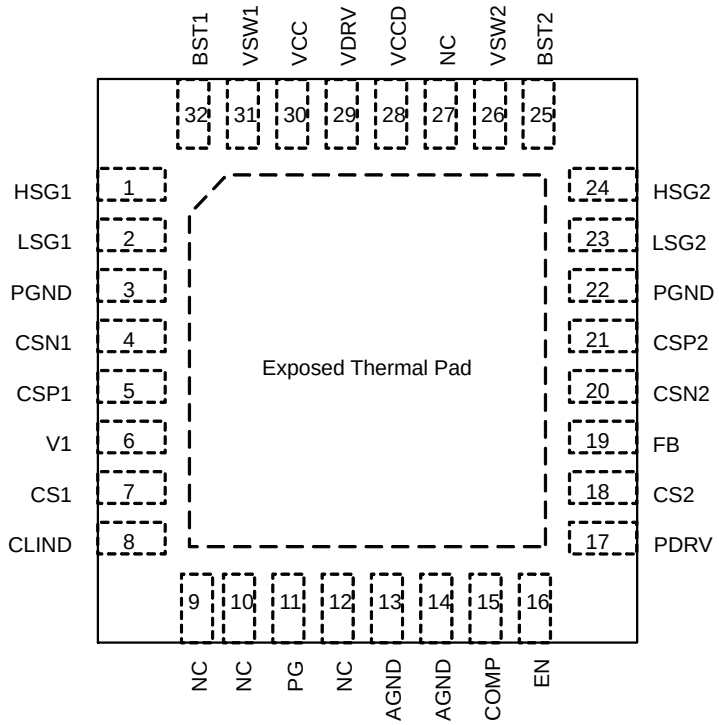


Figure 2. Pinout

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	HSG1	S1 gate drive. Drives the S1 N−channel MOSFET with a voltage equal to VDRV superimposed on the switch node voltage VSW1.
2	LSG1	Drives the gate of the S2 N−channel MOSFET between ground and VDRV.
3, 22	PGND	Power ground for the low side MOSFET drivers. Connect these pins closely to the source of the bottom N−channel MOSFETs.
4	CSN1	Negative terminal of the current sense amplifier.
5	CSP1	Positive terminal of the current sense amplifier.
6	V1	Input voltage of the converter
7	CS1	Current sense amplifier output. CS1 will source a current that is proportional to the voltage across RS1 to an external resistor. CS1 voltage can be monitored with a high impedance input. Ground this pin if not used.
8	CLIND	Open drain output to indicate that the CS1 or CS2 voltage has exceeded the set limit.
9	NC	Not connected.
10	NC	Not connected.
11	PG	Power good indicator, open drain output.
12	NC	Not connected.
13−14	AGND	The ground pin for the analog circuitry.
15	COMP	Output of the transconductance amplifier used for stability in closed loop operation.
16	EN	Precision enable starts the part and places it into default configuration when toggled.
17	PDRV	The open drain output used to control a PMOSFET.
18	CS2	Current sense amplifier output. CS2 will source a current that is proportional to the voltage across RS2 to an external resistor. CS2 voltage can be monitored with a high impedance input. Ground this pin if not used.
19	FB	Feedback voltage of the output, negative terminal of the gm amplifier.
20	CSN2	Negative terminal of the current sense amplifier.
21	CSP2	Positive terminal of the current sense amplifier.
23	LSG2	Drives the gate of the S3 N−channel MOSFET between ground and VDRV.
24	HSG2	S4 gate drive. Drives the S4 N−channel MOSFET with a voltage equal to VDRV superimposed on the switch node voltage VSW2.
25	BST2	Bootstrapped Driver Supply. The BST2 pin swings from a diode voltage below VDRV up to a diode voltage below VOUT + VDRV. Place a 0.1 μF capacitor from this pin to VSW2.
26	VSW2	Switch Node. VSW2 pin swings from a diode voltage drop below ground up to output voltage.
27	NC	Recommend to grounded.
28	VCCD	Internal digital power supply input.
29	VDRV	Internal voltage supply to the driver circuits. A 1 μF capacitor should be placed close to the part to decouple this line.
30	VCC	The VCC pin supplies power to the internal circuitry. The VCC is the output of a linear regulator which is powered from V1. Pin should be decoupled with a 1 μF capacitor for stable operation.
31	VSW1	Switch Node. VSW1 pin swings from a diode voltage drop below ground up to V1.
32	BST1	Driver Supply. The BST1 pin swings from a diode voltage below VDRV up to a diode voltage below V1 + VDRV. Place a 0.1 μF capacitor from this pin to VSW1.
33	THPAD	Center Thermal Pad. Connect to AGND externally.

Table 2. MAXIMUM RATINGS

Over operating free−air temperature range unless otherwise noted

Rating	Symbol	Min	Max	Unit
Digital Power	VCCD	−0.3	5.5	V
Driver Input Voltage	VDRV	−0.3	5.5	V
Internal Regulator Output	VCC	−0.3	5.5	V
Output of Current Sense Amplifiers	CS1, CS2	−0.3	3.0	V
Current Limit Indicator	CLIND	−0.3	VCC + 0.3	V
Power Good Indicator	PG	−0.3	VCC + 0.3	V
Enable Input	EN	−0.3	5.5	V
Compensation Output	COMP	−0.3	VCC + 0.3	V
V1 Power Stage Input Voltage	V1	−0.3	35 V, 40 V (20 ns)	V
Positive Current Sense	CSP1	−0.3	35 V, 40 V (20 ns)	V
Negative Current Sense	CSN1	−0.3	35 V, 40 V (20 ns)	V
Positive Current Sense	CSP2	−0.3	35 V, 40 V (20 ns)	V
Negative Current Sense	CSN2	−0.3	35 V, 40 V (20 ns)	V
Feedback Voltage	FB	−0.3	5.5	V
Driver 1 and Driver 2 Positive Rails	BST1, BST2	−0.3 V wrt/PGND −0.3 V wrt/VSW	37 V, 40 V (20 ns) wrt/PGND 5.5 V wrt/VSW	V
High Side Driver 1 and Driver 2	HSG1, HSG2	−0.3 V wrt/PGND −0.3 V wrt/VSW	37 V, 40 V (20 ns) wrt/GND 5.5 V wrt/VSW	V
Switching Nodes and Return Path of Driver 1 and Driver 2	VSW1, VSW2	−5.0 V	32 V, 40 V (20 ns)	V
Low Side Driver 1 and Driver 2	LSG1, LSG2	−0.3 V	5.5	V
PMOSFET Driver	PDRV	−0.3	32 V, 40 V (20 ns)	V
Voltage Differential	AGND to PGND	−0.3	0.3	V
CSP1−CSN1, CSP2−CSN2 Differential Voltage	CS1DIF, CS2DIF	−0.5	0.5	V
PDRV Maximum Current	PDRVI	0	10	mA
PDRV Maximum Pulse Current (100 ms on time, with > 1 s interval)	PDRVIPUL	0	200	mA
Maximum VCC Current	VCCI	0	80	mA
Operating Junction Temperature Range (Note 1)	TJ	−40	150	°C
Operating Ambient Temperature Range	TA	−40	100	°C
Storage Temperature Range	TSTG	−55	150	°C

Table 2. MAXIMUM RATINGS

Over operating free−air temperature range unless otherwise noted

Rating	Symbol	Min	Max	Unit
Thermal Characteristics (Note 2) QFN 32 5mm x 5mm Maximum Power Dissipation @ TA = 25°C Maximum Power Dissipation @ TA = 85°C Thermal Resistance Junction−to−Air with Solder Thermal Resistance Junction−to−Case Top with Solder Thermal Resistance Junction−to−Case Bottom with Solder	 PD PD RΘJA RΘJCT RΘJCB	 4.1 2.1 30 1.7 2.0		 W W °C/W °C/W °C/W
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3)	RF	260 Peak		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum package power dissipation limit must not be exceeded.
2. The value of ΘJA is measured with the device mounted on a 3in x 3in, 4 layer, 0.062 inch FR−4 board with 1.5 oz. copper on the top and bottom layers and 0.5 ounce copper on the inner layers, in a still air environment with T_A = 25°C.
3. 60−180 seconds minimum above 237°C.

Table 3. ELECTRICAL CHARACTERISTICS

(V1 = 12 V, V_{out} = 1.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Supply						
V1 Operating Input Voltage	V1		4.5		32	V
VDRV Operating Input Voltage	VDRV		4.5	5	5.5	V
VCC UVLO Rising Threshold	VCC_{START}			3.8		V
UVLO Hysteresis for VCC	$VCCV_{HYS}$	Falling Hysteresis		300		mV
VDRV UVLO Rising Threshold	$VDRV_{START}$			3.8		V
UVLO Hysteresis for VDRV	$VDRV_{HYS}$	Falling Hysteresis		300		mV
VCCD UVLO Rising Threshold	$VCCD_{START}$			3.8		V
UVLO Hysteresis for VCCD	$VCCD_{HYS}$			300		mV
VCC Output Voltage	VCC	With no external load	4.5	5		V
VCC Drop Out Voltage	VCCDROOP	30 mA load		150		mV
VCC Output Current Limit	$IOUT_{VCC}$	VCC Loaded to 4.3 V	80	97		mA
V1 Shutdown Supply Current	IVCC_SD	EN = 0 V, 4.3 V ≤ V1 ≤ 32 V		TBD	100	μA
VDRIVE Switching Current Buck	IV1_SW	EN = 5 V, Cgate = 2.2 nF, VSW = 0 V, FSW = 600 kHz		15		mA
VDRIVE Switching Current Boost	IV1_SW	EN = 5 V, Cgate = 2.2 nF, VSW = 0 V, FSW = 600 kHz		15		mA
Voltage Output						
Voltage Output Accuracy	FB		0.495	0.5	0.505	V
Voltage Accuracy Over Temperature	VOUTERT		−1.0		1.0	% mV
	VOUTER	T_A = 25°C	−0.45		0.45	%

4. Ensured by design. Not production tested.

Table 3. ELECTRICAL CHARACTERISTICS

(V1 = 12 V, V_{out} = 1.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Transconductance Amplifier						
Gain Bandwidth Product	GBW	(Note 4)		5.2		MHz
Transconductance	GM1	Default		500		μS
Max Output Source Current limit	GMSOC		60	80		μA
Max Output Sink Current limit	GMSIC		60	80		μA
Voltage Ramp	Vramp			1.4		V
Internal BST Diode						
Forward Voltage Drop	VFBOT	I_F = 10 mA, T_A = 25°C	0.35	0.46	0.55	V
Reverse Bias Leakage Current	DIL	BST−VSW = 5 V V_{SW} = 32 V, T_A = 25°C		0.05	1	μA
BST−VSW UVLO	$BST1_{\_UVLO}$	Rising, Note 4		3.5		V
BST−VSW Hysteresis	$BST_{\_HYS}$	Note 4		300		mV
Oscillator						
Oscillator Frequency	FSW			450		kHz
Oscillator Frequency Accuracy	FSWE		−12		12	%
Minimum On Time	MOT	Measured at 10% to 90% of VCC		50		ns
Minimum Off Time	MOFT	Measured at 90% to 10% of VCC		90		ns
PG Thresholds						
PG Low Voltage	PGLOW	PG(sink) = 2 mA			0.2	V
PG High Leakage Current	IPGSS	3.3 V		3	100	nA
PG Startup Delay	INTPG	Soft Start end to PG positive edge		2.1		ms
PG Propagation Delay	PGI	Delay for power good in		3.3		ms
	PGO	Delay for power good out		100		ns
Power Good Threshold	PGTH	Power Good in from high		105		%
	PGTH	Power Good in from low		95		%
	PGTHYS	PG falling hysteresis		2.5		%
FB Overvoltage Threshold	FB_OV			120		%
Overvoltage Propagation Delay	VFB_OVDL			1 Cycle		
External Current Sense (CS1,CS2)						
Positive Current Measurement High	CS10	CSP1−CSN1 or CSP2−CSN2 = 100 mV		500		μA
Transconductance Gain Factor	CSGT	Current Sense Transconductance Vsense = 1 mV to 100 mV		5		mS
Transconductance Deviation	CSGE		−20		20	%
Current Sense Common Mode Range	CSCMMR		3		32	V
−3dB Small Signal Bandwidth	CSBW	VSENSE (AC) = 10 mVPP, RGAIN = 10 kΩ (Note 4)		30		MHz
Input Sense Voltage Full Scale	ISVFS				100	mV
CS Output Voltage Range	CSOR	VSENSE = 100 mV Rset = 6k	0		3	V

4. Ensured by design. Not production tested.

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(V1 = 12 V, V_{out} = 1.0 V , T_A = +25°C for typical value; −40°C < T_A < 100°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
External Current Limit (CLIND)						
Current Limit Indicator Output Low	CLINDL	Input current = 500 μA		5.6	100	mV
Current Limit Indicator Output High	CLINDH	Input current = 500 μA	4.0	5.0		V
Internal Current Sense						
Internal Current Sense Gain for PWM	ICG	CSPx−CSNx = 100 mV	9.2	9.8	10.5	V/V
Positive Peak Current Limit Trip	PPCLT			70		mV
Negative Valley Current Limit Trip	NVCLT		31	40	45	mV
Switching MOSFET Drivers						
HSG1 HSG2 Pullup Resistance	HSG_PU	BST−VSW = 4.5 V		2.8		Ω
HSG1 HSG2 Pulldown Resistance	HSG_PD	BST−VSW = 4.5 V		1.2		Ω
LSG1 LSG2 Pullup Resistance	LSG_PU	LSG −PGND = 2.5 V		3.3		Ω
LSG1 LSG2 Pulldown Resistance	LSG_PD	LSG −PGND = 2.5 V		0.9		Ω
HSG Falling to LSG Rising Delay	HSLSD			15		ns
LSG Falling to HSG Rising Delay	LSHSD			15		ns
Enable						
EN High Threshold Voltage	ENLDOHT	LDO ON		798	820	mV
EN Low Threshold Voltage	ENLDOLT		640	665		mV
EN Switching High Threshold Voltage	ENHT	LDO ON, Switching		2.5		V
EN Switching Low Threshold Voltage	ENLT	LDO ON, Switching		2.2		V
EN Pull Up Current	IEN_UP	EN = 0 V		1.8		μA
Thermal Shutdown						
Thermal Shutdown Threshold	TSD	(Note 4)		151		°C
Thermal Shutdown Hysteresis	TSDHYS	(Note 4)		28		°C
PDRV						
PDRV Operating Range			0		32	V
PDRV Leakage Current	PDRV_IDS	FET OFF, VPDRV = 32 V		180		nA
PDRV Saturation Voltage	PDRV_VDS	ISNK = 10 mA		0.20		V

4. Ensured by design. Not production tested.

APPLICATION INFORMATION

Dual Edge Current Mode Control

When dual edge current mode control is used, two voltage ramps are generated that are 180 degrees out of phase. The inductor current signal is added to the ramps to incorporate current mode control. In Figure 3, the COMP signal from the compensation output interacts with two triangle ramps to generate gate signals to the switches from S1 to S4. Two ramp signals cross twice at midpoint within a cycle. When COMP is above the midpoint, the system will operate at boost mode with S1 always on and S2 always off, but S3 and S4 turning on alternatively in an active switching mode. When COMP is below the midpoint, the system will operation at buck mode, with S4 always on and S3 always off, but S1 and S2 turning on alternatively in an active switching mode. The controller can switch between buck and boost mode smoothly based on the COMP signal from peak current regulation.

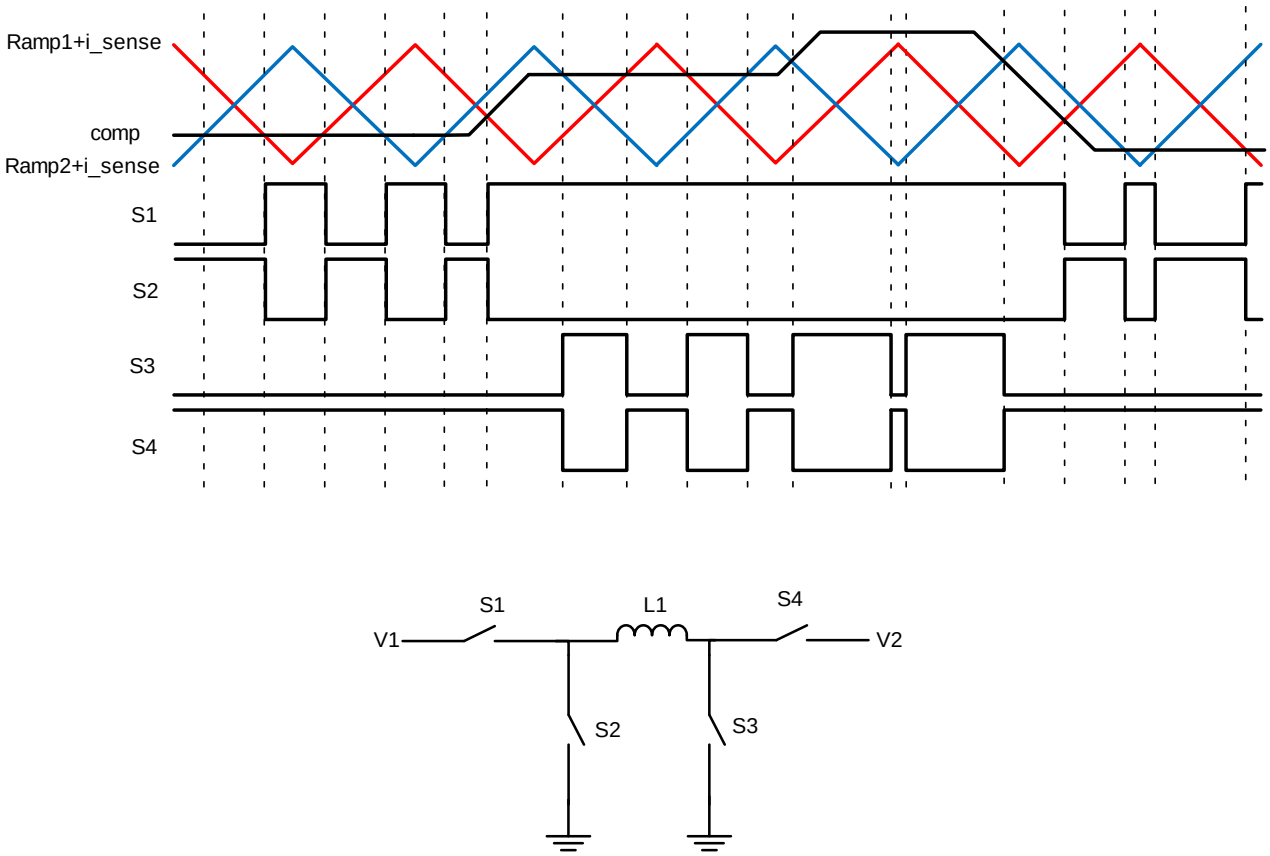


Figure 3. Transitions for Dual Edge 4 Switch Buck Boost

Feedback

The feedback of the converter output voltage is connected to the FB pin of the device through a resistor divider. Internally FB is connected to the inverting input of the internal transconductance error amplifier. The non−inverting input of the gm amplifier is connected to the internal reference. The internal reference voltage is by default 0.5 V. Therefore a 10:1 resistor divider from the converter output to the FB will set the output voltage to 5V.

Soft Start

During a 0 V soft start, standard converters can start in synchronous mode and have a monotonic rising of output voltage. If a prebias exists on the output and the converter starts in synchronous mode, the prebias voltage could be discharged. The NCV81598 controller ensures that if a prebias is detected, the soft start is completed in a non−synchronous mode to prevent the output from discharging. During softstart, the output rising slew rate will be set to 0.6 mV/μs (FB = 0.1*V2).

Current Sense Amplifiers

Internal precision differential amplifiers measure the potential between the terminal CSP1 and CSN1 or CSP2 and CSN2. Current flows from the input V1 to the output in a buck boost design. Current flowing from V1 through the switches to the inductor passes through R_{SENSE}. The external sense resistor, R_{SENSE}, has a significant effect on the function of current sensing and limiting systems and must be chosen with care. First, the power dissipation in the resistor should be considered. The system load current will cause both heat and voltage loss in R_{SENSE}. The power loss and voltage drop drive the designer to make the sense resistor as small as possible while still providing the input dynamic range required by the measurement. Note that input dynamic range is the difference between the maximum input signal and the minimum accurately measured signal, and is limited primarily by input DC offset of the internal amplifier. In addition, R_{SENSE} must be small enough that V_{SENSE} does not exceed the maximum input voltage 100 mV, even under peak load conditions.

The potential difference between CSPx and CSNx is level shifted from the high voltage domain to the low voltage VCC domain where the signal is split into two paths.

The first path, or external path, allows the end user to observe the analog or digital output of the high side current sense. The external path gain is set by the end user allowing the designer to control the observable voltage level.

The second path, or internal path, has internally set gain of 10 and allows cycle by cycle precise limiting of positive and negative peak input current limits.

Positive Current Limit Internal Path

The NCV81598 has a pulse by pulse current limiting function activated when a positive current limit triggers. CSP1/CSN1 will be the positive current limit sense channel.

When a positive current limit is triggered, the current pulse is truncated. In both buck mode and in boost mode the S1 switch is turned off to limit the energy during an over current event. The current limit is reset every switching cycle and waits for the next positive current limit trigger. In this way, current is limited on a pulse by pulse basis. Pulse by pulse current limiting is advantageous for limiting energy into a load in over current situations but are not up to the task of limiting energy into a low impedance short. To address the low impedance short, the NCV81598 does pulse by pulse current limiting for 2 ms known as Ilim timeout or until the output voltage falls below 300 mV, the controller will enter into fast stop. The NCV81598 remains in fast stop state with all switches driven off for 10 ms. Once the 10 ms has expired, the part is allowed to soft start to the previously programmed voltage and current level if the short circuit condition is cleared.

The internal positive current limit by default is 70 mV.

Negative Current Limit Internal Path

Negative current limit can be activated in a few instances, including light load synchronous operation, heavy load to light load transition, output overvoltage, and high output voltage to lower output voltage transitions. CSP2/CSN2 will be the negative current limit sense channel.

During light load synchronous operation, or heavy load to light load transitions the negative current limit can be triggered during normal operation. When the sensed current exceeds the negative current limit, the S4 switch is shut off preventing the discharge of the output voltage both in buck mode and in boost mode if the output is in the power good range. Both in boost mode and in buck mode when a negative current is sensed, the S4 switch is turned off for the remainder of either the S4 or S2 switching cycle and is turned on again at the appropriate time. In buck mode, S4 is turned off at the negative current limit transition and turned on again as soon as the S2 on switch cycle ends. In boost mode, the S4 switch is the rectifying switch and upon negative current limit the switch will shut off for the remainder of its switching cycle. The internal negative current limit by default is −40 mV.

External Path (CS1, CS2, CLIND)

The voltage drop across the sense resistors as a result of the load can be observed on the CS1 and CS2 pins. Both CS1, CS2 can be monitored with a high impedance input. An external series resistor can be added for additional filtering. The voltage drop is converted into a current by a transconductance amplifier with a typical GM of 5 mS. The final gain of the output is determined by the end users selection of the R_{CS} resistors. The output voltage of the CS pin can be calculated from Equation 1. The user must be careful to keep the dynamic range below 3.0 V when considering the maximum short circuit current.

$$V_{CS} = (I_{LOAD\_MAX} * R_{SENSE} * Trans) * R_{CS} \rightarrow$$

$$\rightarrow 2.967\ V = (8.5\ A * 5\ m\Omega * 5\ mS) * 13.96\ k\Omega$$

$$R_{CS} = \frac{V_{CS}}{I_{LOAD} * R_{SENSE} * Trans} \rightarrow$$

$$\rightarrow 13.96\ k\Omega = \frac{2.967\ V}{8.5\ A * 5\ m\Omega * 5\ mS} \quad \text{(eq. 1)}$$

The speed and accuracy of the dual amplifier stage allows the reconstruction of the input and output current signal, creating the ability to limit the peak current. If the user would like to limit the mean DC current of the switch, a capacitor can be placed in parallel with the R_{CS} resistors. CS1, CS2 can be monitored with a high impedance input. An external series resistor can be added for additional filtering.

CS1, CS2 voltages are connected internally to 2 high speed low offset comparators. The comparators output can be used to suspend operation until reset or restart of the part. When the external CLIND flag is triggered, it indicates that one of the internal comparators has exceeded the preset limit (CSx_LIM). The default comparator setting is 250 mV which is a limit of 500 mA with a current sense resistor of 5 mΩ and an R_{CS} resistor of 20 kΩ.

Overvoltage Protection (OVP)

When the divided output voltage is 120% (typical) above the internal reference voltage for greater than one switching cycle, an OV fault is set. During an overvoltage fault, S1 is driven off, S2 is driven on, and S3 and S4 are modulated to discharge the output voltage while preventing the inductor current from going beyond negative current limit.

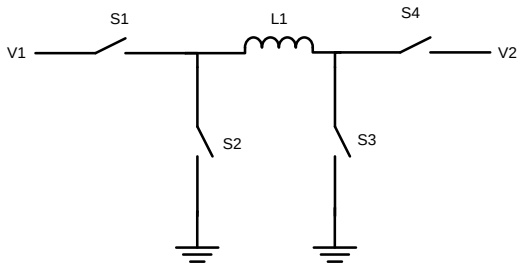


Figure 4. Diagram for OV Protection

During overvoltage fault detection set switching frequency from 450 kHz value to 50 kHz to reduce the power dissipation in the switches and prevent the inductor from saturating. OOV is disabled during voltage changes to ensure voltage changes and glitches during slewing are not falsely reported as faults. The OOV faults are reengaged 1 ms after completion of the soft start.

Power Good Monitor (PG)

NCV81598 provides two window comparators to monitor the internal feedback voltage. The target voltage window is ±5% of the reference voltage (typical). Once the feedback voltage is within the power good window, a power good indication is asserted once a 3.3 ms timer has expired. If the feedback voltage falls outside a ±7% window for greater than 1 switching cycle, the power good register is reset.

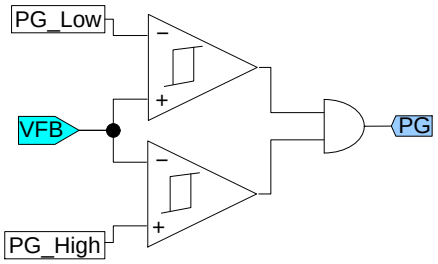


Figure 5. PG Block Diagram

Thermal Shutdown

The NCV81598 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold (typically 150°C), all MOSFETs will be driven to the off state, and the part will wait until the temperature decreases to an acceptable level. When the junction temperature drops below 125°C (typical), the part will discharge the output voltage to 0 V.

PFET Drive

The PMOS drive is an open drain output used to control the turn on and turn off of PMOSFET switches at a floating potential. The external PMOS can be used as a cutoff switch, enable for an auxiliary power supply, or a bypass switch for a power supply. The RDSon of the pulldown NMOSFET is typically 20 Ω allowing the user to quickly turn on large PMOSFET power channels.

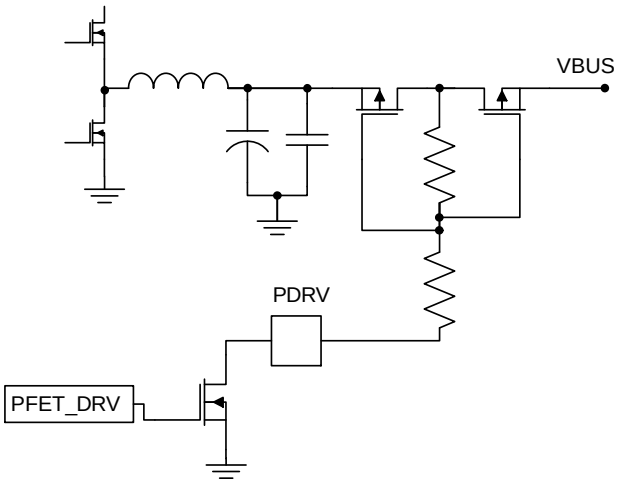
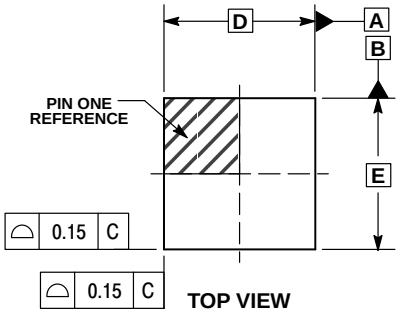
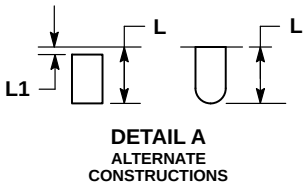


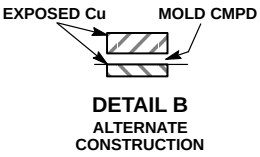
Figure 6. PFET Drive

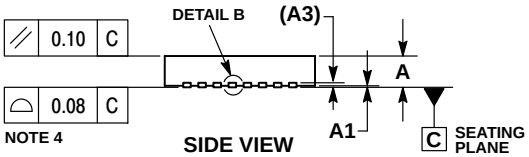
PACKAGE OUTLINE

QFN32 5x5, 0.5P
CASE 485CE
ISSUE O



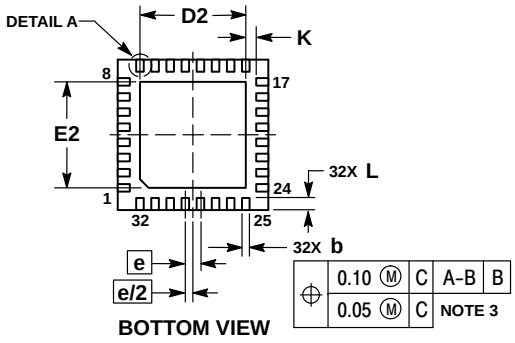




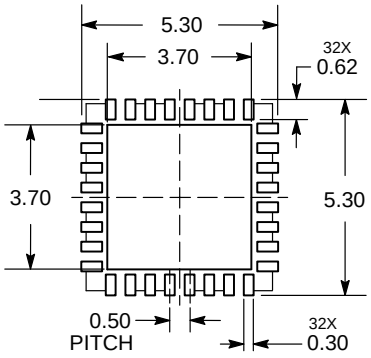


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	–––	0.05
A3	0.20 REF	
b	0.20	0.30
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.50 BSC	
K	0.20	–––
L	0.30	0.50
L1	–––	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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