NCV8161

LDO Regulator - Ultra-Low Noise, High PSRR, RF and Analog Circuits

450 mA

The NCV8161 is a linear regulator capable of supplying 450 mA output current. Designed to meet the requirements of RF and analog circuits, the NCV8161 device provides low noise, high PSRR, low quiescent current, and very good load/line transients. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in TSOP−5 and XDFN4 packages.

Features

- Operating Input Voltage Range: 1.9 V to 5.5 V
- Available in Fixed Voltage Option: 1.8 V to 5.14 V
- ±2% Accuracy Over Temperature
- Ultra Low Quiescent Current Typ. 18 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 225 mV at 450 mA
- Ultra High PSRR: Typ. 98 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 10 μV_{RMS}
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in TSOP−5 and XDFN4 Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable; Device Temperature Grade 1: −40°C to +125°C Ambient Operating Temperature Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Parking Camera Modules
- Wireless Handsets, Wireless LAN, Bluetooth®, Zigbee®
- Automotive Infotainment Systems
- Other Battery Powered Applications

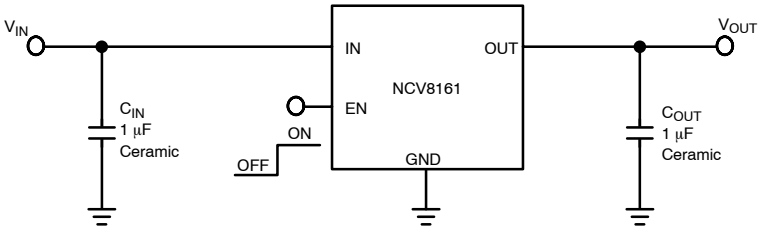
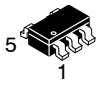


Figure 1. Typical Application Schematic

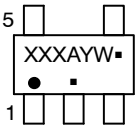
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM

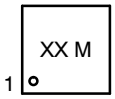


TSOP−5
CASE 483



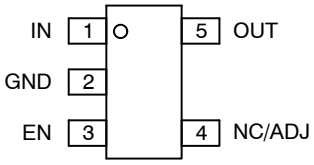
XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

XDFN4
CASE 711AJ

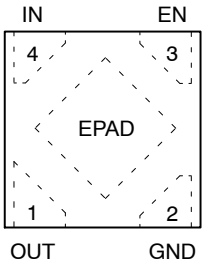


XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

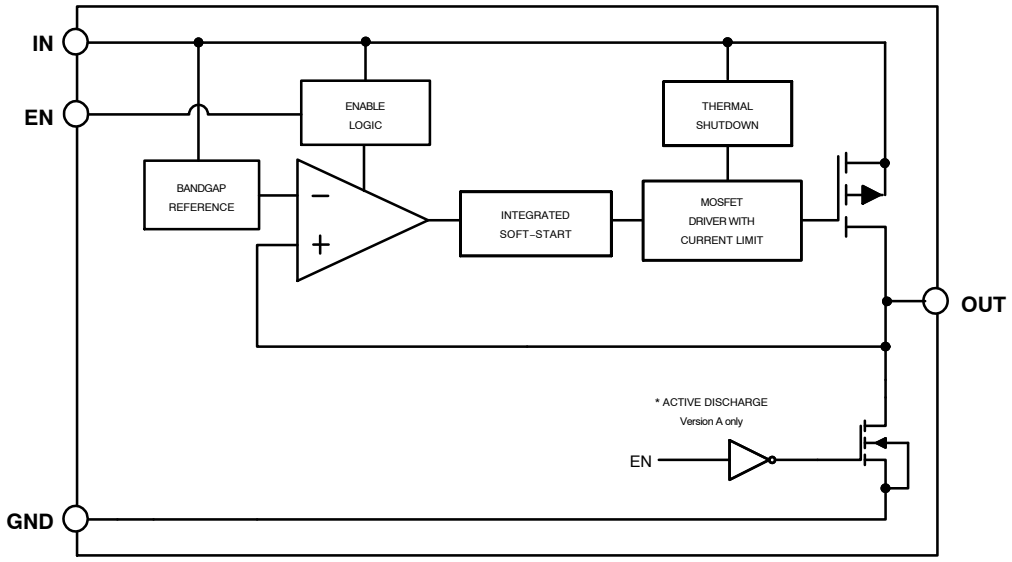


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin No. XDFN4	Pin Name	Description
1	4	IN	Input voltage supply pin
5	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor.
3	3	EN	Chip enable: Applying V_{EN} < 0.4 V disables the regulator, Pulling V_{EN} > 1.2 V enables the LDO.
2	2	GND	Common ground connection
4	–	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
–	EP	EPAD	Exposed Pad. Exposed pad can be tied to ground plane for better power dissipation.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Chip Enable Input	V_{CE}	−0.3 to V_{IN} + 0.3, max. 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−5 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	218	°C/W
Thermal Characteristics, XDFN4 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	198	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	1.9	5.5	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ μF, unless otherwise noted. $V_{EN} = 1.2$ V. Typical values are at $T_J = +25°C$ (Note 4).

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.9		5.5	V
Output Voltage Accuracy	$-40°C \le T_J \le 125°C$		V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT(NOM)} + 1$ V $\le V_{IN} \le 5.5$ V		$Line_{Reg}$		0.02		%/V
Load Regulation	I_{OUT} = 1 mA to 450 mA	XDFN4	$Load_{Reg}$		0.001	0.005	%/mA
		TSOP−5			0.005	0.008	
Dropout Voltage (Note 5)	I_{OUT} = 450 mA (XDFN4)	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		325	450	mV
		$V_{OUT(NOM)}$ = 2.8 V			195	290	
		$V_{OUT(NOM)}$ = 3.0 V			185	275	
		$V_{OUT(NOM)}$ = 3.3 V			175	260	
Dropout Voltage (Note 5)	I_{OUT} = 450 mA (TSOP−5)	$V_{OUT(NOM)}$ = 1.8 V	V_{DO}		365	480	mV
		$V_{OUT(NOM)}$ = 2.8 V			260	345	
		$V_{OUT(NOM)}$ = 3.0 V			240	330	
		$V_{OUT(NOM)}$ = 3.3 V			225	305	
Output Current Limit	V_{OUT} = 90% $V_{OUT(NOM)}$		I_{CL}	450	700		mA
Short Circuit Current	V_{OUT} = 0 V		I_{SC}		690		
Quiescent Current	I_{OUT} = 0 mA		I_Q		18	23	μA
Shutdown Current	$V_{EN} \le 0.4$ V, V_{IN} = 4.8 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	1.2			V
	EN Input Voltage “L”		V_{ENL}			0.4	
EN Pull Down Current	V_{EN} = 4.8 V		I_{EN}		0.2	0.5	μA
Turn−On Time	C_{OUT} = 1 μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$				120		μs
Power Supply Rejection Ratio	I_{OUT} = 20 mA	f = 100 Hz f = 1 kHz f = 10 kHz f = 100 kHz	PSRR		91 98 82 48		dB
Output Voltage Noise	f = 10 Hz to 100 kHz	I_{OUT} = 1 mA I_{OUT} = 250 mA	V_N		14 10		μV_{RMS}
Thermal Shutdown Threshold	Temperature rising		T_{SDH}		160		°C
	Temperature falling		T_{SDL}		140		°C
Active output discharge resistance	V_{EN} < 0.4 V, Version A only		R_{DIS}		280		Ω
Line transient (Note 6)	$V_{IN} = (V_{OUT(NOM)} + 1$ V) to $(V_{OUT(NOM)} + 1.6$ V) in 30 μs, I_{OUT} = 1 mA		$Tran_{LINE}$	−1			mV
	$V_{IN} = (V_{OUT(NOM)} + 1.6$ V) to $(V_{OUT(NOM)} + 1$ V) in 30 μs, I_{OUT} = 1 mA					+1	
Load transient (Note 6)	I_{OUT} = 1 mA to 450 mA in 10 μs		$Tran_{LOAD}$	−40			mV
	I_{OUT} = 450 mA to 1mA in 10 μs					+40	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.
6. Guaranteed by design.

TYPICAL CHARACTERISTICS

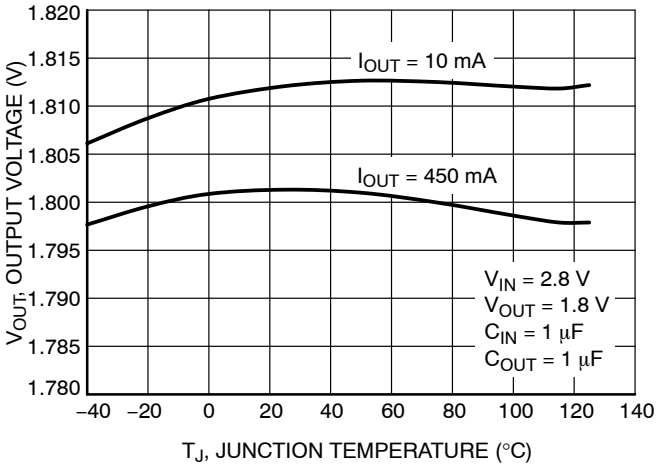


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V – XDFN Package

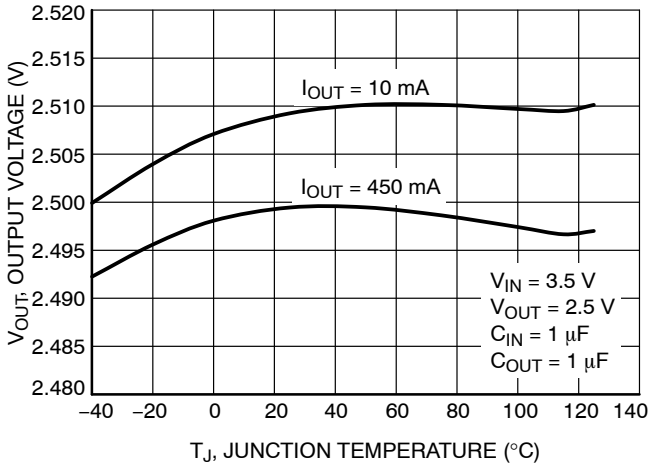


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 2.5 V – XDFN Package

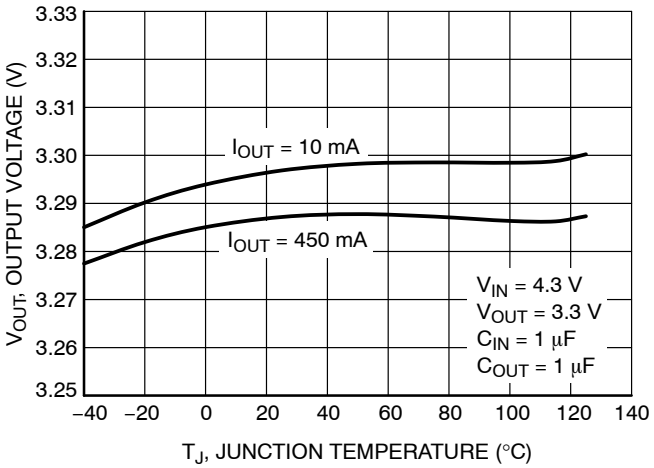


Figure 5. Output Voltage vs. Temperature – V_{OUT} = 3.3 V – XDFN Package

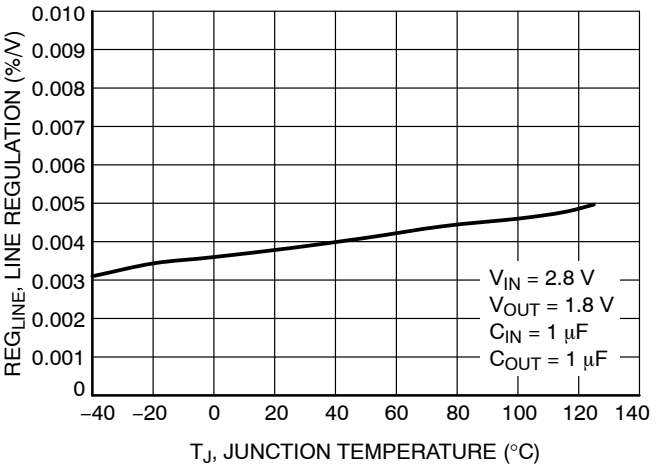


Figure 6. Line Regulation vs. Temperature – V_{OUT} = 1.8 V

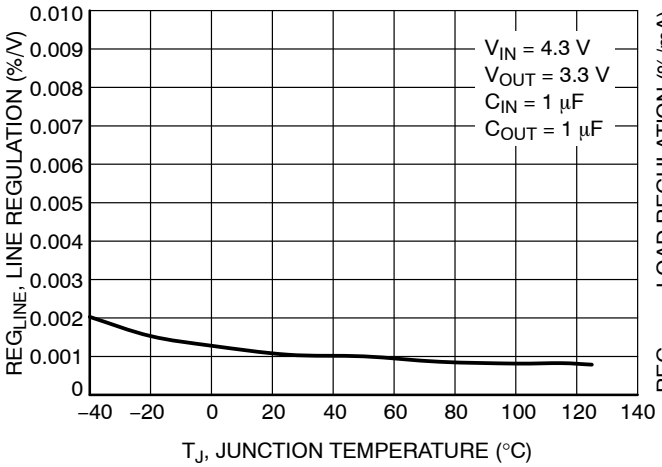


Figure 7. Line Regulation vs. Temperature – V_{OUT} = 3.3 V

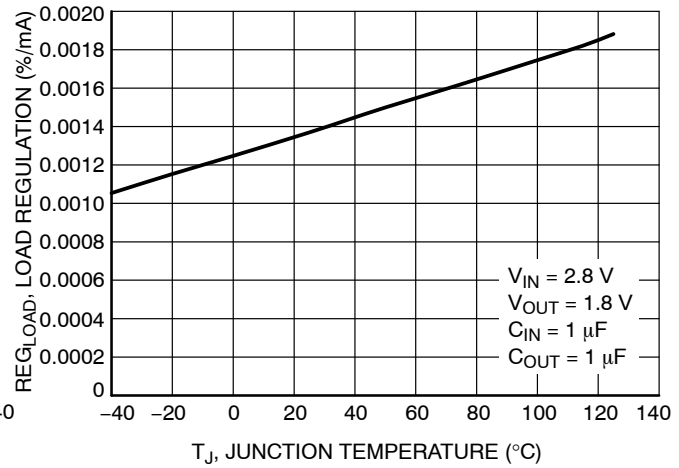


Figure 8. Load Regulation vs. Temperature – V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

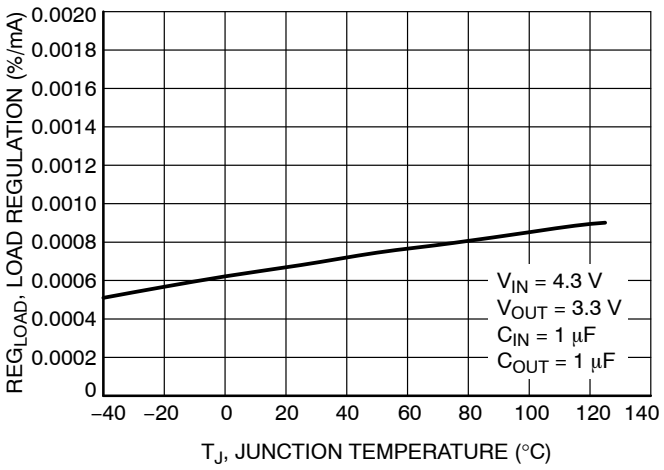


Figure 9. Load Regulation vs. Temperature – V_{OUT} = 3.3 V

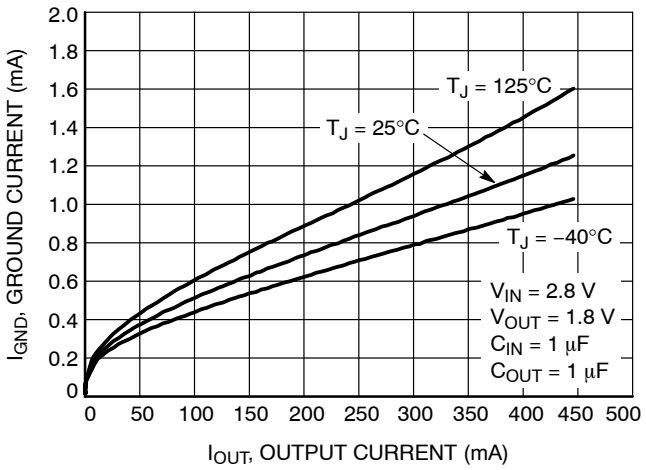


Figure 10. Ground Current vs. Load Current – V_{OUT} = 1.8 V

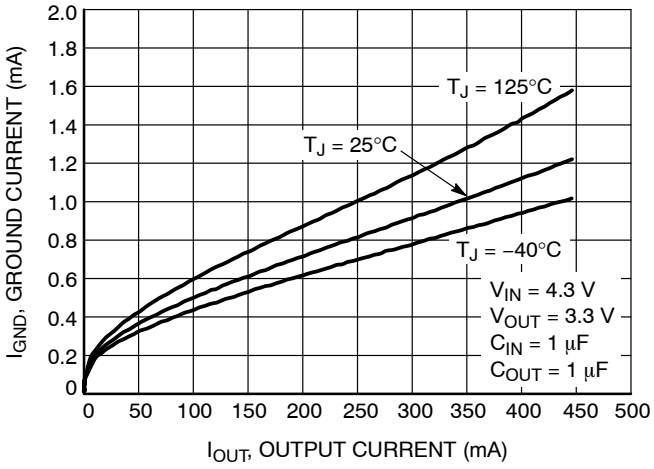


Figure 11. Ground Current vs. Load Current – V_{OUT} = 3.3 V

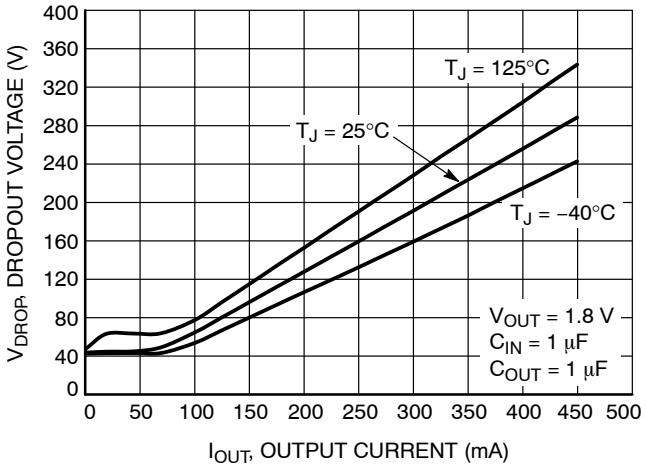


Figure 12. Dropout Voltage vs. Load Current – V_{OUT} = 1.8 V

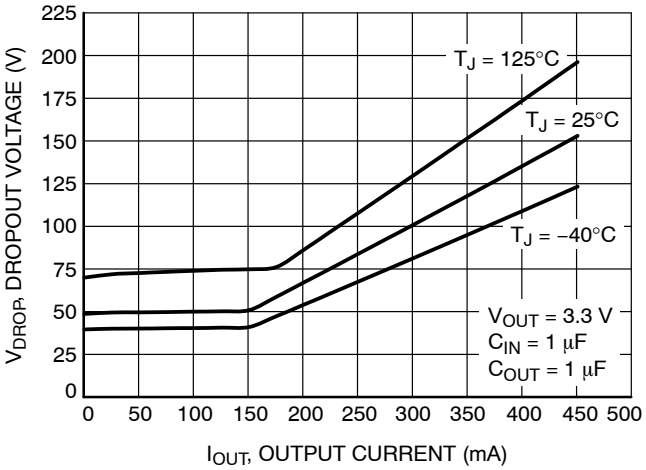


Figure 13. Dropout Voltage vs. Load Current – V_{OUT} = 3.3 V

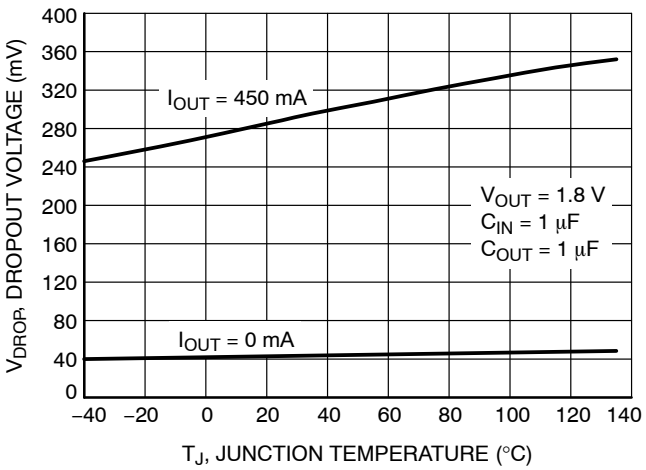


Figure 14. Dropout Voltage vs. Temperature– V_{OUT} = 1.8 V

TYPICAL CHARACTERISTICS

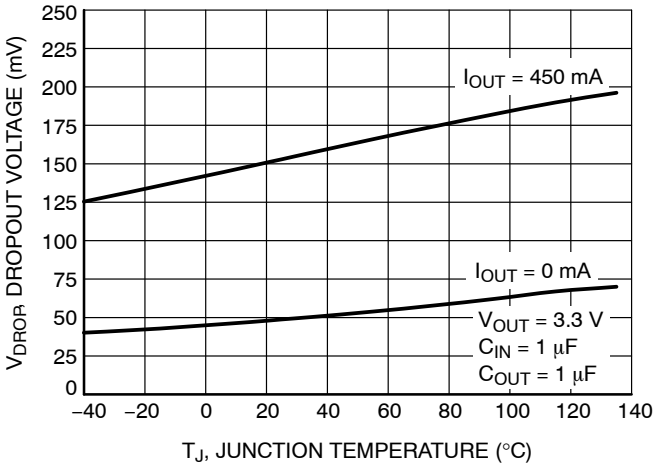


Figure 15. Dropout Voltage vs. Temperature– V_{OUT} = 3.3 V

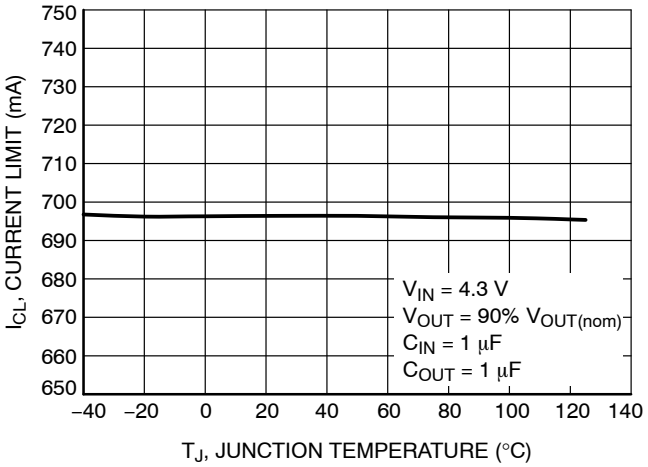


Figure 16. Current Limit vs. Temperature

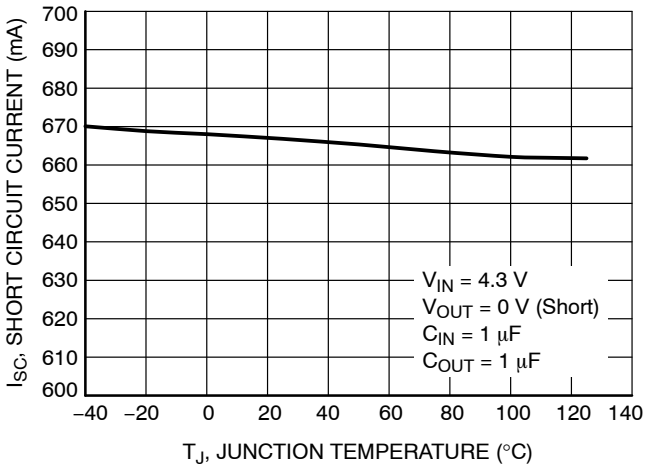


Figure 17. Short Circuit Current vs. Temperature

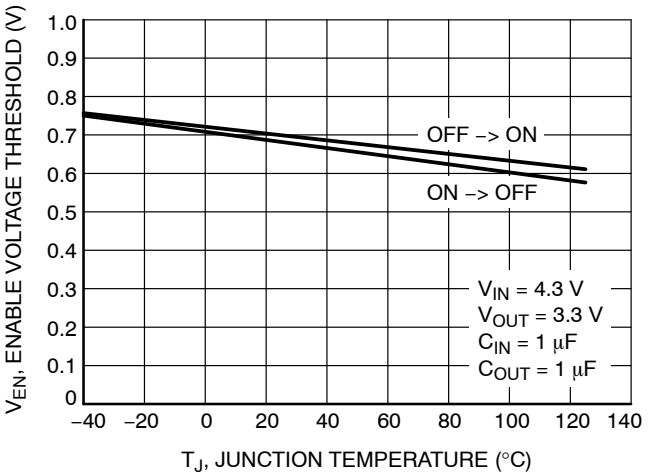


Figure 18. Enable Threshold Voltage vs. Temperature

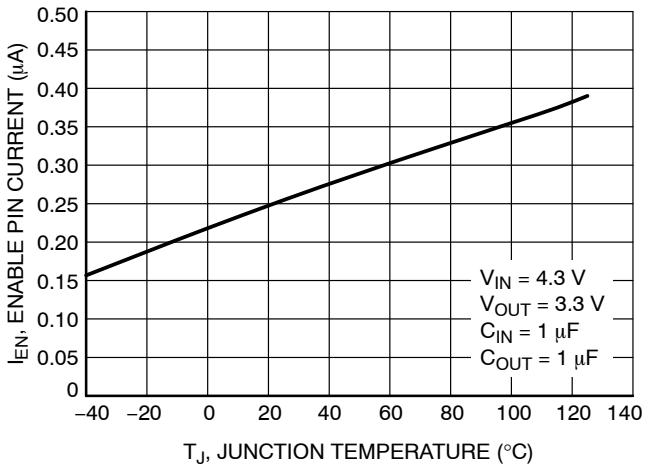


Figure 19. Enable Current Temperature

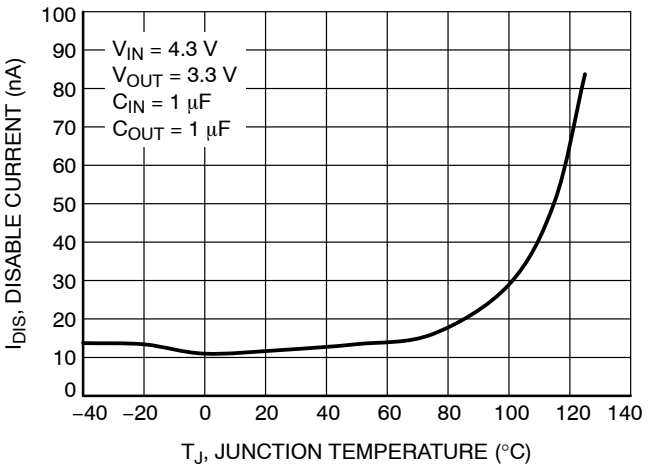


Figure 20. Disable Current vs. Temperature

TYPICAL CHARACTERISTICS

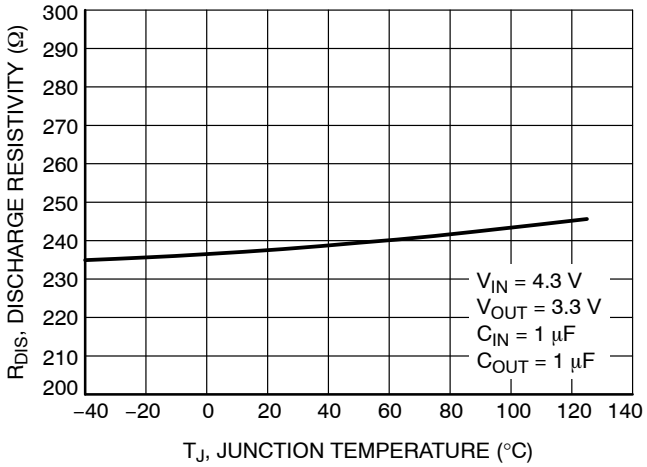
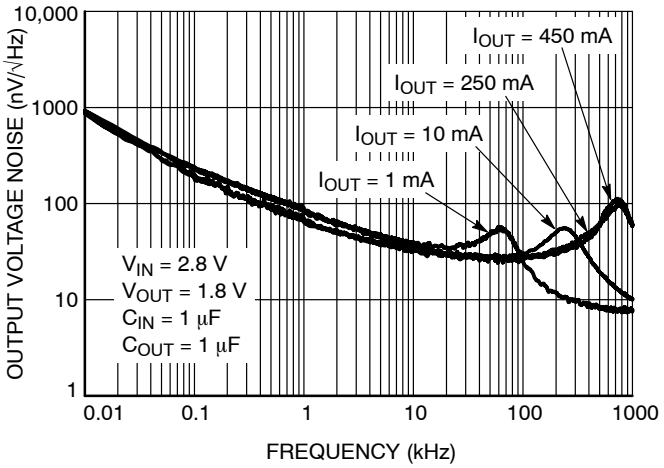
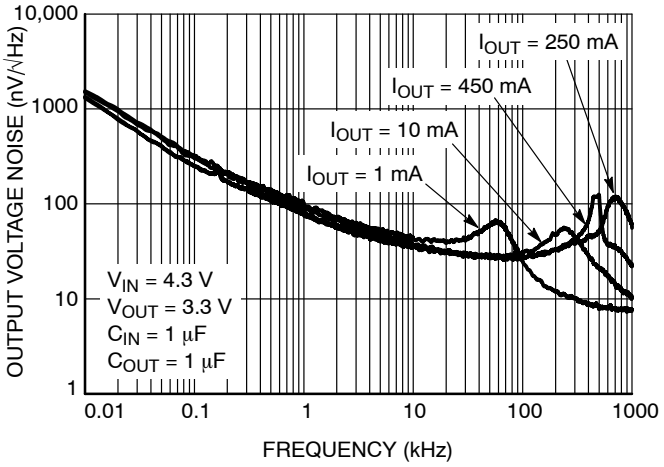


Figure 21. Discharge Resistivity vs. Temperature



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	14.62	14.10
10 mA	11.12	10.48
250 mA	10.37	9.82
450 mA	10.22	9.62

Figure 22. Output Voltage Noise Spectral Density – V_{OUT} = 1.8 V



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	16.9	15.79
10 mA	12.64	11.13
250 mA	11.96	10.64
450 mA	11.50	10.40

Figure 23. Output Voltage Noise Spectral Density – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

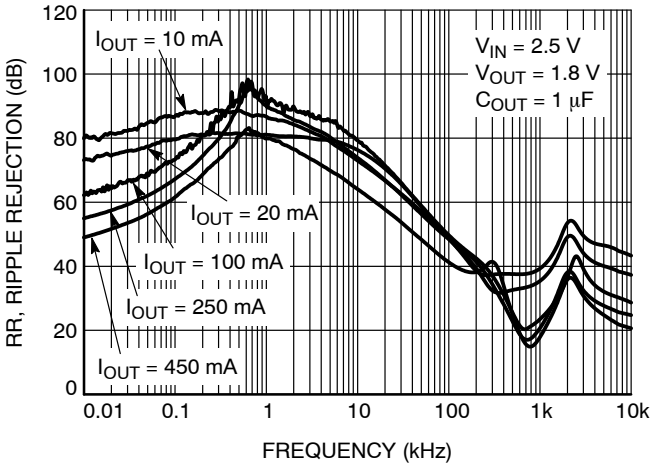


Figure 24. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

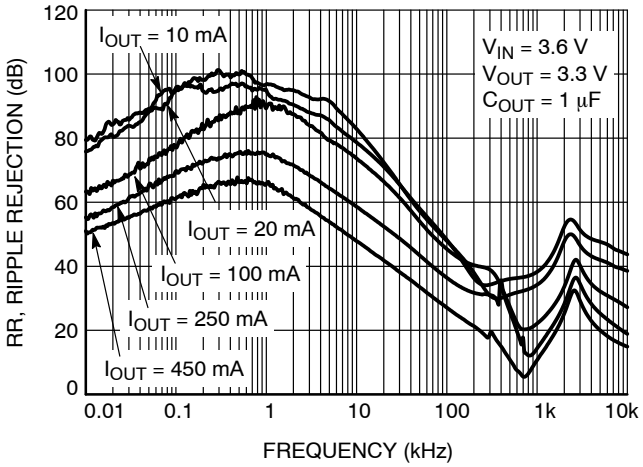


Figure 25. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

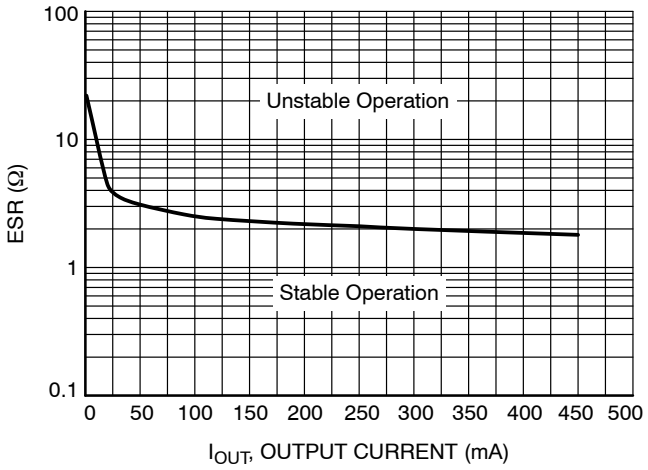


Figure 26. Stability vs. ESR

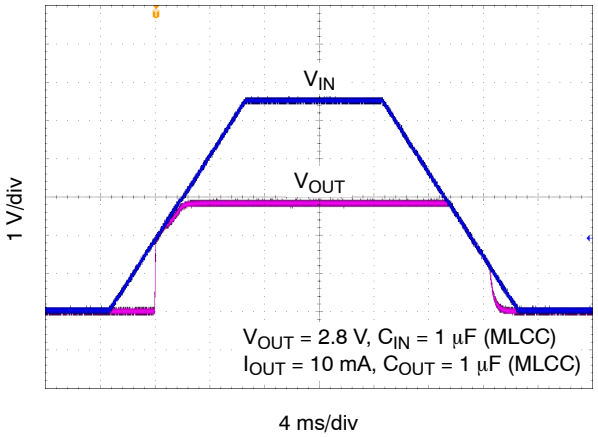


Figure 27. Turn−on/off − Slow Rising V_{IN}

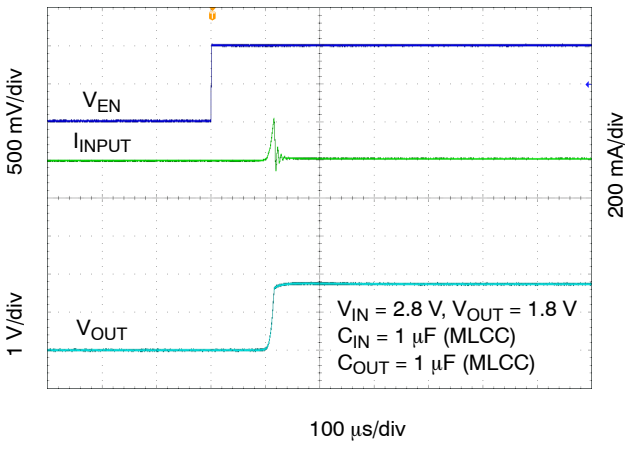


Figure 28. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 10 mA

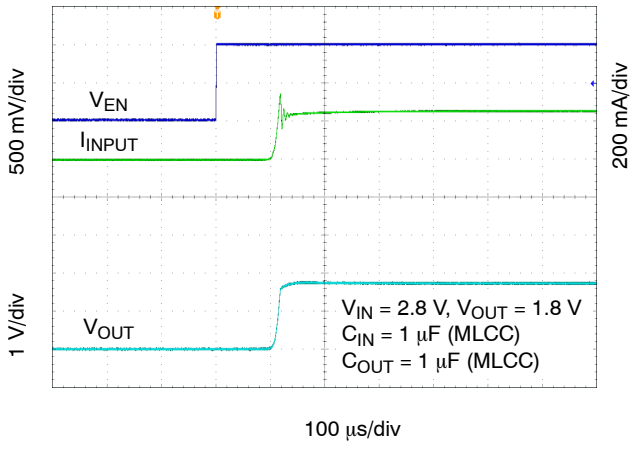


Figure 29. Enable Turn−on Response − C_{OUT} = 1 μF, I_{OUT} = 250 mA

TYPICAL CHARACTERISTICS

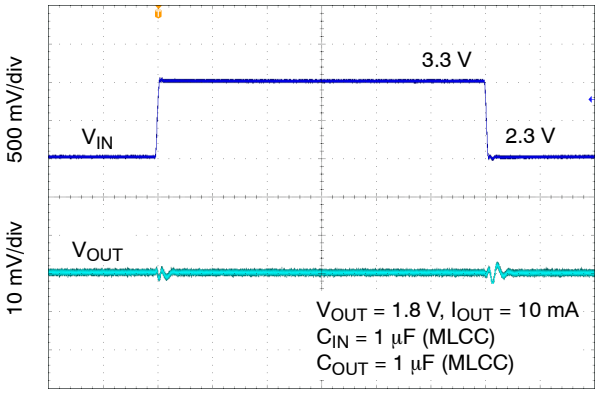


Figure 30. Line Transient Response – V_{OUT} = 1.8 V

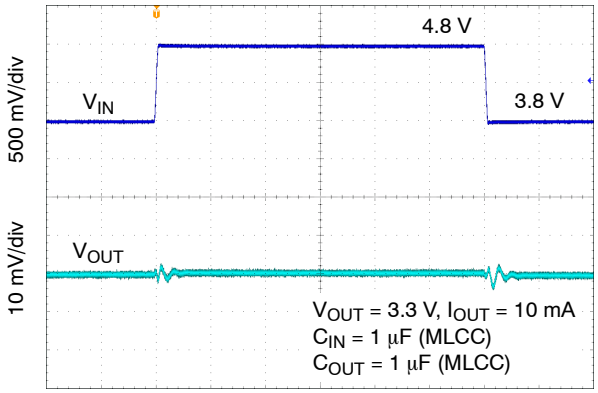


Figure 31. Line Transient Response – V_{OUT} = 3.3 V

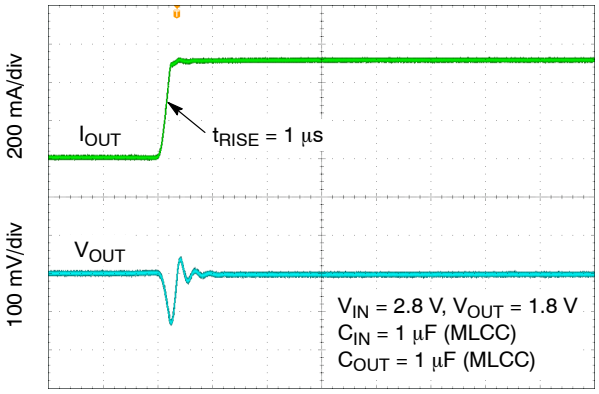


Figure 32. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 1.8 V

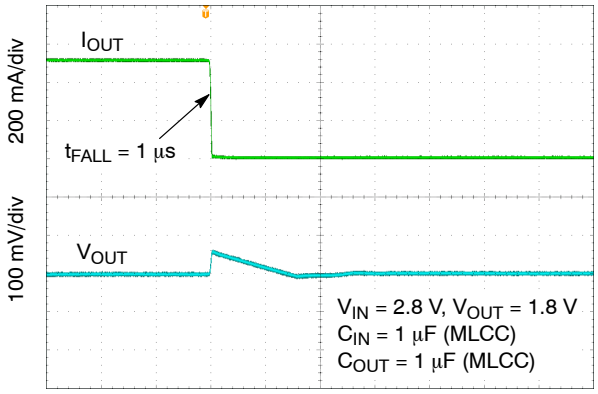


Figure 33. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 1.8 V

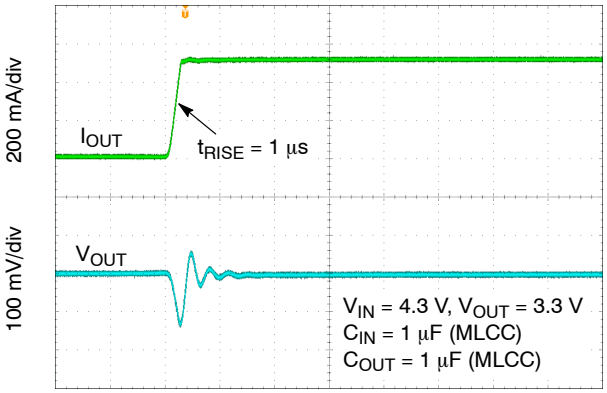


Figure 34. Load Transient Response – 1 mA to 450 mA – V_{OUT} = 3.3 V

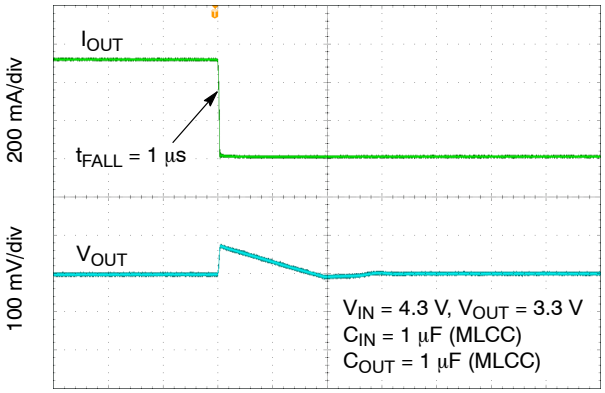


Figure 35. Load Transient Response – 450 mA to 1 mA – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

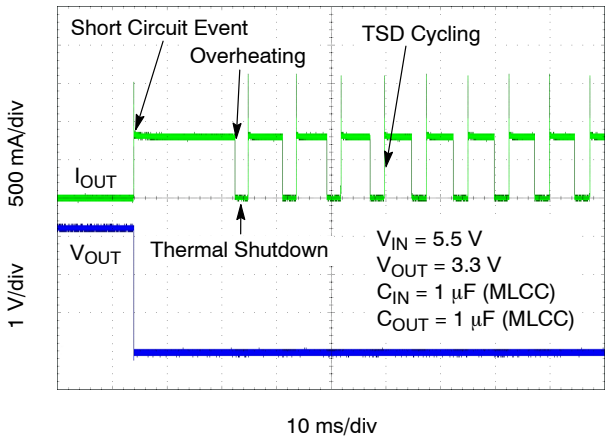


Figure 36. Short Circuit and Thermal Shutdown

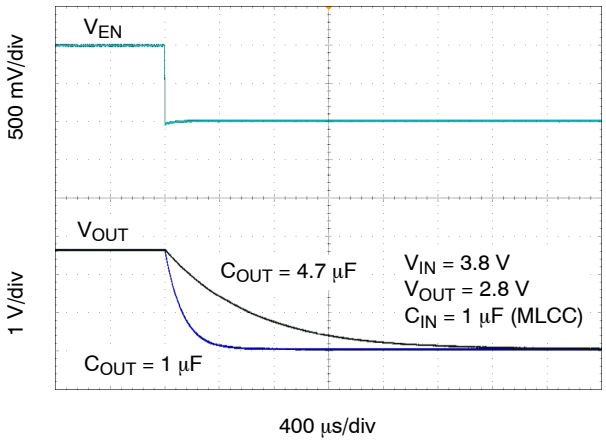


Figure 37. Enable Turn−off

APPLICATIONS INFORMATION

General

The NCV8161 is an ultra−low noise 450 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCV8161 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCV8161 is fully protected in case of current overload, output short circuit and overheating.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Decoupling (C_{OUT})

The NCV8161 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8161 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 38.

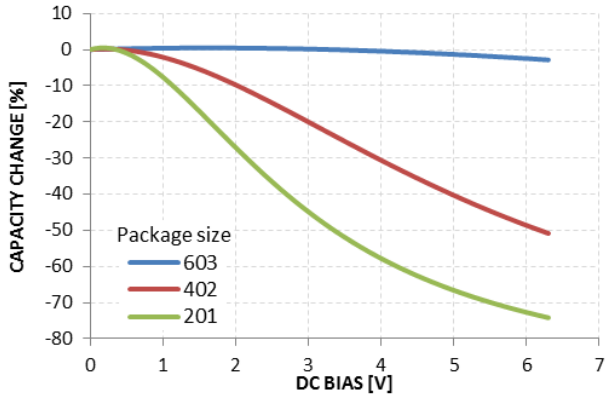


Figure 38. Capacity vs DC Bias Voltage

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCV8161 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCV8161 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCV8161 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8161 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature

rise for the part. For reliable operation, junction temperature should be limited to +125°C.

The maximum power dissipation the NCV8161 can handle is given by:

$$P_{D(MAX)} = \frac{[125^{\circ}C - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8161 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

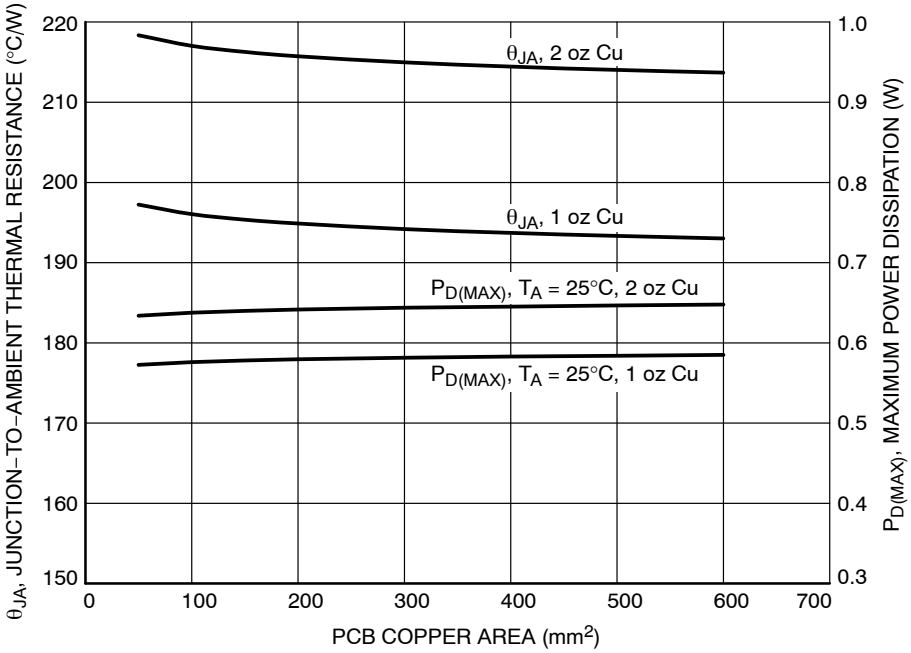


Figure 39. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4)

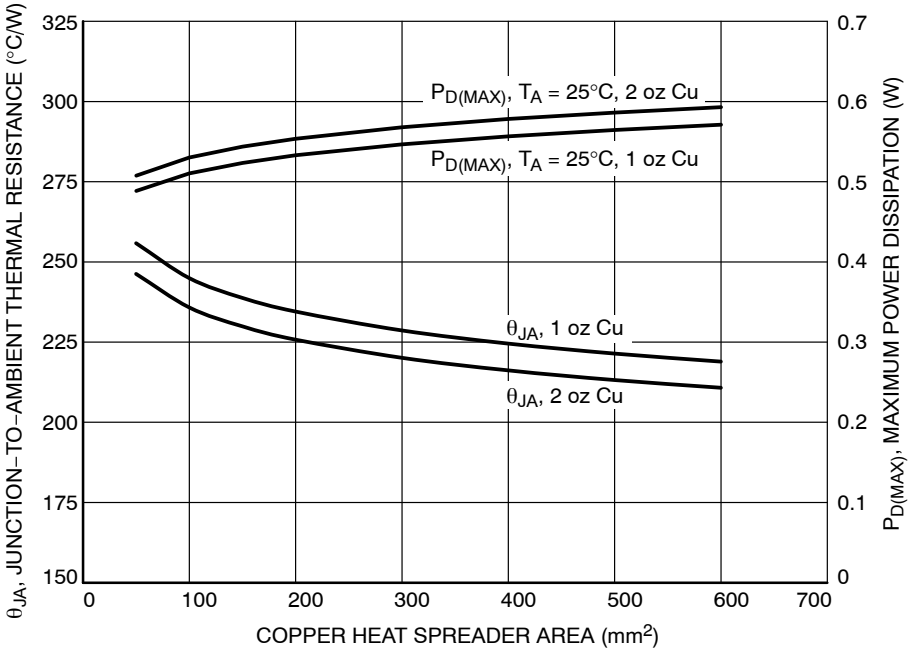


Figure 40. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (TSOP−5)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCV8161 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

ORDERING INFORMATION

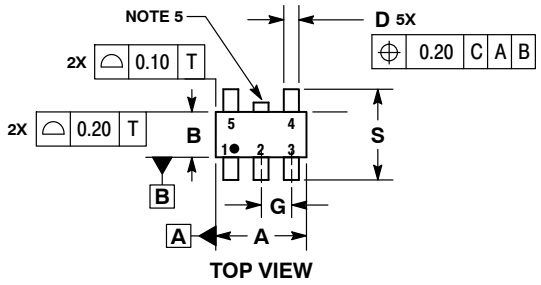
Device	Voltage Option	Marking	Description	Package	Shipping
NCV8161ASN180T1G	1.8 V	LKH	With Output Active Discharge Function	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCV8161ASN280T1G	2.8 V	LKL			
NCV8161ASN300T1G	3.0 V	LKJ			
NCV8161ASN330T1G	3.3 V	LKK			
NCV8161BSN180T1G	1.8 V	LKM	Without Output Active Discharge Function		
NCV8161BSN280T1G	2.8 V	LKN			
NCV8161BSN300T1G	3.0 V	LKP			
NCV8161BSN330T1G	3.3 V	LKQ			

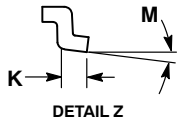
ORDERING INFORMATION

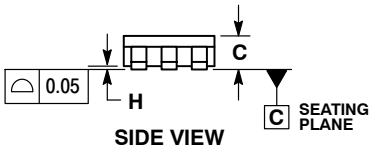
Device	Voltage Option	Marking	Description	Package	Shipping
NCV8161AMX180TBG	1.8 V	DN	With Output Active Discharge Function	XDFN4 (Pb-Free)	3000 / Tape & Reel
NCV8161AMX250TBG	2.5 V	DP			
NCV8161AMX280TBG	2.8 V	DQ			
NCV8161AMX290TBG	2.9 V	D5			
NCV8161AMX300TBG	3.0 V	DT			
NCV8161AMX330TBG	3.3 V	DD			
NCV8161BMX180TBG	1.8 V	EN	Without Output Active Discharge Function		
NCV8161BMX250TBG	2.5 V	EP			
NCV8161BMX280TBG	2.8 V	EQ			
NCV8161BMX300TBG	3.0 V	ET			
NCV8161BMX330TBG	3.3 V	ED			

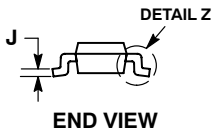
PACKAGE DIMENSIONS

TSOP−5
CASE 483
ISSUE M





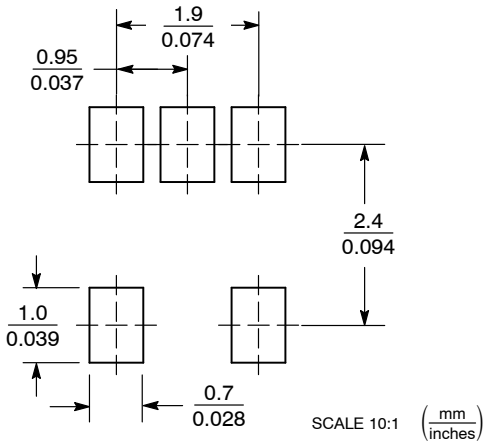




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

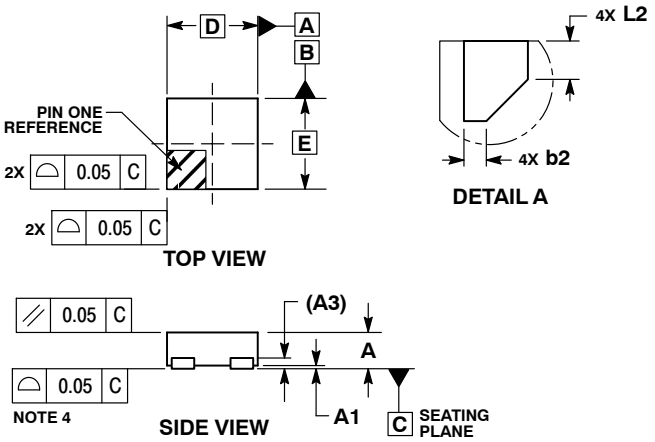
SOLDERING FOOTPRINT*

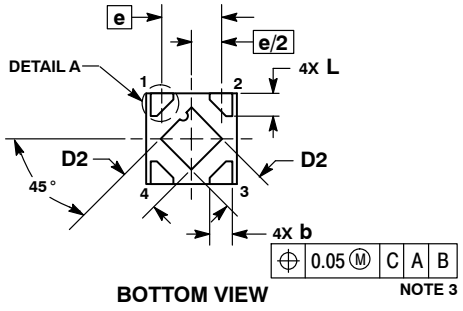


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE A

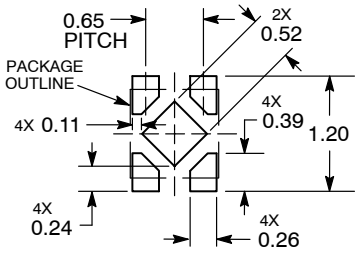




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.10 REF	
b	0.15	0.25
b2	0.02	0.12
D	1.00 BSC	
D2	0.43	0.53
E	1.00 BSC	
e	0.65 BSC	
L	0.20	0.30
L2	0.07	0.17

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Bluetooth is a registered trademark of Bluetooth SIG. ZigBee is a registered trademark of ZigBee Alliance.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative