NCV8186

LDO Regulator - Fast Transient Response, Low Voltage

1 A

The NCV8186x series are CMOS LDO regulators featuring 1 A output current. The input voltage is as low as 1.8 V and the output voltage can be set from 1.2 V.

Features

- Operating Input Voltage Range: 1.8 V to 5.5 V
- Output Voltage Range: 1.2 to 3.9 V
- Quiescent Current typ. 90 μA
- Low Dropout: 100 mV typ. at 1 A, V_{OUT} = 3.0 V
- High Output Voltage Accuracy ±1%
- Stable with Small 1 μF Ceramic Capacitors
- Over−current Protection
- Built−in Soft Start Circuit to Suppress Inrush Current
- Thermal Shutdown Protection: 165°C
- With (NCV8186A) and Without (NCV8186B) Output Discharge Function
- Available in Small DFN8 2 x 2 mm Package
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Telematics, Infotainment & Cluster, General Purpose Automotive
- Building & Factory Automation, Smart Meters, and General Industrial

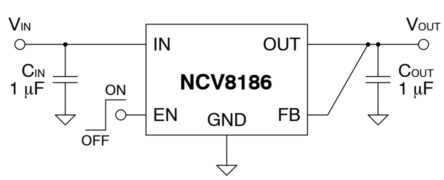

Figure 1. Typical Application Schematic

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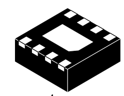
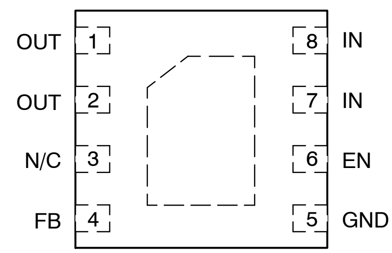


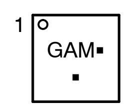
DFN8
MX SUFFIX
CASE 506AA

PIN CONNECTIONS



(Top View)

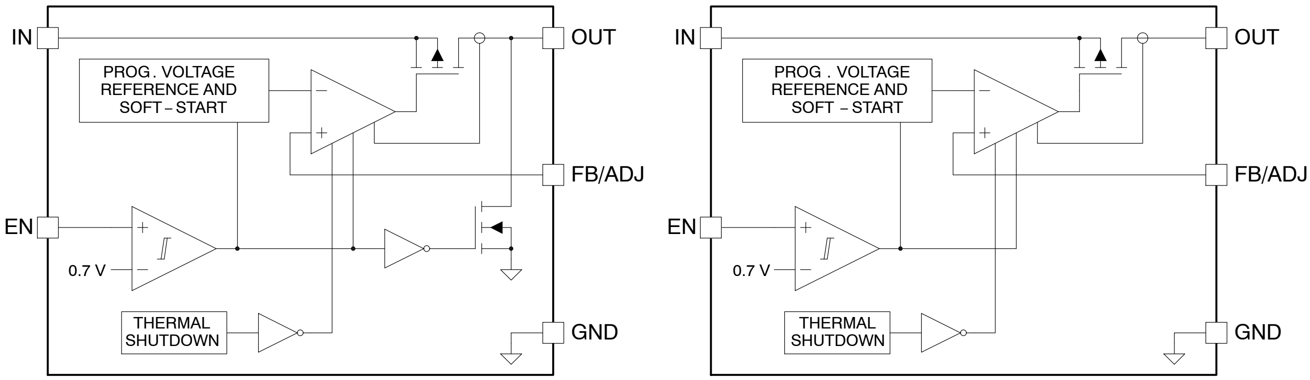
MARKING DIAGRAM



GA = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 9 of this data sheet.



NCV8186A (with output discharge) NCV8186B (without output discharge)

Figure 2. Internal Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. DFN8	Pin Name	Description
1	OUT	LDO output pin
2		
3	N/C	Not internally connected. This pin can be tied to the ground plane to improve thermal dissipation.
4	FB	Feedback input pin
5	GND	Ground pin
6	EN	Chip enable input pin (active “H”)
7	IN	Power supply input pin
8		
EPAD	EPAD	It’s recommended to connect the EPAD to GND, but leaving it open is also acceptable

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	IN	−0.3 to 6.0	V
Output Voltage	OUT	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	EN	−0.3 to 6.0	V
Output Current	I_{OUT}	Internally Limited	mA
Maximum Junction Temperature	$T_{J(MAX)}$	125	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air, DFN8 2 mm x 2 mm (Note 3)	$R_{\theta JA}$	93	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7.

Table 4. ELECTRICAL CHARACTERISTICS
$V_{IN} = V_{OUT\_NOM} + 0.5$ V or $V_{IN} = 1.8$ V whichever is greater; $I_{OUT} = 1$ mA; $C_{IN} = C_{OUT} = 1.0$ µF (effective capacitance) (Note 5); $V_{EN} = 1.2$ V; $T_J = 25°C$; unless otherwise noted. The specifications in bold are guaranteed at $-40°C \le T_J \le 125°C$. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	**1.8**		**5.5**	V
Output Voltage	$V_{OUT\_NOM} + 0.5\ V \le V_{IN} \le 5.5$ V, $I_{OUT} = 0$ to 1 A, $-40°C \le T_J \le 85°C$	V_{OUT}	−1.0		1.0	%
	$V_{OUT\_NOM} + 0.5\ V \le V_{IN} \le 5.5$ V, $I_{OUT} = 0$ to 1 A, $-40°C \le T_J \le 125°C$		**−2.0**		**1.0**	
Load Regulation	$I_{OUT} = 1$ mA to 1000 mA	LoadReg		0.7	**5.0**	mV
Line Regulation	$V_{IN} = V_{OUT\_NOM} + 0.5$ V to 5.0 V	LineReg		0.002	**0.1**	%/V
Dropout Voltage	$I_{OUT} = 1$ A; When V_{OUT} falls to $V_{OUT\_NOM} - 100$ mV; $V_{OUT\_NOM} = 1.75$ V	V_{DO}		210	**310**	mV
	$V_{OUT\_NOM} = 3.3$ V			115	**170**	
Quiescent Current	$I_{OUT} = 0$ mA	I_Q		90	**140**	µA
Standby Current	$V_{EN} = 0$ V	I_{STBY}		0.1	**1.5**	µA
Output Current Limit	$V_{OUT} = 90\%$ of V_{OUT_NOM}	I_{OCL}	**1100**	1400		mA
Output Short Circuit Current	$V_{OUT} = 0$ V	I_{OSC}	**1100**	1400		mA
Enable Input Current		I_{EN}		0.15	**0.6**	µA
Enable Threshold Voltage	EN Input Voltage “H”	V_{ENH}	**1.0**			V
	EN Input Voltage “L”	V_{ENL}			**0.4**	
Power Supply Rejection Ratio	$V_{IN} = V_{OUT\_NOM} + 1.0$ V, Ripple 0.2 Vp−p, $I_{OUT} = 30$ mA, f = 1 kHz	PSRR		75		dB
Output Noise	f = 10 Hz to 100 kHz	V_N		48		μV_{RMS}
Output Discharge Resistance (NCV8186A option only)	$V_{IN} = 5.5$ V, $V_{EN} = 0$ V, $V_{OUT} = 1.75$ V	R_{AD}		34		Ω
Thermal Shutdown Temperature	Temperature rising from $T_J = +25°C$	T_{SD}		165		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}	T_{SDH}		20		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 0.5$ V or $V_{IN} = 1.8$ V whatever is greater, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ μF, $T_J = 25°C$.

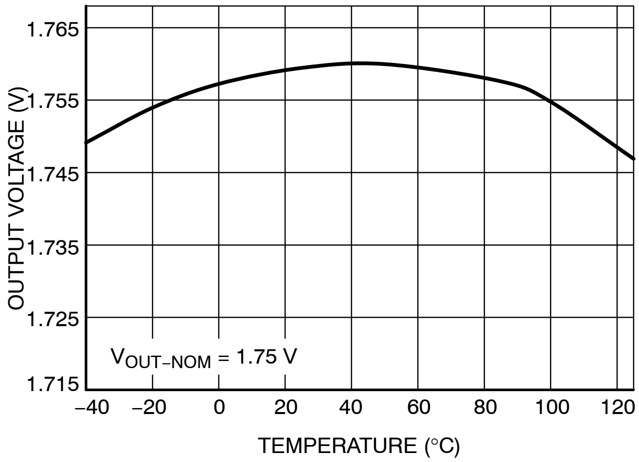


Figure 3. Output Voltage vs. Temperature

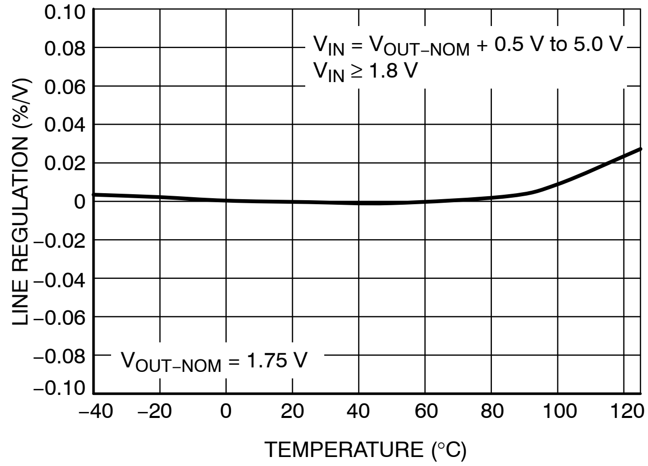


Figure 4. Line Regulation vs. Temperature

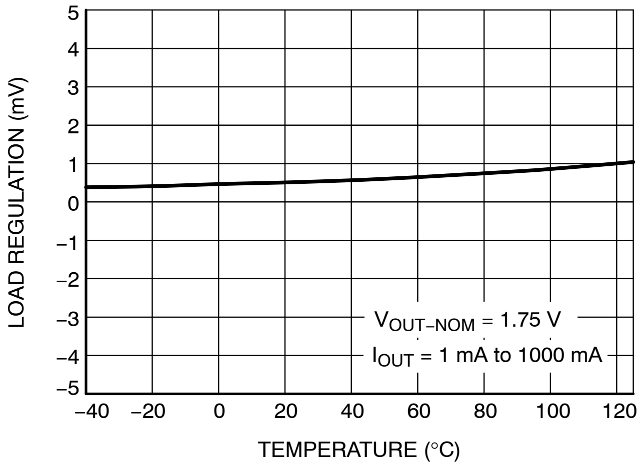


Figure 5. Load Regulation vs. Temperature

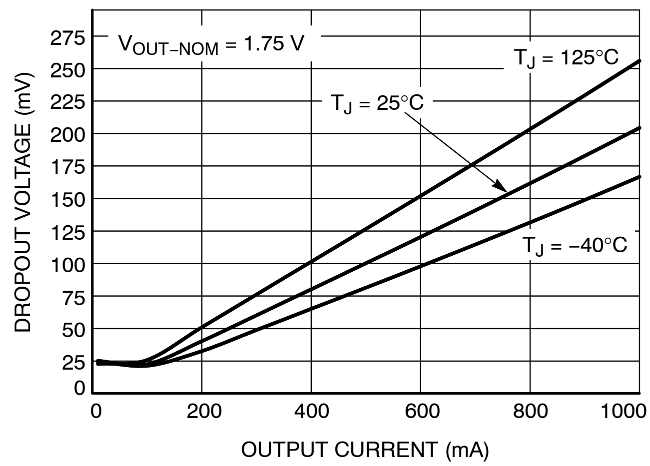


Figure 6. Dropout Voltage vs. Output Current

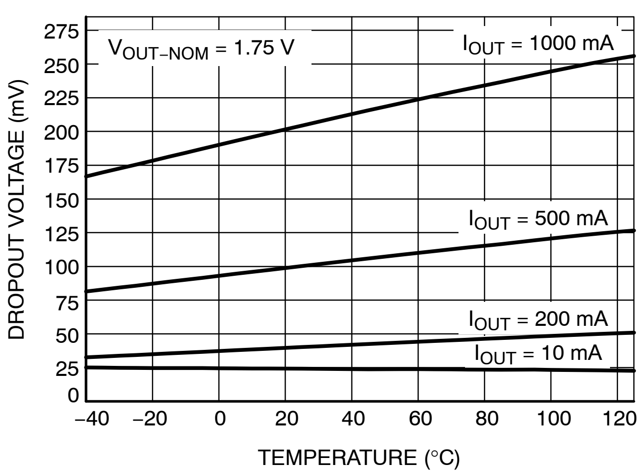


Figure 7. Dropout Voltage vs. Temperature

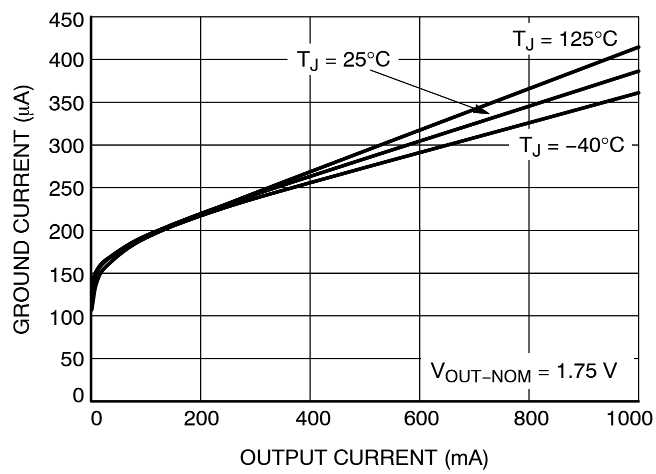


Figure 8. Ground Current vs. Output Current

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 0.5$ V or $V_{IN} = 1.8$ V whatever is greater, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF, $T_J = 25$°C.

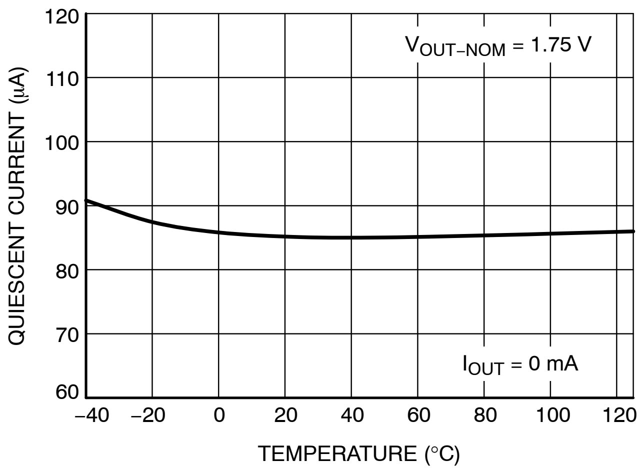


Figure 9. Quiescent Current vs. Temperature

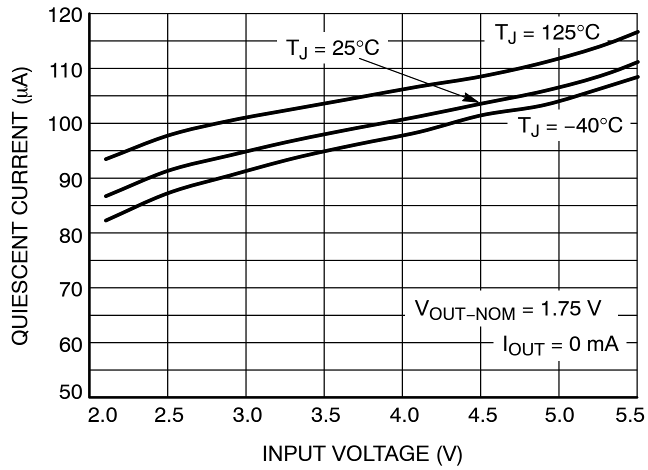


Figure 10. Quiescent Current vs. Input Voltage

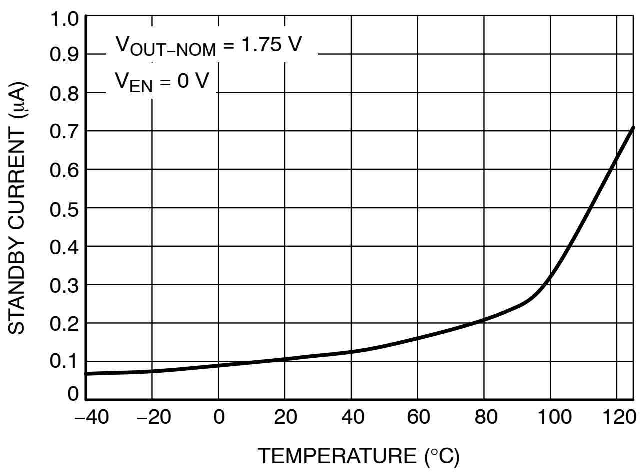


Figure 11. Standby Current vs. Temperature

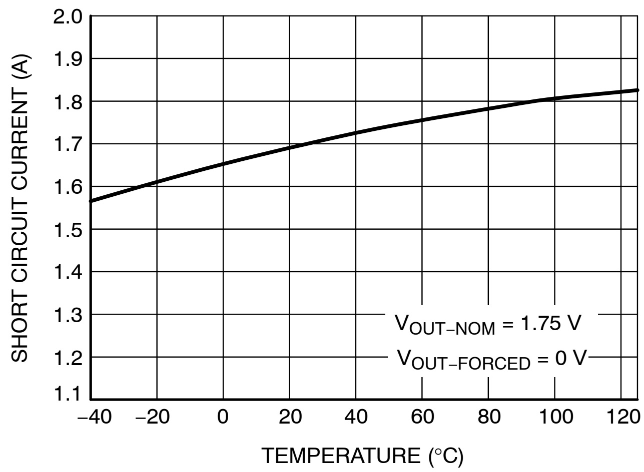


Figure 12. Short Circuit Current vs. Temperature

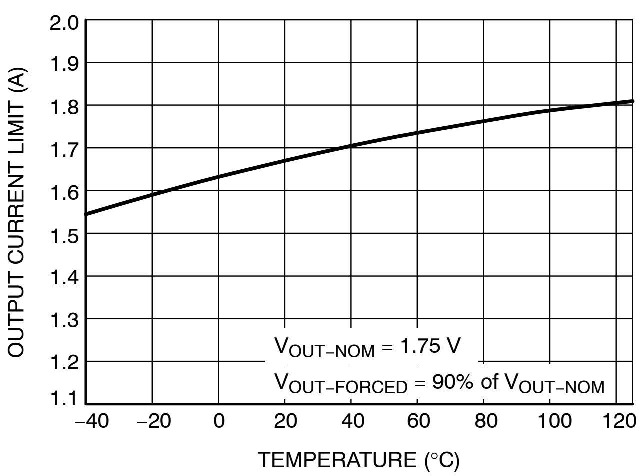


Figure 13. Output Current Limit vs. Temperature

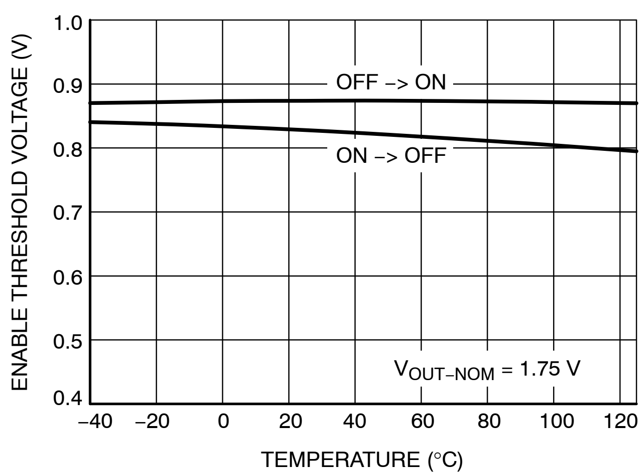


Figure 14. Enable Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 0.5$ V or $V_{IN} = 1.8$ V whatever is greater, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ μF, $T_J = 25°C$.

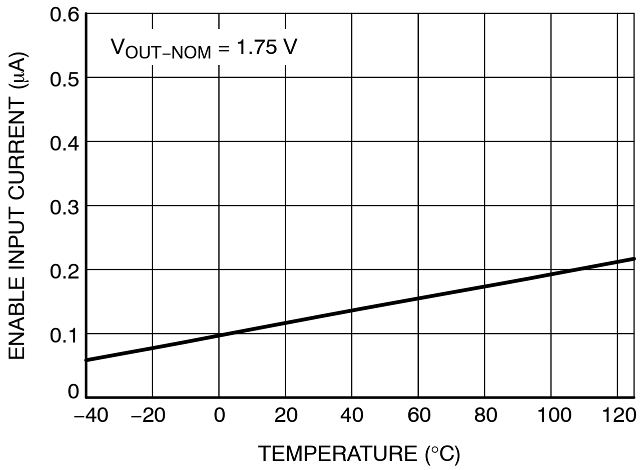


Figure 15. Enable Input Current vs. Temperature

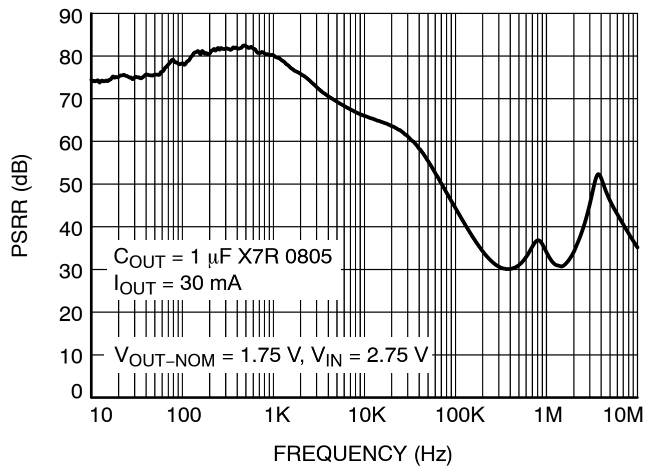


Figure 16. Power Supply Rejection Ratio

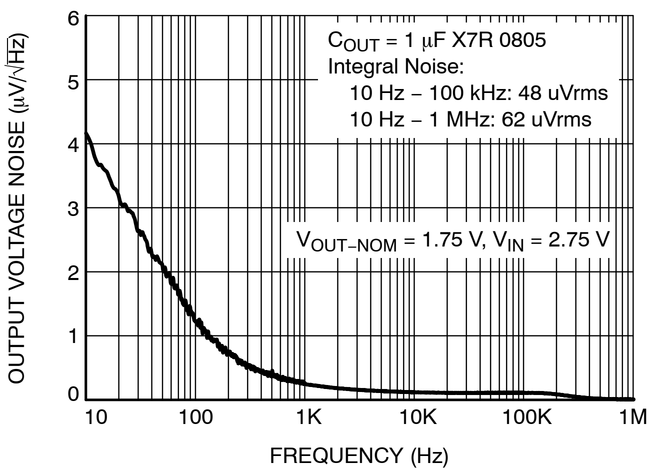


Figure 17. Output Voltage Noise Spectral Density

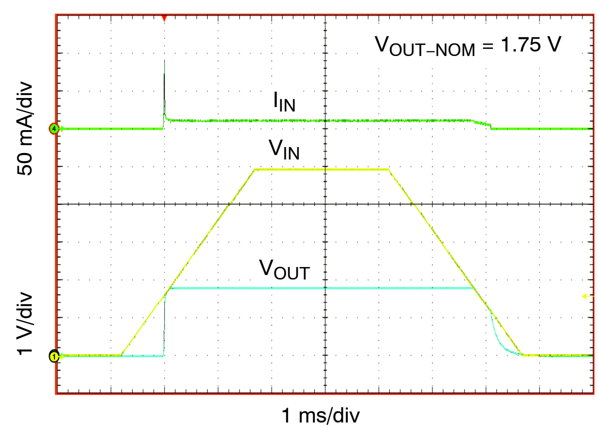


Figure 18. Turn−ON/OFF – V_{IN} Driven (slow)

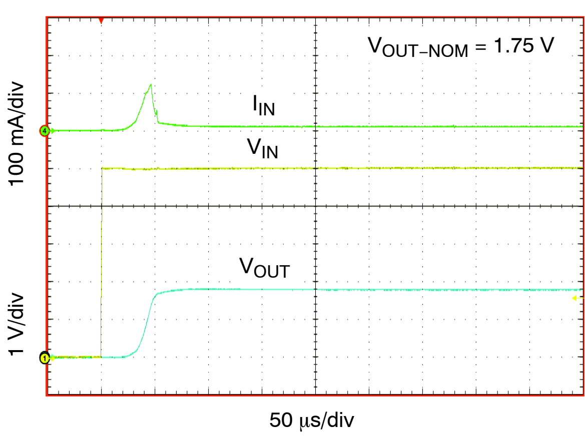


Figure 19. Turn−ON – V_{IN} Driven (fast)

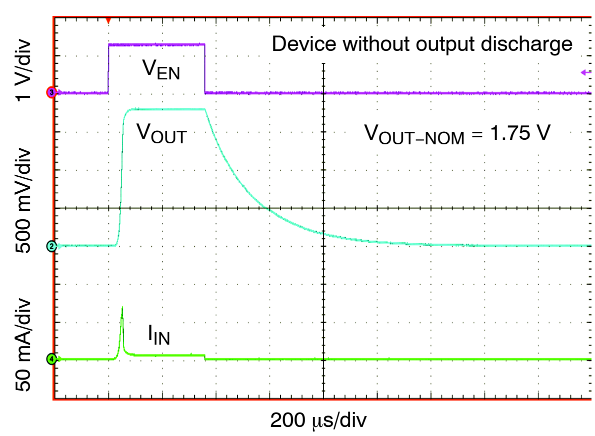


Figure 20. Turn−ON/OFF – EN Driven

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 0.5$ V or $V_{IN} = 1.8$ V whatever is greater, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF, $T_J = 25°C$.

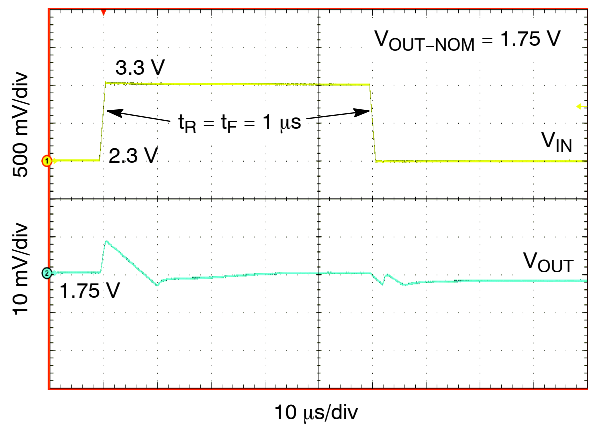


Figure 21. Line Transient Response

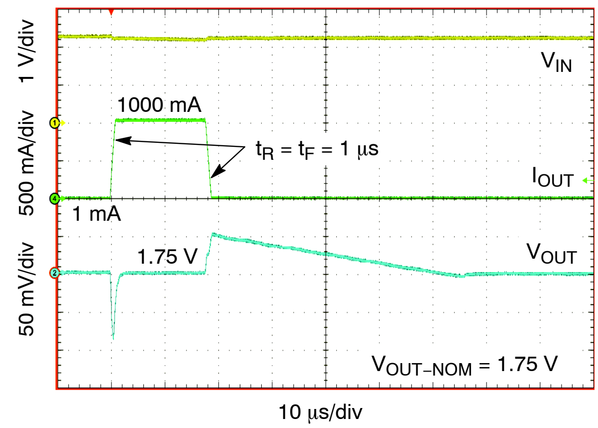


Figure 22. Load Transient Response

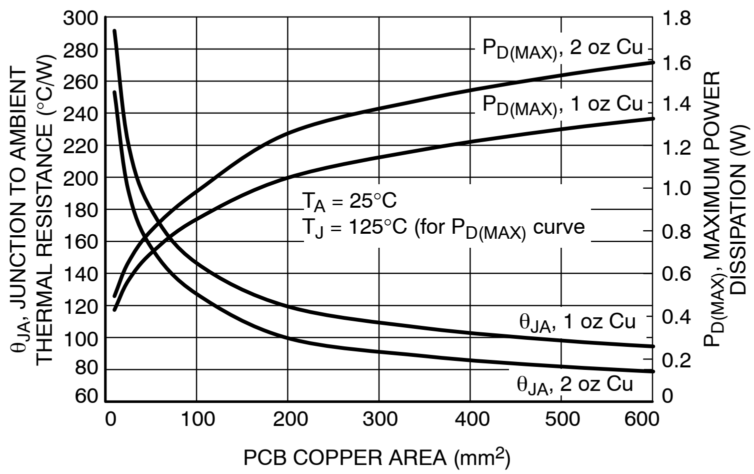


Figure 23. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

APPLICATIONS INFORMATION

General

The NCV8186 is a high performance 1 A low dropout linear regulator (LDO) delivering excellent noise and dynamic performance. Thanks to its adaptive ground current behavior the device consumes only 90 μA typ. of quiescent current (no−load condition).

The regulator features low noise of 48 μV_{RMS}, PSRR of 75 dB at 1 kHz and very good line/load transient performance. Such excellent dynamic parameters, small dropout voltage and small package size make the device an ideal choice for powering the precision noise sensitive circuitry in portable applications.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as 100 nA typ. from the IN pin.

The device is fully protected in case of output overload, output short circuit condition or overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater for the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage.

There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes.

Output Capacitor Selection (C_{OUT})

The LDO requires an output capacitor connected as close as possible to the output and ground pins. The recommended capacitor value is 1 μF, ceramic X7R or X5R type due to its low capacitance variations over the specified temperature range. The LDO is designed to remain stable with minimum effective capacitance of 0.8 μF. When selecting the capacitor the changes with temperature, DC bias and package size needs to be taken into account. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details).

There is no requirement for the minimum value of equivalent series resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 0.5 Ω. Larger capacitance and lower ESR improves the load transient response and high frequency PSRR. Only ceramic capacitors are recommended, the other types like tantalum capacitors not due to their large ESR.

Enable Operation

The LDO uses the EN pin to enable/disable its operation and to deactivate/activate the output discharge function (A−version only).

If the EN pin voltage is < 0.4 V the device is disabled and the pass transistor is turned off so there is no current flow between the IN and OUT pins. On A−version the active discharge transistor is active so the output voltage is pulled to GND through 34 Ω (typ.) resistor.

If the EN pin voltage is > 1.0 V the device is enabled and regulates the output voltage. The active discharge transistor is turned off.

The EN pin has internal pull−down current source with value of 150 nA typ. which assures the device is turned off when the EN pin is unconnected. In case when the EN function isn't required the EN pin should be tied directly to IN pin.

Output Current Limit

Output current is internally limited to a 1.4 A typ. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is 90% of $V_{OUT-NOM}$). If the output voltage is shorted to ground, the short circuit protection will limit the output current to 1.4 A typ. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Thermal Shutdown

When the LDO's die temperature exceeds the thermal shutdown threshold value the device is internally disabled. The IC will remain in this state until the die temperature decreases by value called thermal shutdown hysteresis. Once the IC temperature falls this way the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} \text{ [W]} \qquad \text{(eq. 1)}$$

Where ($T_J - T_A$) is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT}\ [W] \quad \text{(eq. 2)}$$

Where I_{GND} is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and N/C pin to a large ground planes helps to dissipate the heat from the chip.

The relation of θ_{JA} and $P_{D(MAX)}$ to PCB copper area and Cu layer thickness could be seen on the Figure 23.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case when $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The LDO features very high power supply rejection ratio. The PSRR at higher frequencies (in the range above 100 kHz) can be tuned by the selection of C_{OUT} capacitor and proper PCB layout. A simple LC filter could be added to the LDO's IN pin for further PSRR improvement.

Enable Turn−On Time

The enable turn−on time is defined as the time from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT-NOM}$, C_{OUT} and T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors as close as possible to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors size with appropriate effective capacitance.

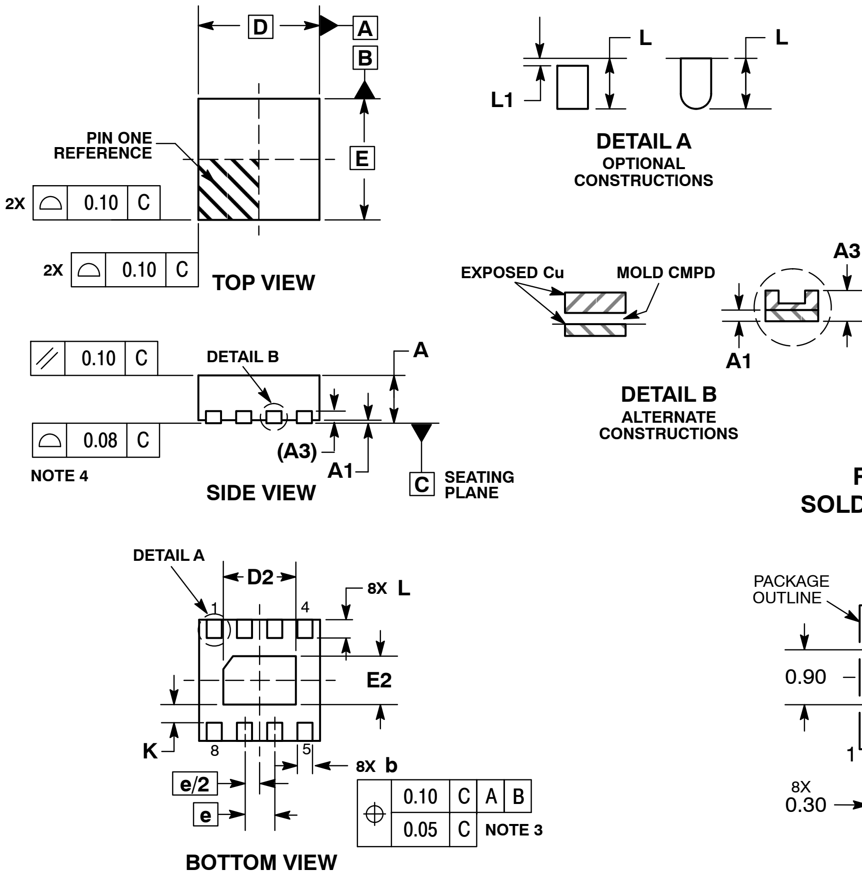
Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Power Dissipation section). Exposed pad and N/C pin should be tied to the ground plane for good power dissipation.

ORDERING INFORMATION TABLE

Part Number	Voltage Option	Marking	Option	Package	Shipping
NCV8186AMN330TAG	3.3 V	GD	With active discharge	DFN8 (Pb−Free)	3000 / Tape & Reel
NCV8186BMN175TAG	1.75 V	GA	Without active discharge		
NCV8186BMN330TAG	3.3 V	GK			

PACKAGE DIMENSIONS

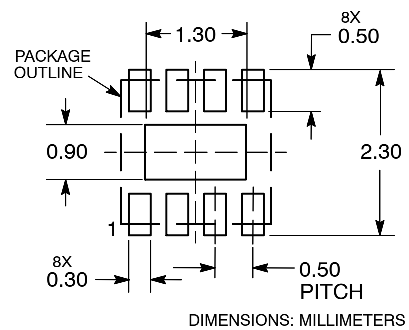
DFN8 2x2, 0.5P
CASE 506AA
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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