NCV8187

1.2 A Low Iq, Low Dropout Voltage Regulator with Power Good Output

The NCV8187 is 1.2 A LDO Linear Voltage Regulator. It is a very stable and accurate device with low quiescent current consumption (typ. 30 μA over the full temperature range), low dropout, low output noise and very good PSRR. The regulator incorporates several protection features such as Thermal Shutdown, Soft Start, Current Limiting and also Power Good Output signal for easy MCU interfacing.

Features

- Operating Input Voltage Range: 1.5 V to 5.5 V
- Fixed Voltage Options Available: 0.8 V to 5.2 V
- Low Quiescent Current: typ. 30 μA over Temperature
- ±2% Accuracy Over Full Load, Line and Temperature variations
- PSRR: 75 dB at 1 kHz
- Low Noise: typ. 15 μV_{RMS} from 10 Hz to 100 kHz
- Stable With Small 10 μF Ceramic Capacitor
- Soft−start to Reduce Inrush Current and Overshoots
- Thermal Shutdown and Current Limit Protection
- Power Good Signal Extends Application Range
- Available in WDFN6 2x2, DFN6 3x3, DFNW6 3x3 with Wettable Flank (pin edge plating)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Wireless Chargers and Portable Equipment
- Smart Camera and Robotic Vision Systems
- Telecommunication and Networking Systems
- Infotainment and Cluster
- Modular Platforms for Dashboard Display
- Internet Connection Sharing (ICS) Gateway Server Applications
- General Purpose Automotive

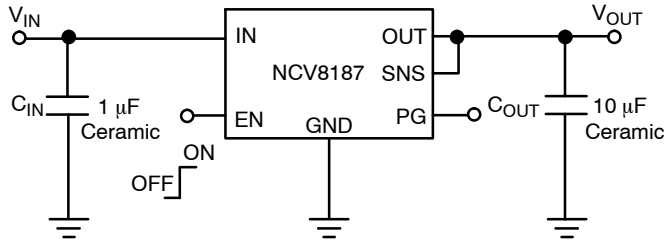


Figure 1. Typical Application Schematic

ON Semiconductor®

www.onsemi.com

WDFN6 2x2
CASE 511BR

DFN6 3x3
CASE 506DK

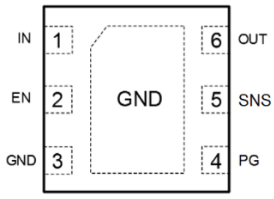
DFNW6 3x3
CASE 507AW

MARKING DIAGRAMS

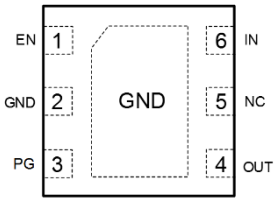
XXXXX = Specific Device Code
M = Month Code
A = Assembly Location
L = Wafet Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



WDFN6 2x2 mm
(Top View)



DFN6, DFNW6 3x3 mm
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin No. (WDFN6)	Pin No. (DFN6 3x3)	Pin Name	Description
1	6	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability
6	4	OUT	Regulated output voltage pin. A small 10 μF ceramic capacitor is needed from this pin to ground to assure stability
3, EXP	2, EXP	GND	Power supply ground
2	1	EN	Enable pin. Driving this pin high turns on the regulator. Driving EN pin low puts the regulator into shut-down mode
5	–	SNS	Sense pin. Connect this pin to regulated output voltage
4	3	PG	Power Good, open collector. Use 10 kΩ to 100 kΩ pull–up resistor connected to output or input voltage
–	5	NC	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected

ABSOLUTE MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	–0.3 to 6	V
Enable Voltage	V_{EN}	–0.3 to 6	V
Power Good Current	I_{PG}	30	mA
Power Good Voltage	V_{PG}	–0.3 to 6	V
Output Voltage	V_{OUT}	–0.3 to V_{IN} + 0.3 (max. 5.5)	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	–55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC–Q100–002 (EIA/JESD22–A114)
   ESD Machine Model tested per AEC–Q100–003 (EIA/JESD22–A115)

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6, 2x2, 0.65 Pitch Package			
Thermal Resistance, Junction–to–Ambient (Note 3)	$R_{\theta JA}$	51	°C/W
Thermal Resistance, Junction–to–Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction–to–Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.8	°C/W
Thermal Resistance, Junction–to–Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction–to–Top	Ψ_{JT}	2.0	°C/W
Characterization Parameter, Junction–to–Board	Ψ_{JB}	7.7	°C/W
Thermal Characteristics, DFN6 / DFNW6, 3x3, 0.95 Pitch Packages			
Thermal Resistance, Junction–to–Ambient (Note 3)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction–to–Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction–to–Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.9	°C/W
Thermal Resistance, Junction–to–Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction–to–Top	Ψ_{JT}	2.0	°C/W
Characterization Parameter, Junction–to–Board	Ψ_{JB}	7.5	°C/W

3. The junction–to–ambient thermal resistance under natural convection is obtained in a simulation on a high–K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51–2a.
4. The junction–to–case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30–88.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 150°C$; VIN = V_{OUT}+1.0 V; I_{OUT} = 10 mA, C_{IN} = 1 μF, C_{OUT} = 10 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 6))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.5		5.5	V
Output Voltage Accuracy	$-40°C \le T_J \le 150°C$, V_{OUT} +1 V < V_{IN} < 5.5 V, 0 mA < I_{OUT} < 1.2 A	V_{OUT} < 1.7 V	V_{OUT}	−35 mV		+35 mV	V
		$V_{OUT} \ge$ 1.7 V		−2 %		+2 %	
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		Reg_{LINE}		40		μV/V
Load Regulation	I_{OUT} = 0 mA to 1.2 A		Reg_{LOAD}		2		μV/mA
Dropout voltage	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 3\%)$ I_{OUT} = 1.2 A	1.2 V – 1.4 V	V_{DO}		325	495	mV
		1.5 V – 1.7 V			240	400	
		1.8 V – 2.7 V			200	335	
		2.8 V – 3.2 V			165	250	
		3.3 V – 4.9 V			150	220	
		5 V			120	180	
Maximum Output Current	(Note 7)		I_{OUT}	1300	1750		mA
Short Circuit Current	(Note 7)		I_{SC}		1850		mA
Disable Current	V_{EN} = 0 V		I_{DIS}		0.1	5.0	μA
Quiescent Current	I_{OUT} = 0 mA		I_Q		30	45	μA
Ground current	I_{OUT} = 1.2 A		I_{GND}		2		mA
Power Supply Rejection Ratio	V_{IN} = 3.5 V + 100 mVpp V_{OUT} = 2.5 V I_{OUT} = 10 mA, C_{OUT} = 1 μF	f = 1 kHz	PSRR		75		dB
Output Noise Voltage	VOUT = 1.8 V, IOUT = 10 mA f = 10 Hz to 100 kHz		V_N		15		μV_{rms}
Enable Input Threshold Voltage	Voltage increasing		V_{EN_HI}	0.9	–	–	V
	Voltage decreasing		V_{EN_LO}	–	–	0.3	
EN Pin Current	V_{EN} = 5.5 V				100		nA
Active Output Discharge Resistance	V_{IN} = 5.5 V, V_{EN} = 0 V		R_{DIS}		120		Ω
Power Good, Output Voltage Raising			V_{PGup}		92		%
Power Good, Output Voltage Falling			V_{PGdw}		80		%
Power Good Output Voltage Low	I_{PG} = 6 mA, Open drain		V_{PGlo}		0.14	0.4	V
Thermal Shutdown Temperature (Note 5)	Temperature increasing from T_J = +25°C		T_{SD}		170		°C
Thermal Shutdown Hysteresis (Note 5)	Temperature falling from TSD		T_{SDH}	–	15	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by design and characterization.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Respect SOA.

TYPICAL CHARACTERISTICS

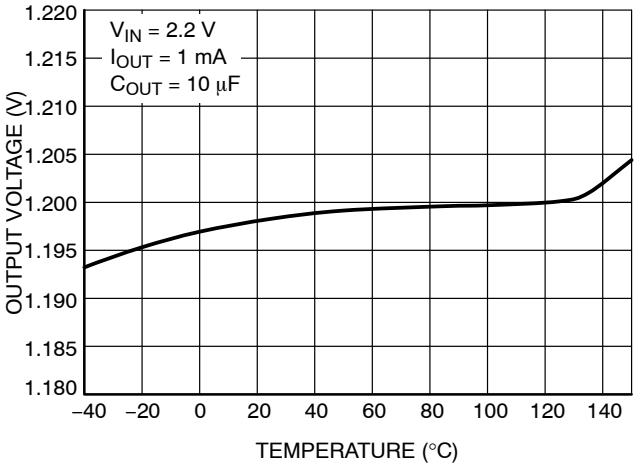


Figure 2. Output Voltage vs. Temperature – V_{OUT} = 1.2 V

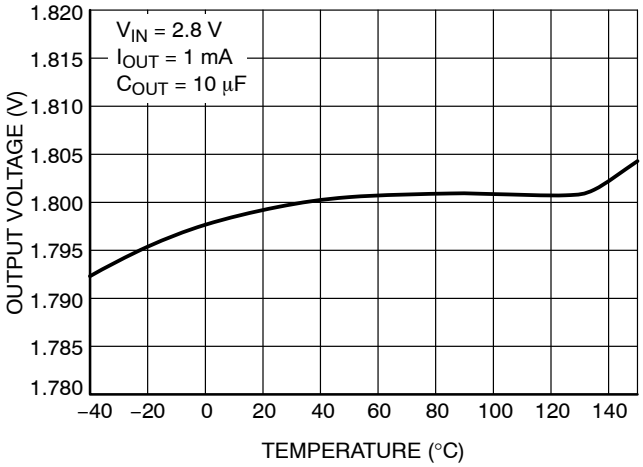


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

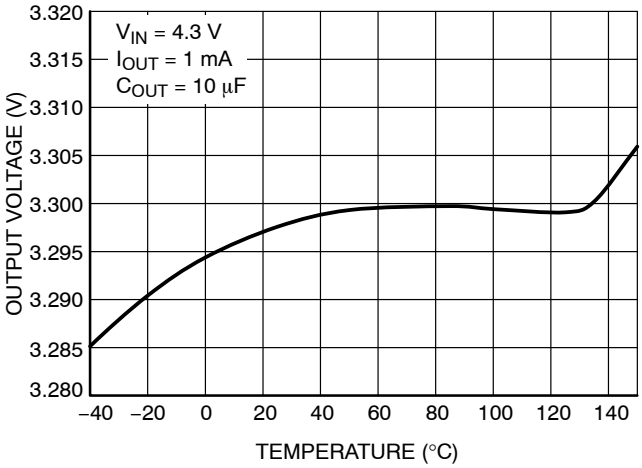


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 3.3 V

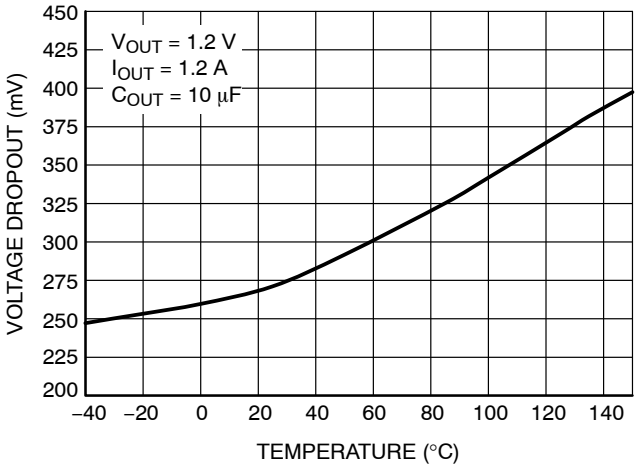


Figure 5. Dropout Voltage vs. Temperature – V_{OUT} = 1.2 V

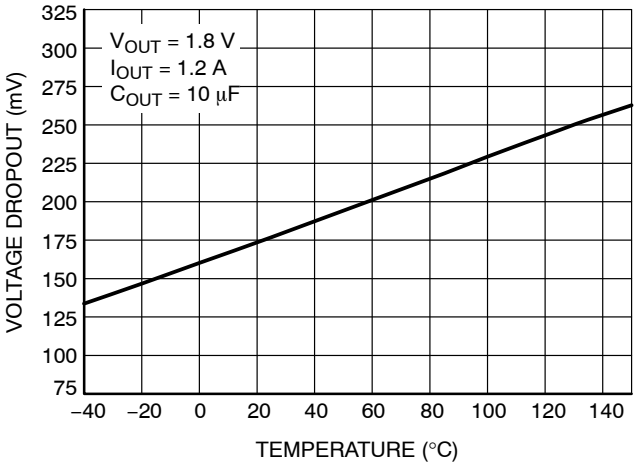


Figure 6. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

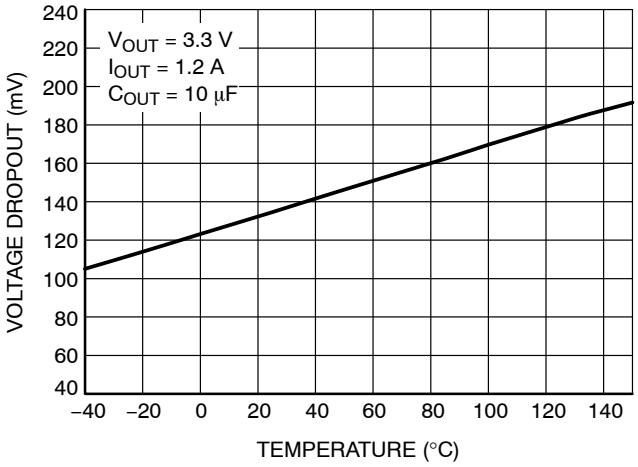


Figure 7. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

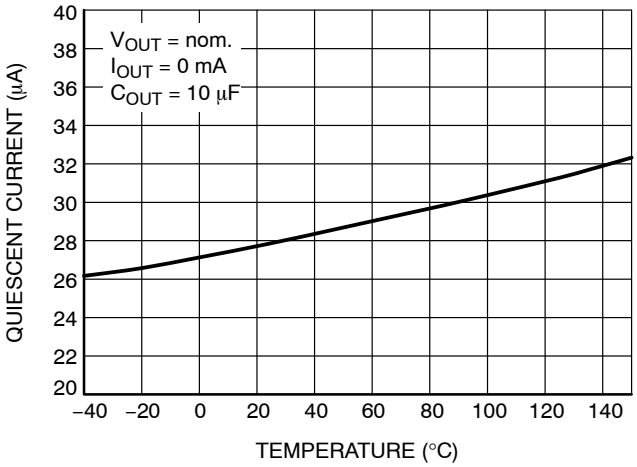


Figure 8. Quiescent Current vs. Temperature

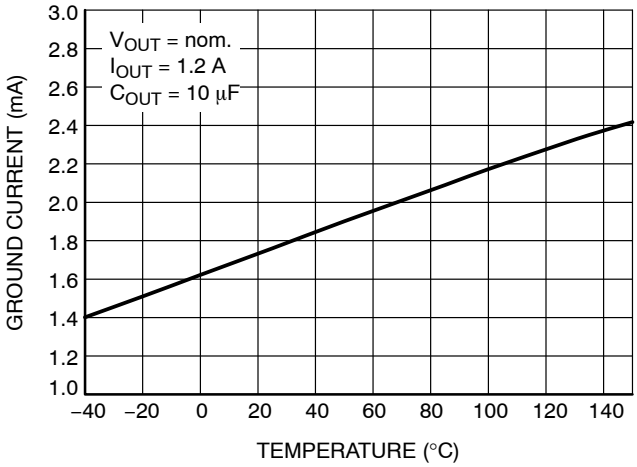


Figure 9. Ground Current vs. Temperature

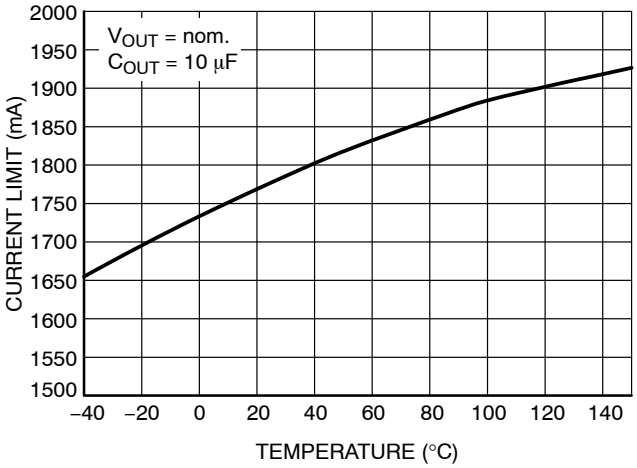


Figure 10. Current Limit vs. Temperature

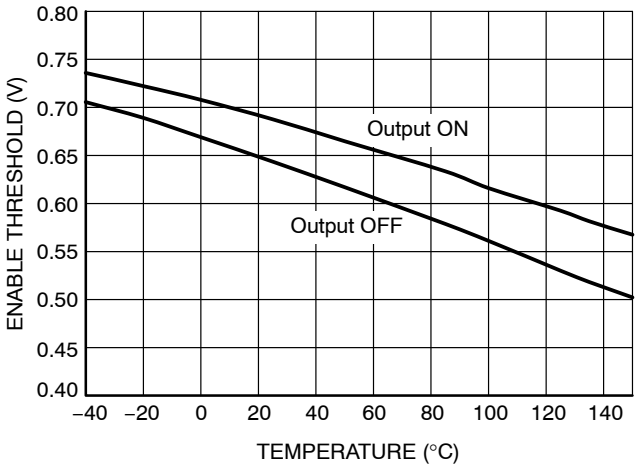


Figure 11. Enable Thresholds vs. Temperature

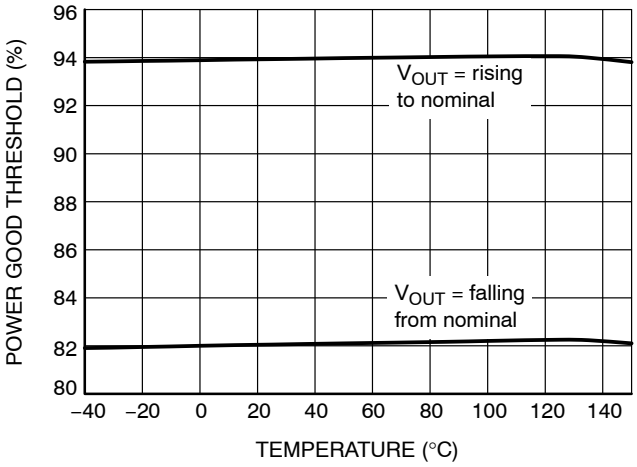


Figure 12. Power Good Thresholds vs. Temperature

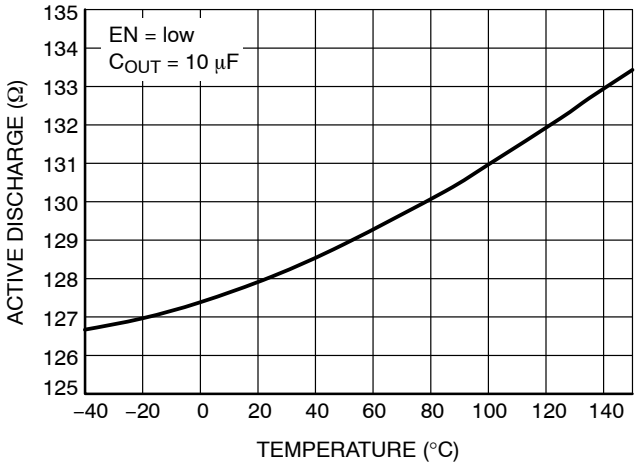


Figure 13. Active Discharge Resistance vs. Temperature

TYPICAL CHARACTERISTICS

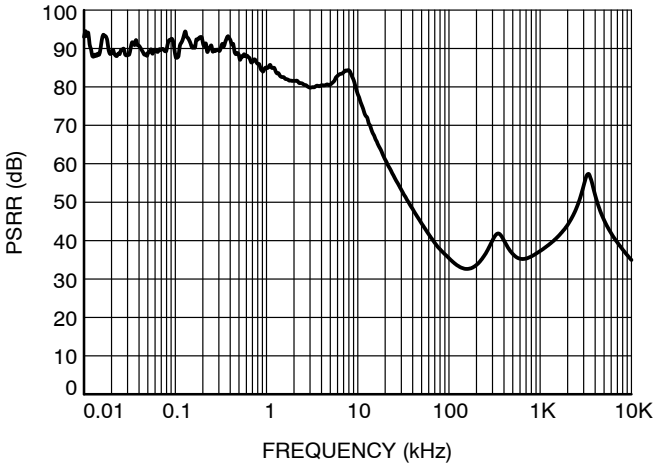


Figure 14. Power Supply Rejection Ratio for V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 10 μF

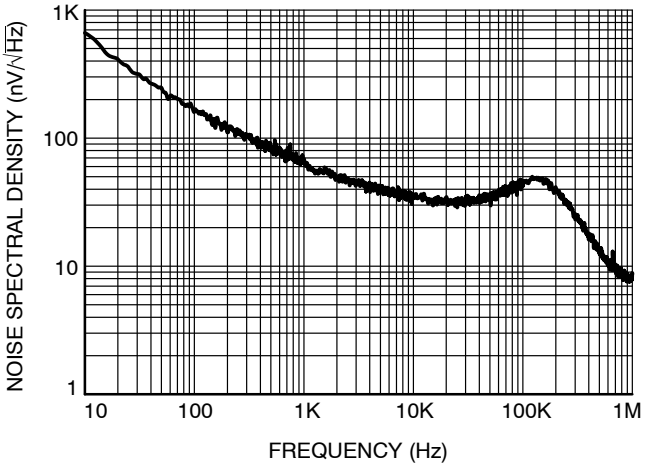


Figure 15. Output Voltage Noise Spectral Density for V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 10 μF

APPLICATIONS INFORMATION

The NCV8187 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCV8187 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft−start feature and thermal protection.

Input Decoupling (C_{IN})

It is recommended to connect at least 1 μF ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCV8187 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 4.7 μF or greater. Recommended capacitor for the best performance is 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Good Output Connection

The NCV8187 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between 10 μA and 1 mA to obtain low saturation voltage. External pull−up resistor can be connected to any voltage up to 5.5 V (please see Absolute Maximum Ratings table above).

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C. The maximum power dissipation the NCV8187 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8187 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8187, and make traces as short as possible.

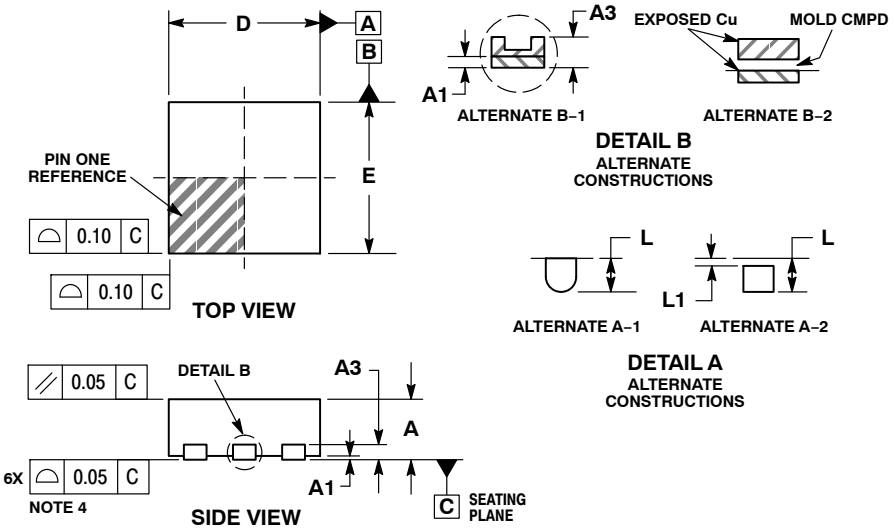
ORDERING INFORMATION

Device part no.	Voltage Option	Marking	Option	Package	Shipping†
NCV8187AMT120TAG	1.2V	PJ	With Active Output Discharge	WDFN6 2x2 non WF (Pb−Free)	3000 / Tape & Reel
NCV8187AMT180TAG	1.8V	PK	With Active Output Discharge	WDFN6 2x2 non WF (Pb−Free)	3000 / Tape & Reel
NCV8187AMT330TAG	3.3V	PL	With Active Output Discharge	WDFN6 2x2 non WF (Pb−Free)	3000 / Tape & Reel
NCV8187AMN120TAG	1.2V	NA	With Active Output Discharge	DFN6 3x3 non WF (Pb−Free)	3000 / Tape & Reel
NCV8187AMN180TAG	1.8V	NH	With Active Output Discharge	DFN6 3x3 non WF (Pb−Free)	3000 / Tape & Reel
NCV8187AML120TAG	1.2V	WD	With Active Output Discharge	DFNW6 3x3 WF SLP (Pb−Free)	3000 / Tape & Reel
NCV8187AML180TAG	1.8V	WE	With Active Output Discharge	DFNW6 3x3 WF SLP (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

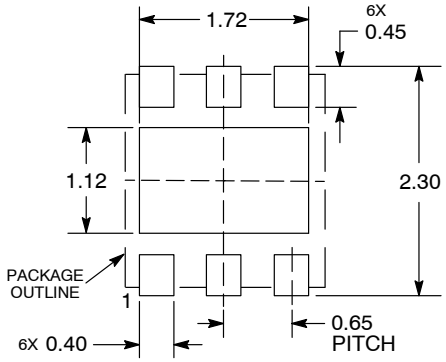
WDFN6 2x2, 0.65P
CASE 511BR
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICES CONTAINING WETTABLE FLANK OPTION, DETAIL A ALTERNATE CONSTRUCTION A–2 AND DETAIL B ALTERNATE CONSTRUCTION B–2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
L	0.20	0.40
L1	---	0.15

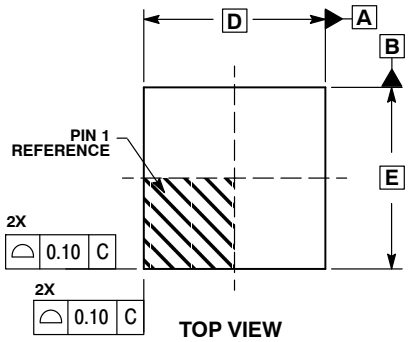
RECOMMENDED MOUNTING FOOTPRINT



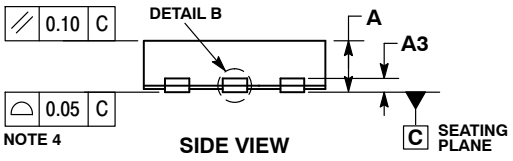
DIMENSIONS: MILLIMETERS

PACKAGE DIMENSIONS

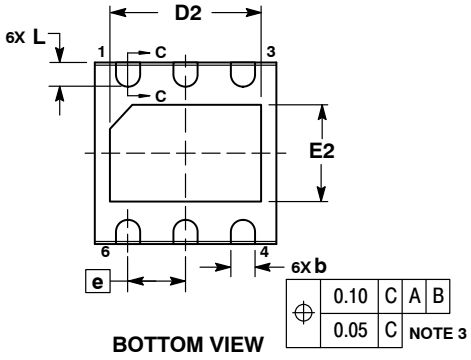
DFN6 3x3, 0.95P
CASE 506DK
ISSUE O



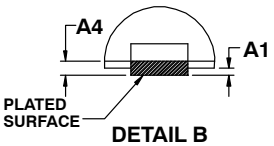
TOP VIEW



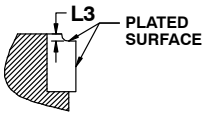
SIDE VIEW



BOTTOM VIEW



DETAIL B

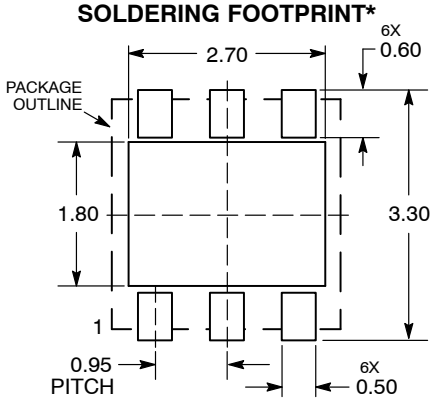


SECTION C–C

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.75	0.95
A1	0.00	0.05
A3	0.20 REF	
A4	0.05	0.15
b	0.35	0.45
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.50	1.70
e	0.95 BSC	
L	0.30	0.50
L3	0.00	0.10

RECOMMENDED SOLDERING FOOTPRINT*

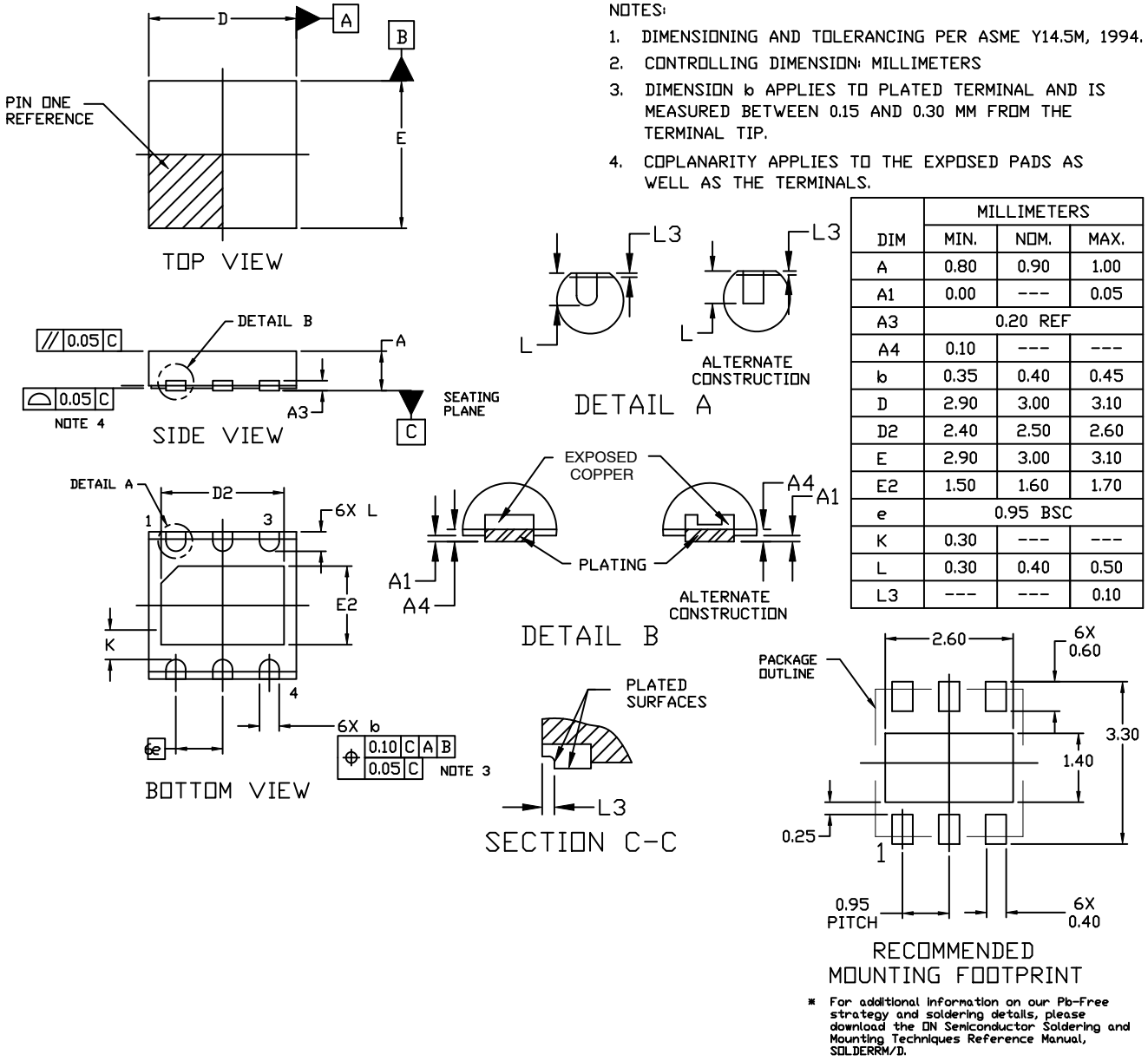


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

DFNW6 3X3, 0.95P
CASE 507AW
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.35	0.40	0.45
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
e	0.95 BSC		
K	0.30	---	---
L	0.30	0.40	0.50
L3	---	---	0.10

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