Automotive Grade Non-Synchronous Boost Controller

NCV8873

The NCV8873 is an adjustable output non−synchronous boost controller which drives an external N−channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

Protection features include internally−set soft−start, undervoltage lockout, cycle−by−cycle current limiting and thermal shutdown.

Additional features include low quiescent current sleep mode and externally−synchronizable switching frequency.

Features

- Peak Current Mode Control with Internal Slope Compensation
- 0.2 V ±3% Reference Voltage for Constant Current Loads
- Fixed Frequency Operation
- Wide Input Voltage Range of 3.2 V to 40 V, 45 V Load Dump
- Input Undervoltage Lockout (UVLO)
- Internal Soft−Start
- Low Quiescent Current in Sleep Mode
- Cycle−by−Cycle Current Limit Protection
- Thermal Shutdown (TSD)
- This is a Pb−Free Device
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

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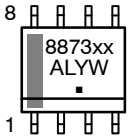
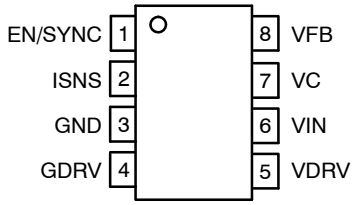
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



8873xx	= Specific Device Code xx = 00, 01 or 02
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV887300D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV887301D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV887302D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

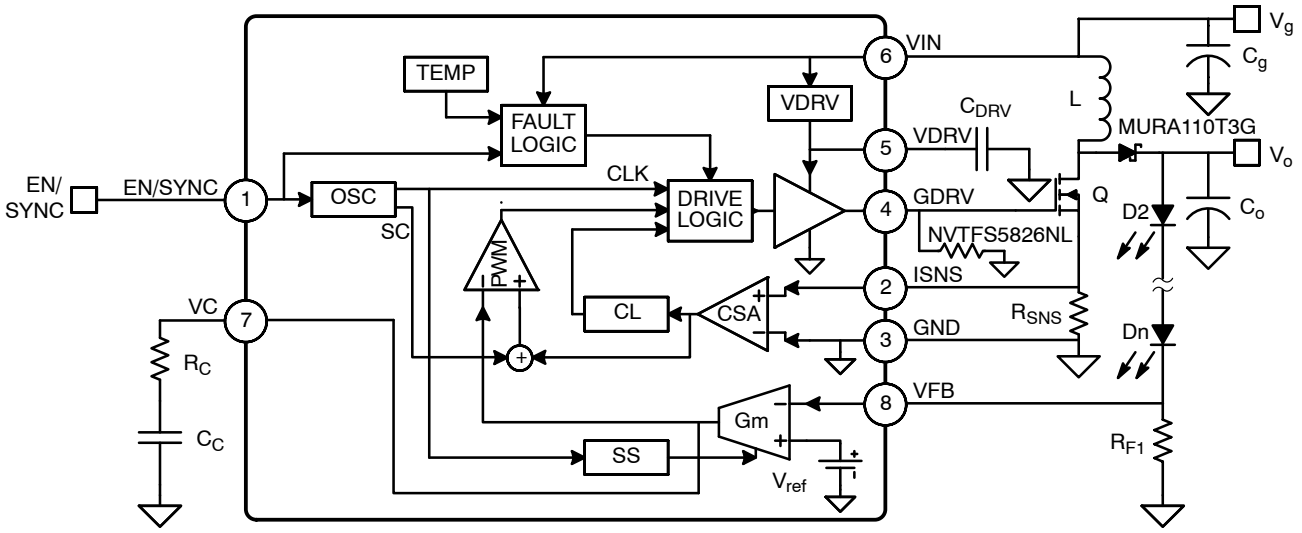


Figure 1. Simplified Block Diagram and Example Application Schematic

PACKAGE PIN DESCRIPTIONS

Pin No.	Pin Symbol	Function
1	EN/SYNC	Enable and synchronization input. The falling edge synchronizes the internal oscillator. The part is disabled into sleep mode when this pin is brought low for longer than the enable time−out period.
2	ISNS	Current sense input. Connect this pin to the source of the external N−MOSFET, through a current−sense resistor to ground to sense the switching current for regulation and current limiting.
3	GND	Ground reference.
4	GDRV	Gate driver output. Connect to gate of the external N−MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance. An R_{GND} = 15 kΩ (typical) GDRV−GND resistor is strongly recommended.
5	VDRV	Driving voltage. Internally−regulated supply for driving the external N−MOSFET, sourced from VIN. Bypass with a 1.0 μF ceramic capacitor to ground.
6	VIN	Input voltage. If bootstrapping operation is desired, connect a diode from the input supply to VIN, in addition to a diode from the output voltage to VDRV and/or VIN.
7	VC	Output of the voltage error amplifier. An external compensator network from VC to GND is used to stabilize the converter.
8	VFB	Output voltage feedback. A resistor from the output voltage to VFB with another resistor from VFB to GND creates a voltage divider for regulation and programming of the output voltage.

ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to GND, unless otherwise indicated)

Rating	Value	Unit
Dc Supply Voltage (VIN)	−0.3 to 40	V
Peak Transient Voltage (Load Dump on VIN)	45	V
Dc Supply Voltage (VDRV, GDRV)	12	V
Peak Transient Voltage (VFB)	−0.3 to 6	V
Dc Voltage (VC, VFB, ISNS)	−0.3 to 3.6	V
Dc Voltage (EN/SYNC)	−0.3 to 6	V
Dc Voltage Stress (VIN − VDRV)*	−0.7 to 40	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*An external diode from the input to the VIN pin is required if bootstrapping VDRV and VIN off of the output voltage.

PACKAGE CAPABILITIES

Characteristic		Value	Unit
ESD Capability (All Pins)	Human Body Model Machine Model	≥ 2.0 ≥ 200	KV V
Moisture Sensitivity Level		1	
Package Thermal Resistance	Junction−to−Ambient, $R_{\theta JA}$ (Note 1)	100	°C/W

1. 1 in^2, 1 oz copper area used for heatsinking.

Ordering Options

The NCV8873 features several variants to better fit a multitude of applications. The table below shows the typical values of parameters for the parts that are currently available.

TYPICAL VALUES

YY	D_{max}	f_s	t_{ss}	S_a	V_{cl}	I_{src}	I_{sink}	V_{DRV}
NCV887300	86.5%	1000 kHz	1.6 ms	130 mV/μs	400 mV	800 mA	600 mA	6.3 V
NCV887301	87.5%	400 kHz	4.0 ms	30 mV/μs	200 mV	800 mA	600 mA	6.3 V
NCV887302	92.5%	400 kHz	4.0 ms	51 mV/μs	200 mV	800 mA	600 mA	6.3 V

DEFINITIONS

Symbol	Characteristic	Symbol	Characteristic	Symbol	Characteristic
D_{max}	Maximum duty cycle	f_s	Switching frequency	t_{ss}	Soft−start time
S_a	Slope compensating ramp	V_{cl}	Current limit trip voltage	I_{src}	Gate drive sourcing current
I_{sink}	Gate drive sinking current	V_{DRV}	Drive voltage		

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN} < 40\ V$, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, T_J = 25°C	–	2.0	–	μA
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, $-40°C < T_J < 125°C$	–	2.0	6.0	μA
Quiescent Current, No switching	$I_{q,off}$	Into VIN pin, EN = 1, No switching	–	1.5	2.5	mA
Quiescent Current, Switching, normal operation	$I_{q,on}$	Into VIN pin, EN = 1, Switching	–	4.0	6.0	mA
OSCILLATOR						
Minimum pulse width	$t_{on,min}$		90	115	140	ns
Maximum duty cycle	D_{max}	YY = 00 YY = 01 YY = 02	84 85 90	86.5 87.5 92.5	89 90 95	%
Switching frequency	f_s	YY = 00 YY = 01 YY = 02	900 360 360	1000 400 400	1100 440 440	kHz
Soft−start time	t_{ss}	From start of switching with V_{FB} = 0 until reference voltage = V_{REF} YY = 00 YY = 01 YY = 02	 1.3 3.3 3.3	 1.6 4.0 4.0	 1.9 4.7 4.7	ms
Soft−start delay	$t_{ss,dly}$	From EN → 1 until start of switching with V_{FB} = 0 with floating V_C pin	–	240	280	μs
Slope compensating ramp	S_a	YY = 00 YY = 01 YY = 02	114 25 44	130 30 51	146 35 58	mV/μs
ENABLE/SYNCHRONIZATION						
EN/SYNC pull−down current	$I_{EN/SYNC}$	$V_{EN/SYNC}$ = 5 V	–	5.0	10	μA
EN/SYNC input high voltage	$V_{s,ih}$	$V_{IN} > V_{UVLO}$	2.0	–	5.0	V
EN/SYNC input low voltage	$V_{s,il}$		0	–	800	mV
EN/SYNC time−out ratio	$\%t_{en}$	From SYNC falling edge, to oscillator control (EN high) or shutdown (EN low), Percent of typical switching frequency	–	–	350	%
SYNC minimum frequency ratio	$\%f_{sync,min}$	Percent of f_s	–	–	80	%
SYNC maximum frequency	$f_{sync,max}$		1.1	–	–	MHz
Synchronization delay	$t_{s,dly}$	From SYNC falling edge to GDRV falling edge under open loop conditions.	–	50	100	ns
Synchronization duty cycle	D_{sync}		25	–	75	%
CURRENT SENSE AMPLIFIER						
Low−frequency gain	A_{csa}	Input−to−output gain at dc, ISNS ≤ 1 V	0.9	1.0	1.1	V/V
Bandwidth	BW_{csa}	Gain of A_{csa} − 3 dB	2.5	–	–	MHz
ISNS input bias current	$I_{sns,bias}$	Out of ISNS pin	–	30	50	μA
Current limit threshold voltage	V_{cl}	Voltage on ISNS pin YY = 00 YY = 01 YY = 02	 360 180 180	 400 200 200	 440 220 220	mV
Current limit, Response time	t_{cl}	CL tripped until GDRV falling edge, $V_{ISNS} = V_{cl}(typ) + 60\ mV$	–	80	125	ns
Overcurrent protection, Threshold voltage	$\%V_{ocp}$	Percent of V_{cl}	125	150	175	%

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.2 V < V_{IN} < 40 V, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER						
Overcurrent protection, Response Time	t_{ocp}	From overcurrent event, Until switching stops, V_{ISNS} = V_{OCP} + 40 mV	–	80	125	ns
VOLTAGE ERROR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER						
Transconductance	$g_{m,vea}$	V_{FB} − V_{ref} = ± 20 mV	0.8	1.2	1.63	mS
VEA output resistance	$R_{o,vea}$		2.0	–	–	MΩ
VFB input bias current	$I_{vfb,bias}$	Current out of VFB pin	–	0.5	2.0	μA
Reference voltage	V_{ref}		0.194	0.200	0.206	V
VEA maximum output voltage	$V_{c,max}$		2.5	–	–	V
VEA minimum output voltage	$V_{c,min}$		–	–	0.3	V
VEA sourcing current	$I_{src,vea}$	VEA output current, Vc = 2.0 V	80	100	–	μA
VEA sinking current	$I_{snk,vea}$	VEA output current, Vc = 0.7 V	80	100	–	μA
GATE DRIVER						
Sourcing current	I_{src}	V_{DRV} ≥ 6 V, V_{DRV} − V_{GDRV} = 2 V YY = 00 YY = 01 YY = 02	 600 600 600	 800 800 800	 – – –	mA
Sinking current	I_{sink}	V_{GDRV} ≥ 2 V YY = 00 YY = 01 YY = 02	 500 500 500	 600 600 600	 – – –	mA
Driving voltage dropout	$V_{drv,do}$	V_{IN} − V_{DRV}, Iv_{DRV} = 25 mA	–	0.3	0.6	V
Driving voltage source current	I_{drv}	V_{IN} − V_{DRV} = 1 V	35	45	–	mA
Backdrive diode voltage drop	$V_{d,bd}$	V_{DRV} − V_{IN}, $I_{d,bd}$ = 5 mA	–	–	0.7	V
Driving voltage	V_{DRV}	I_{VDRV} = 0.1 − 25 mA YY = 00 YY = 01 YY = 02	 6.0 6.0 6.0	 6.3 6.3 6.3	 6.6 6.6 6.6	V
UVLO						
Undervoltage lock−out, Threshold voltage	V_{uvlo}	V_{IN} falling	2.95	3.05	3.15	V
Undervoltage lock−out, Hysteresis	$V_{uvlo,hys}$	V_{IN} rising	50	150	250	mV
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_{sd}	T_J rising	160	170	180	°C
Thermal shutdown hysteresis	$T_{sd,hys}$	T_J falling	10	15	20	°C
Thermal shutdown delay	$t_{sd,dly}$	From T_J > T_{sd} to stop switching	–	–	100	ns

TYPICAL PERFORMANCE CHARACTERISTICS

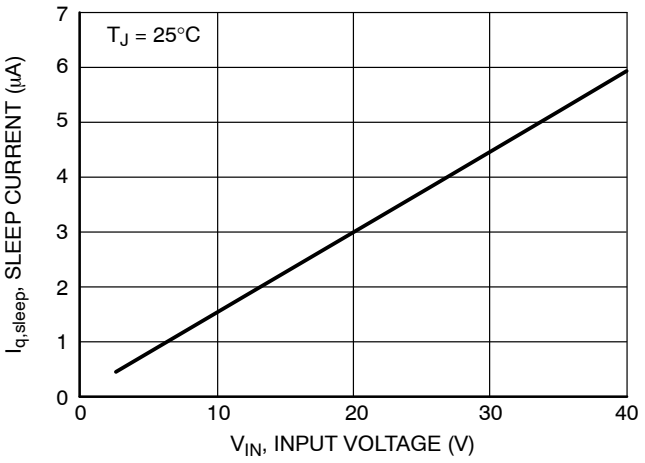


Figure 2. Sleep Current vs. Input Voltage

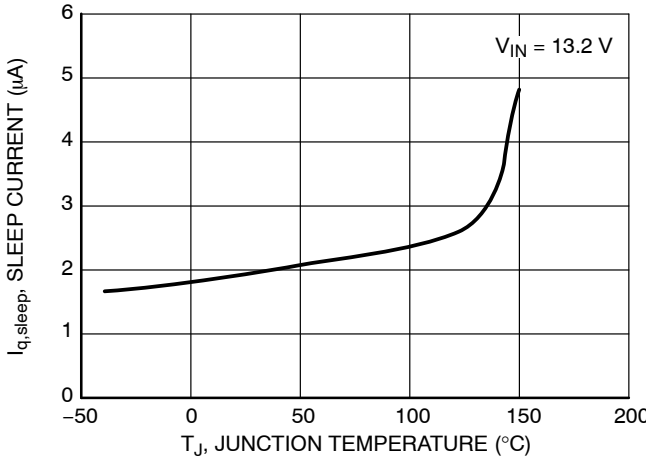


Figure 3. Sleep Current vs. Temperature

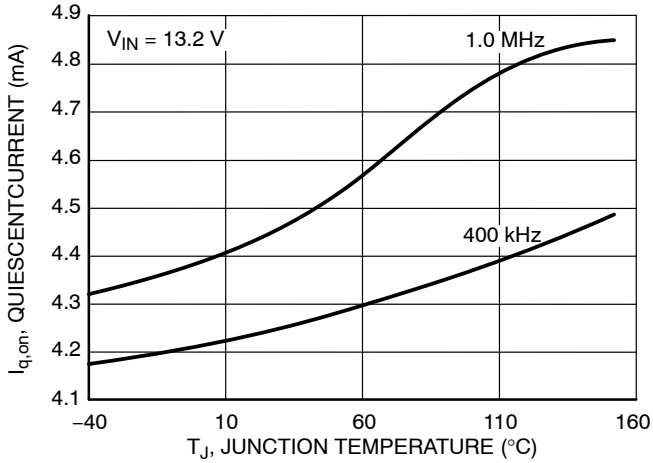


Figure 4. Quiescent Current vs. Temperature

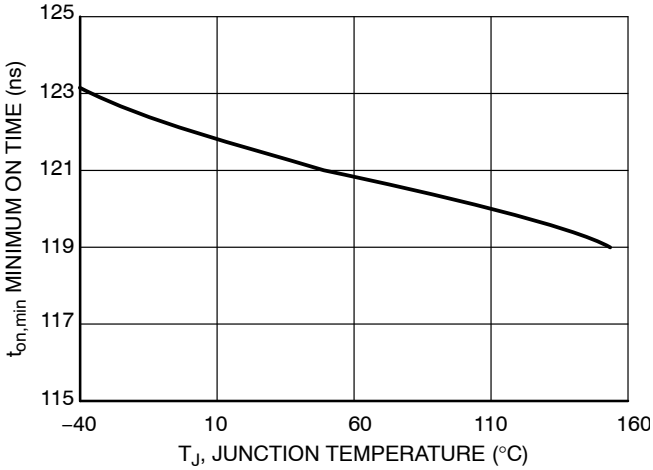


Figure 5. Minimum On Time vs. Temperature

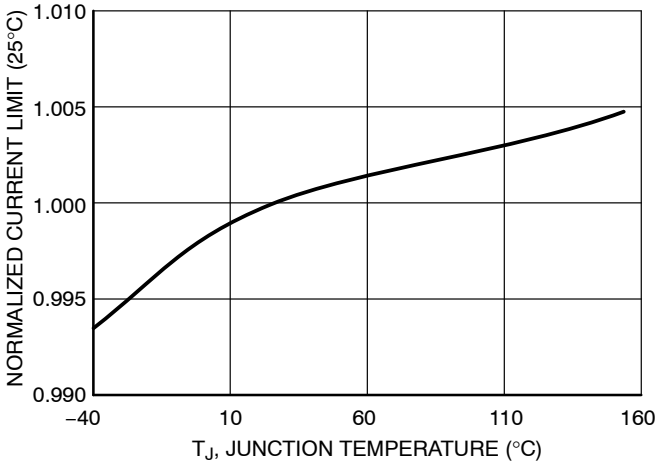


Figure 6. Normalized Current Limit vs. Temperature

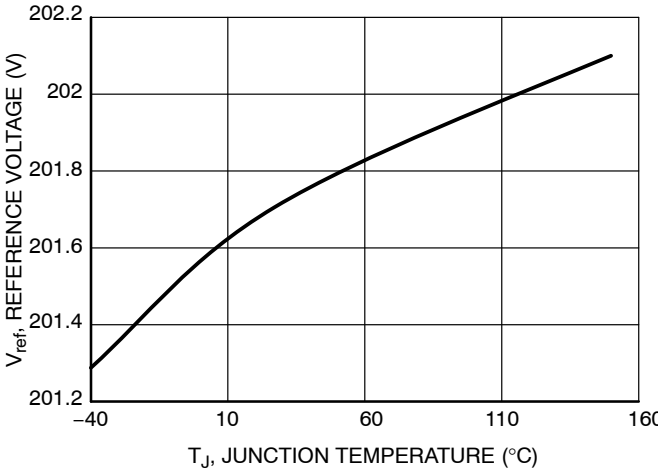


Figure 7. Reference Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

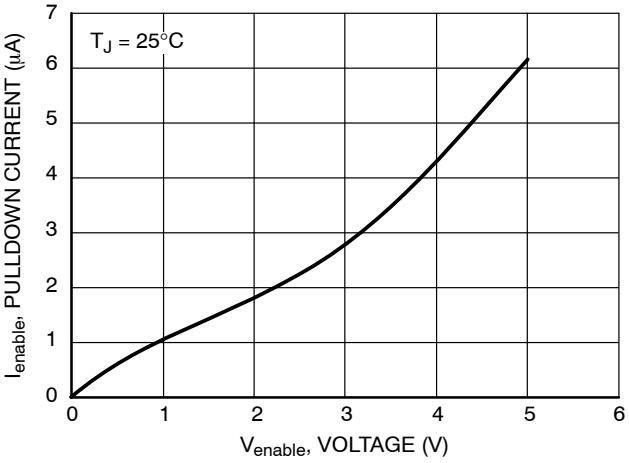


Figure 8. Enable Pulldown Current vs. Voltage

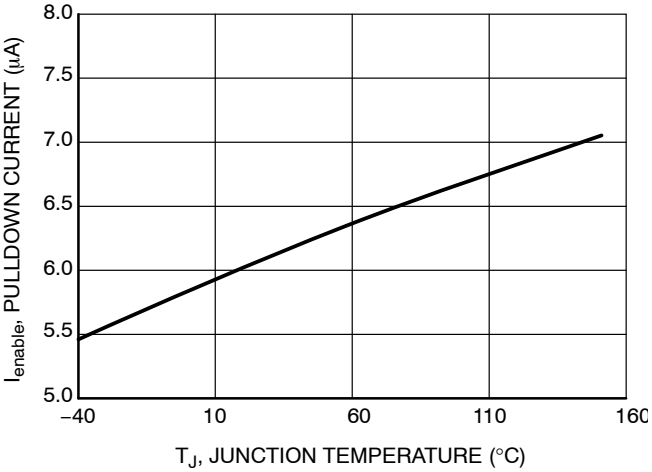


Figure 9. Enable Pulldown Current vs. Temperature

THEORY OF OPERATION

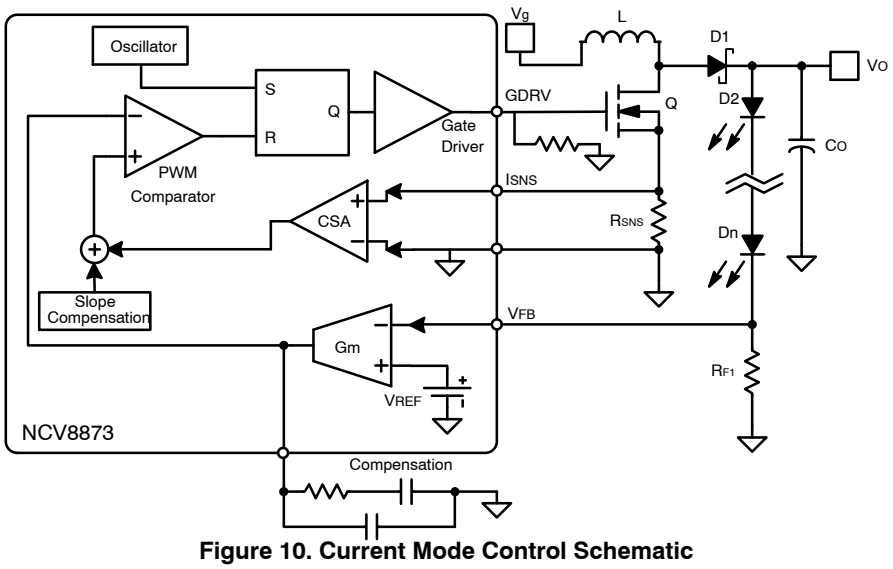


Figure 10. Current Mode Control Schematic

Current Mode Control

The NCV8873 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV8873 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Current Limit

The NCV8873 features a peak current−mode current limit protection. When the current sense amplifier detects a voltage above the peak current limit between ISNS and GND after the current limit leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from ISNS to GND, with $R = V_{CL} / I_{limit}$.

If the voltage across the current sense resistor exceeds the over current threshold voltage the part enters soft−start mode.

EN/SYNC

This pin has three modes. When a dc logic high (CMOS/TTL compatible) voltage is applied to this pin the NCV8873 operates at the programmed frequency. When a dc logic low voltage is applied to this pin the NCV8873 enters a low quiescent current sleep mode. When a square wave of at least $\%f_{sync,min}$ of the free running switching frequency is applied to this pin, the switcher operates at the same frequency as the square wave. If the signal is slower than this, it will be interpreted as enabling and disabling the part. The falling edge of the square wave corresponds to the start of the switching cycle. If an Enable command is received during normal operation, the minimum duration of the Enable low−state must be greater than 7 clock cycles.

If the VIN pin voltage falls below V_{UVLO} when EN/SYNC pin is at logic−high, the IC may not power up when VIN returns back above the UVLO. To resume a normal operating state, the EN/SYNC pin must be cycled with a single logic−low to logic−high transition.

UVLO

Input Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VIN is too low to support the internal rails and power the controller. The IC will start up when enabled and VIN surpasses the UVLO threshold plus the UVLO hysteresis and will shut down when VIN drops below the UVLO threshold or the part is disabled.

To avoid any lock state under UVLO conditions, the EN/SYNC pin should be in logic−low state. For further details, please refer to EN/SYNC paragraph.

Internal Soft−Start

To insure moderate inrush current and reduce output overshoot, the NCV8873 features a soft start which charges a capacitor with a fixed current to ramp up the reference voltage.

This fixed current is based on the switching frequency, so that if the NCV8873 is synchronized to twice the default switching frequency the soft start will last half as long.

GDRV

An R_{GND} = 15 kΩ (typical) GDRV−GND resistor is strongly recommended.

APPLICATION INFORMATION

Design Methodology

This section details an overview of the component selection process for the NCV8873 in discontinuous conduction mode (DCM) Boost converter operation with a high brightness LED (100−150 mA typical) string as a load. LED current is used for the feedback signal. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select Output Inductor
4. Select Output Capacitors
5. Select Input Capacitors
6. Select Feedback Resistors
7. Select Compensator Components
8. Select MOSFET(s)
9. Select Diode

1. Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
I_{LED}: LED current [A]
I_{CL}: desired typical cycle-by-cycle current limit [A]
V_{ref}: NCV8873 feedback reference voltage = 0.2 V
I_L: inductor current [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$M_{min} = \frac{V_{out}}{V_{in(max)}}$$

$$M_{max} = \frac{V_{out}}{V_{in(min)}}$$

$$R_{out} = \frac{V_{out}}{I_{LED}}$$

$$D_{min} = \sqrt{\frac{Lf_s}{2R_{out}}\left[(2M_{min} - 1)^2 - 1\right]}$$

$$D_{max} = \sqrt{\frac{Lf_s}{2R_{out}}\left[(2M_{max} - 1)^2 - 1\right]}$$

$$\delta = \frac{2V_{out}{}^2}{V_{in}R_{out}I_{L,peak}} - D\,,$$

Where: (D + δ) < 1 for DCM operation IL.

Both duty cycles will actually be slightly higher due to power loss in the conversion. The exact duty cycles depend on conduction and switching losses. If the maximum input voltage is higher than the output voltage, the minimum duty cycle will be a complex value. This is because a Boost converter cannot have an output voltage lower than the input voltage. In situations where the input voltage is higher than the output, the output will follow the input (minus the diode drop of the Boost diode) and the converter will not attempt to switch.

If the inductor value is too large, continuous conduction mode (CCM) operation will occur and a right-half-plane (RHP) zero appears which can result in operation instability.

If the calculated D_{max} is higher than the D_{max} of the NCV8873, the conversion will not be possible. It is important for a Boost converter to have a restricted D_{max}, because while the ideal conversion ration of a Boost converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to maintain output regulation.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

2. Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. The easiest method of generating this signal is to use a current sense resistor between the MOSFET source and ground. The sense resistor should be selected as follows:

$$R_{SNS} = \frac{V_{CL}}{I_{CL}}$$

Where: R_{SNS}: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desired current limit [A]

3. Select the Boost Inductor

The Boost inductor controls the current ripple that occurs over a switching period. A discontinuous current ripple will result in superior transient response and lower switching noise at the expense of higher transistor conduction losses and operating ripple current requirements. A low current ripple will result in CCM operation having a slower response current slew rate in case of load steps (e.g. introducing an

LED series dimming circuit). A good starting point is to select components for DCM operation at $V_{in(min)}$, but operation should be verified empirically. Calculate the maximum inductor value as follows:

$$L_{max} = \frac{\left(1 - \frac{1}{M_{max}}\right) V_{in(min)}{}^2 \left(\frac{V_{out}}{I_{LED}}\right)}{2 f_s V_{out}{}^2}$$

The maximum average inductor current can be calculated as follows:

$$I_{L,avg} = \frac{V_{OUT} I_{OUT(max)}}{V_{IN(min)}}$$

The peak inductor current can be calculated as follows:

$$I_{L,peak} = \frac{V_{IN(min)} D_{max}}{L f_s}$$

Where: $I_{L,peak}$: Peak inductor current value [A]

4. Select Output Capacitor

The output capacitor smoothes the output voltage and reduces the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{I_{LED}(1 - \delta\,(M_{max}))}{f_s C_{OUT}}$$

The capacitors must withstand an RMS ripple current as follows:

$$I_{Cout(RMS)} = \sqrt{I_{LED}{}^2 + \delta(M_{max})\left(\frac{I_{L,pk}{}^2}{3} - I_{L,pk} I_{LED}\right)}$$

A 2.2 μF ceramic capacitor is usually sufficient for high brightness LED applications for f_s = 1 MHz.

5. Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \sqrt{\left(\frac{D(M_{max}) + \delta\,(M_{max})}{3}\right) I_{L,pk}{}^2 - I_{L,avg}{}^2}$$

6. Select Feedback Resistors

The feedback resistor provides LED current sensing for the feedback signal. It may be calculated as follows:

$$R_{F1} = \frac{V_{ref}}{I_{LED}}$$

7. Select Compensator Components

Current Mode control method employed by the NCV8873 allows the use of a simple Type II compensation to optimize the dynamic response according to system requirements. A transconductance amplifier is used, so compensation components must be connected between the compensation pin and ground.

8. Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out, the selected MOSFET must not violate the following inequality:

$$Q_{g(total)} \le \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

The maximum RMS Current can be calculated as follows:

$$I_{Q(max)} = I_{L,peak} \sqrt{\frac{D(M_{max})}{3}}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltage:

$$V_{Q(max)} = V_{OUT(max)}$$

9. Select Diode

The output diode rectifies the output current. The average current through diode will be equal to the output current:

$$I_{D(avg)} = I_{OUT(max)}$$

Additionally, the diode must block voltage equal to the higher of the output voltage or the maximum input voltage:

$$V_{D(max)} = V_{OUT}$$

The maximum power dissipation in the diode can be calculated as follows:

$$P_D = V_{f(max)} I_{OUT(max)}$$

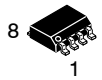
Where: P_d: Power dissipation in the diode [W]
$V_{f(max)}$: Maximum forward voltage of the diode [V]

Low Voltage Operation

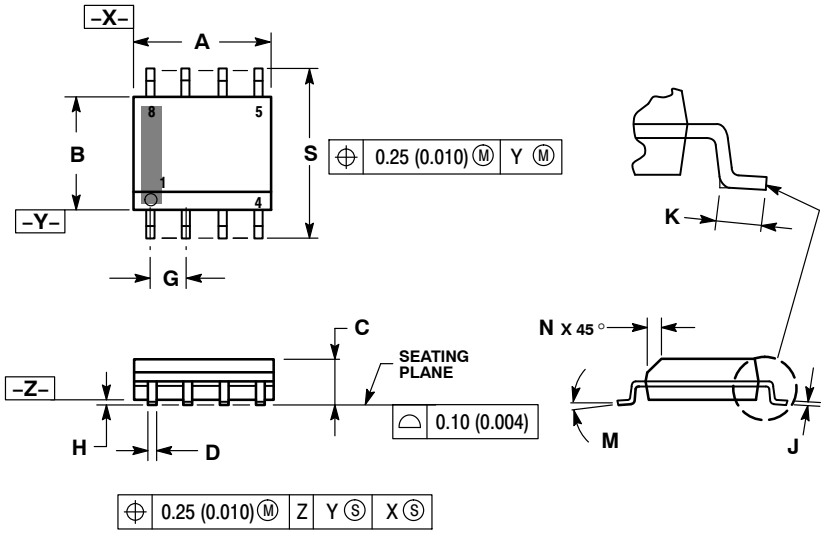
If the input voltage drops below the UVLO or MOSFET threshold voltage, another voltage may be used to power the device. Simply connect the voltage you would like to boost to the inductor and connect the stable voltage to the VIN pin of the device. In Boost configuration, the output of the converter can be used to power the device. In some cases it may be desirable to connect 2 sources to VIN pin, which can be accomplished simply by connecting each of the sources through a diode to the VIN pin.

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011



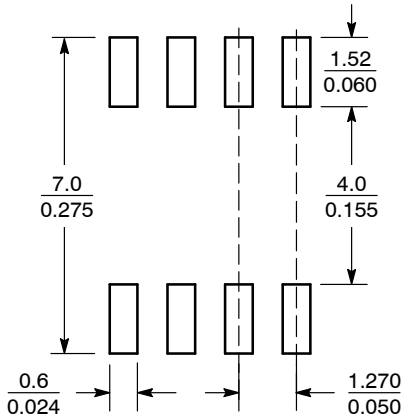
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

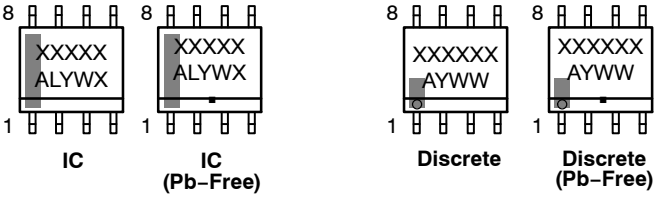
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

STYLES ON PAGE 2

SOIC−8 NB
CASE 751−07
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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

ISSUE	REVISION	DATE
AB	ADDED STYLE 25. REQ. BY S. CHANG.	15 MAR 2004
AC	ADDED CORRECTED MARKING DIAGRAMS. REQ. BY S. FARRETTA.	13 AUG 2004
AD	CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY S. FARRETTA.	18 NOV 2004
AE	UPDATED SCALE ON FOOTPRINT. REQ. BY S. WEST.	31 JAN 2005
AF	UPDATED MARKING DIAGRAMS. REQ. BY S. WEST. ADDED STYLE 26. REQ. BY S. CHANG.	14 APR 2005
AG	ADDED STYLE 27. REQ. BY S. CHANG.	30 JUN 2005
AH	ADDED STYLE 28. REQ. BY S. CHANG.	09 MAR 2006
AJ	ADDED STYLE 29. REQ. BY D. HELZER.	19 SEP 2007
AK	ADDED STYLE 30. REQ. BY I. CAMBALIZA.	16 FEB 2011

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