

NDDL1N60Z, NDTL1N60Z

Product Preview

N-Channel Power MOSFET 600 V, 15 Ω

Features

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | NDD | NDT | Unit |
|---|-----------------------------------|-------------|------|------|
| Drain-to-Source Voltage | V _{DSS} | 600 | | V |
| Continuous Drain Current R _{θJC} Steady State, T _C = 25°C (Note 1) | I _D | 0.8 | 0.3 | A |
| Continuous Drain Current R _{θJC} Steady State, T _C = 100°C (Note 1) | I _D | 0.5 | 0.15 | A |
| Pulsed Drain Current, t _p = 10 μs | I _{DM} | 3.2 | 1.0 | A |
| Power Dissipation – R _{θJC} Steady State, T _C = 25°C | P _D | 25 | 3 | W |
| Gate-to-Source Voltage | V _{GS} | ±30 | | V |
| Single Pulse Drain-to-Source Avalanche Energy (I _{PK} = 1.0 A) | EAS | 60 | | mJ |
| Peak Diode Recovery (Note 2) | dv/dt | 4.5 | | V/ns |
| Source Current (Body Diode) | I _S | 0.5 | 0.3 | A |
| Lead Temperature for Soldering Leads | T _L | 260 | | °C |
| Operating Junction and Storage Temperature | T _J , T _{STG} | -55 to +150 | | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Limited by maximum junction temperature
2. I_S = 1.5 A, di/dt ≤ 100 A/μs, V_{DD} ≤ BV_{DSS}

THERMAL RESISTANCE

| Parameter | Symbol | Value | Unit |
|--|------------------|-------|------|
| Junction-to-Case (Drain) NDDL1N60Z | R _{θJC} | 5 | °C/W |
| Junction-to-Ambient (Note 4) NDDL1N60Z (Note 3) NDDL1N60Z-1 (Note 4) NDTL1N60Z (Note 5) NDTL1N60Z | R _{θJA} | 50 | °C/W |
| | | 96 | |
| | | 62 | |
| | | 151 | |

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

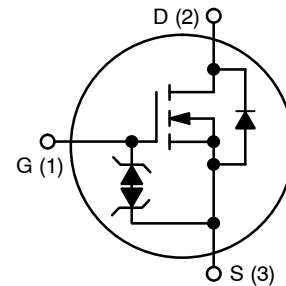


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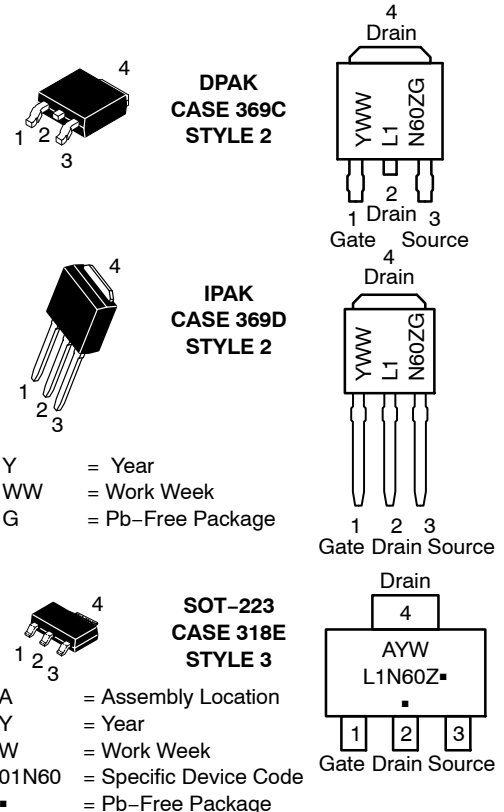
<http://onsemi.com>

| V _{(BR)DSS} | R _{DS(ON)} MAX |
|----------------------|-------------------------|
| 600 V | 15 Ω @ 10 V |

N-Channel MOSFET



MARKING DIAGRAMS



(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------|--------|-----------------|-----|-----|-----|------|
|----------------|--------|-----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|--|---------------------------|-----|-----------|----------------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ | 600 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | Reference to $25^\circ\text{C}, I_D = 1\text{ mA}$ | | 660 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source Leakage Current | I_{DSS} | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 1 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 50 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS (Note 6)

| | | | | | | |
|--|------------------|--|---|------|-----|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS} = V_{GS}, I_D = 50\ \mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | 7.0 | | mV/ $^\circ\text{C}$ |
| Static Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 0.2\text{ A}$ | | 13 | 15 | Ω |
| Forward Transconductance | g_{FS} | $V_{DS} = 15\text{ V}, I_D = 0.2\text{ A}$ | | 0.5 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCES

| | | | | | | |
|---------------------------------------|-----------|---|--|-----|--|----------|
| Input Capacitance (Note 7) | C_{iss} | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 94 | | pF |
| Output Capacitance (Note 7) | C_{oss} | | | 18 | | |
| Reverse Transfer Capacitance (Note 7) | C_{rss} | | | 3 | | |
| Total Gate Charge (Note 7) | Q_g | $V_{DS} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}$ | | 5 | | nC |
| Gate-to-Source Charge (Note 7) | Q_{gs} | | | 1 | | |
| Gate-to-Drain Charge (Note 7) | Q_{gd} | | | 3 | | |
| Plateau Voltage | V_{GP} | | | 6 | | |
| Gate Resistance | R_g | | | TBD | | Ω |

SWITCHING CHARACTERISTICS (Note 8)

| | | | | | | |
|---------------------|--------------|--|--|----|--|----|
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 0\ \Omega$ | | 6 | | ns |
| Rise Time | t_r | | | 5 | | |
| Turn-off Delay Time | $t_{d(off)}$ | | | 13 | | |
| Fall Time | t_f | | | 25 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|---|---------------------------|--|-----|-----|----|
| Diode Forward Voltage | V_{SD} | $I_S = 0.4\text{ A}, V_{GS} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 0.8 | 1.6 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.6 | | |
| Reverse Recovery Time | t_{rr} | $V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}, I_S = 0.8\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$ | | | 140 | | ns |
| Charge Time | t_a | | | | 25 | | |
| Discharge Time | t_b | | | | 115 | | |
| Reverse Recovery Charge | Q_{rr} | | | | 220 | | |

6. Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

7. Guaranteed by design.

8. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

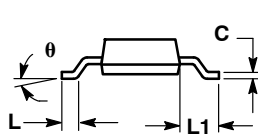
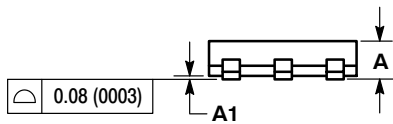
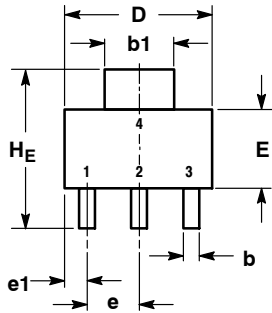
| Device | Package | Shipping [†] |
|--------------|------------------------------------|-----------------------|
| NDDL1N60Z-1G | IPAK (Pb-Free, Halogen-Free) | 75 Units / Rail |
| NDDL1N60ZT4G | DPAK (Pb-Free, Halogen-Free) | 2500 / Tape & Reel |
| NDTL1N60ZT1G | SOT-223 (Pb-Free, Halogen-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N



NOTES:

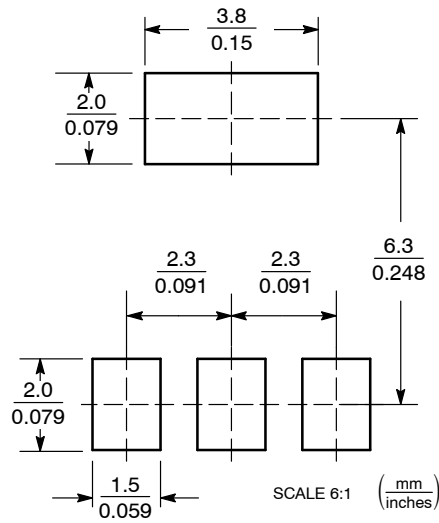
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|--------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.50 | 1.63 | 1.75 | 0.060 | 0.064 | 0.068 |
| A1 | 0.02 | 0.06 | 0.10 | 0.001 | 0.002 | 0.004 |
| b | 0.60 | 0.75 | 0.89 | 0.024 | 0.030 | 0.035 |
| b1 | 2.90 | 3.06 | 3.20 | 0.115 | 0.121 | 0.126 |
| c | 0.24 | 0.29 | 0.35 | 0.009 | 0.012 | 0.014 |
| D | 6.30 | 6.50 | 6.70 | 0.249 | 0.256 | 0.263 |
| E | 3.30 | 3.50 | 3.70 | 0.130 | 0.138 | 0.145 |
| e | 2.20 | 2.30 | 2.40 | 0.087 | 0.091 | 0.094 |
| e1 | 0.85 | 0.94 | 1.05 | 0.033 | 0.037 | 0.041 |
| L | 0.20 | --- | --- | 0.008 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 | 0.060 | 0.069 | 0.078 |
| HE | 6.70 | 7.00 | 7.30 | 0.264 | 0.276 | 0.287 |
| θ | 0° | --- | 10° | 0° | --- | 10° |

STYLE 3:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

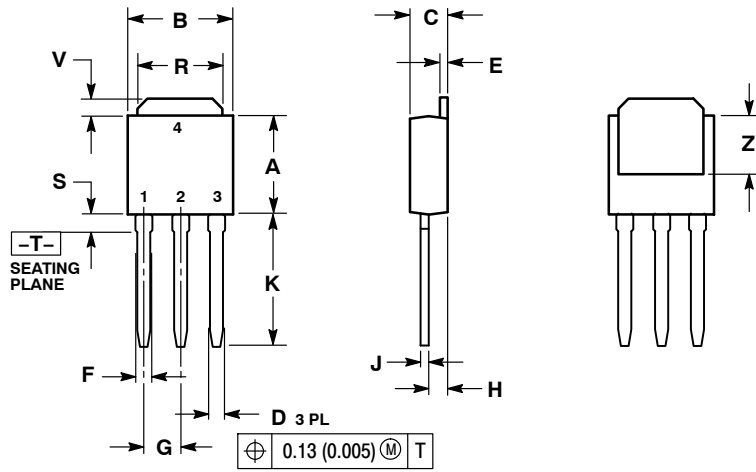
SOLDERING FOOTPRINT



NDDL1N60Z, NDTL1N60Z

PACKAGE DIMENSIONS

IPAK
CASE 369D
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

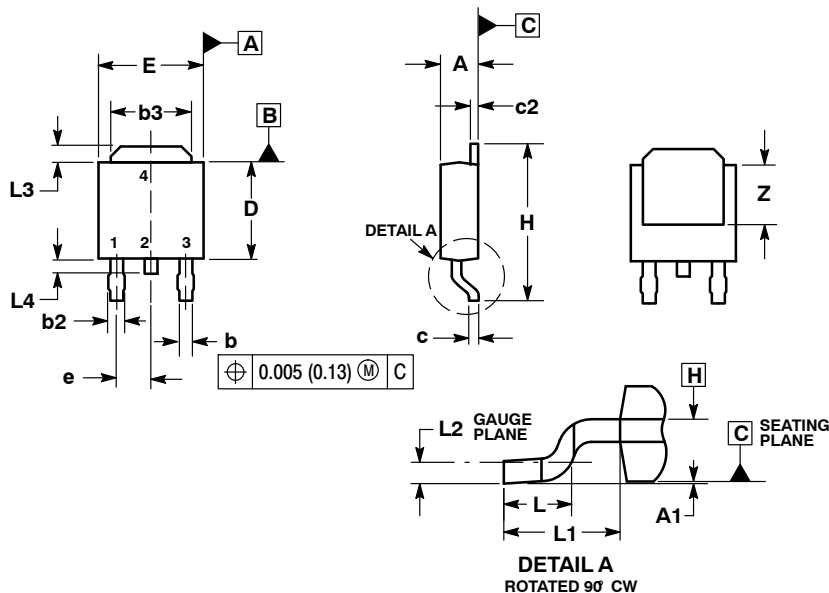
NDDL1N60Z, NDTL1N60Z

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)

CASE 369C-01

ISSUE D



NOTES:

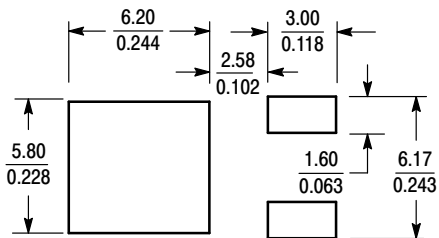
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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