NIMD6001AN

Dual N-Channel Driver with Diagnostic Output 60 V, 3 A, 110 mΩ

NIMD6001AN is a dual 3 Amp low-side switch with an integrated common disable input and drain diagnostic output. Pulling the Disable pin low will override any applied gate voltages and turn off both FET switches. Should either Drain-Source voltage exceed approximately 50 V, a logic 1 (> 3 V) will be asserted on the Diagnostic/Feedback pin. Internal isolation diodes permit the Disable and Diagnostic/ Feedback pins of multiple devices to be interconnected in a "wired-OR" configuration without additional components.

Features

- R_{DSON} 110 mΩ Maximum at V_{GS} = 10 V
- Avalanche Energy Specified
- Gate Drive Disable Input
- Drain-Source Voltage Diagnostic Feedback Output
- Electrically Isolated Drains for Low Crosstalk
- Internal Resistors Limit Peak Transient gate Current
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Injector Driver
- Solenoid / Relay Driver

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage (DC, sustained)	V_{DSS}	60	Vdc
Gate−to−Source Voltage	V_{GS}	±20	Vdc
Continuous Drain Current V_{GS} = 10 V, $R_{\theta JA}$ = 55°C/W V_{GS} = 5.0 V, $R_{\theta JA}$ = 55°C/W	I_D	 3.3 3.0	A
Single Pulse Drain Current Pulse duration = 80 μs	I_D	10	A
Single Pulse Drain-to-Source Avalanche Energy V_{DD} = 60 V; V_{GS} = 10 V; I_{PK} = 2.6 A; L = 76 mH; Start Tj = 25°C	E_{AS}	258	mJ
Operating Junction Temperature	T_J	−55 − 150	°C
Storage Temperature	T_{STG}	−55 − 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ON Semiconductor®

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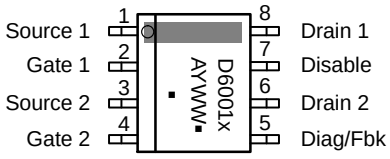
3.0 AMPERES
60 VOLTS
$R_{DS(on)}$ = 110 mΩ

SOIC−8
CASE 751

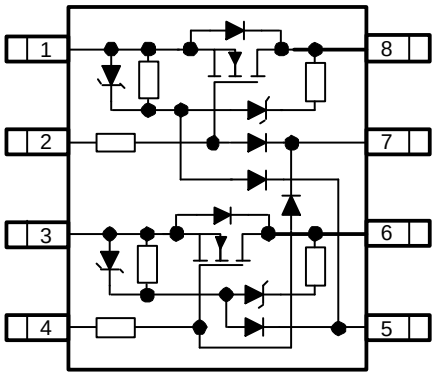
MARKING DIAGRAM



(Top View)

D6001x = Specific Device Code
x = N or A
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



INTERNAL DIAGRAM

ORDERING INFORMATION

Device	Package	Shipping†
NIMD6001ANR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN DESCRIPTIONS

Pin #	Symbol	Description
1	S1	FET 1 Source and Body
2	G1	FET 1 Gate
3	S2	FET 2 Source and Body
4	G2	FET 2 Gate
5	Diag/Fbk	Diagnostic Feedback − This pin will be logic high when either FET Drain-Source voltage exceeds the Drain Diagnostic threshold.
6	D2	FET 2 Drain
7	Disable	Gate Disable − Pull this pin low to disable both FETs. A logic low will override voltage applied to G1 or G2.
8	D1	FET 1 Drain

THERMAL RESISTANCE

Parameter	Symbol	Value	Units
Junction-to-Ambient − min. pad footprint (Notes 1 and 2)	$R_{\theta JA}$	96	°C/W
Junction-to-Ambient − 1″ Cu pad (Notes 1 and 3)	$R_{\theta JA}$	75	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V; I_D = 5 mA	60	67		V
Zero Gate Voltage Drain Current (Note 1)	I_{DSS}	V_{GS} = 0 V; V_{DS} = 15 V V_{GS} = 0 V; V_{DS} = 15 V; T_A = 150°C		10 80	20 250	μA
Gate Input Current	I_{GSS}	V_{GS} = ±20 V; V_{DS} = 0 V	−100	±25	+100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}; I_D = 250 μA	1.0	1.7	3.0	
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 10 V; I_D = 3.3 A		60	110	mΩ
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 5 V; I_D = 3.0 A		72	130	mΩ
DYNAMIC CHARACTERISTICS (Note 1)						
Input Capacitance	C_{ISS}	V_{GS} = 0 V; V_{DS} = 15 V; f = 75 kHz		150	175	pF
Output Capacitance	C_{OSS}			150	170	
Reverse Transfer Capacitance	C_{RSS}			25	30	
Gate Resistance	R_G			8	15	kΩ
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 V to 5 V; V_{DD} = 30 V; I_D = 3.3 A; I_G = 1.0 mA,		8.3	9.0	nC
Gate-to-Source Gate Charge	Q_{gs}			1.1	1.6	
Gate-to-Drain Miller Charge	Q_{gd}			4.2	5	

1. These values are established by statistical characterization and may not be tested.
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 40 sq. mm; 1 oz.)
3. Surface-mounted on FR4 board using 1 sq. inch heat spreader (Cu area = 625 sq. mm, 2 oz.)
4. Refer to Figure 1 for definition of switching characteristics symbols.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Notes 1 and 4)						
Turn-On Time	T(on)	V_{GS} = 10 V; V_{DD} = 30 V; I_D = 3.3 A, Ext. R_{GS} = 47 Ω		6.0	8.0	μs
Turn-On Delay	Td(on)			1.7		
Rise Time	Tr			3.9		
Turn-Off Time	T(off)			24	28	
Turn-Off Delay	Td(off)			15		
Fall Time	Tf			9.0		
BODY DIODE						
Source-Drain Forward On Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 3.3 A		0.85	1.25	V
DIAGNOSTIC FEEDBACK (Note 1)						
Feedback voltage	V_{FBK}	V_{DS} = 35 V, $R_{FBK-SOURCE}$ = 51 kΩ			1.7	V
Feedback Logical High voltage	$V_{FBK(HI)}$	V_{DS} = 60 V, $R_{FBK-SOURCE}$ = 51 kΩ	3.0		5.5	V
V_{DS} threshold voltage for logical High	$V_{DSFBK(HI)}$	Ramp V_{DS} positive until V_{FBK} = 3.5 V	45		65	V
V_{DS} threshold voltage for logical Low	$V_{DSFBK(LOW)}$	Ramp V_{DS} negative until V_{FBK} = 0.8 V	25		45	V
DISABLE (Note 1)						
Gate Drive Disable Input Voltage, Gate Enable	$V_{DIS(HI)}$	V_{DIS} ≥ 3.0 V, V_{GS} = 5 V, I_D = 3.0 A	3			V
Gate Drive Disable Input Voltage, Gate Disable	$V_{DIS(LOW)}$	V_{DIS} ≤ 0.4 V, V_{GS} = V_{DS} = 10 V, I_D ≤ 250 μA; Tj = 150°C (Note 1)			0.4	V

1. These values are established by statistical characterization and may not be tested.
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 40 sq. mm; 1 oz.)
3. Surface-mounted on FR4 board using 1 sq. inch heat spreader (Cu area = 625 sq. mm, 2 oz.)
4. Refer to Figure 1 for definition of switching characteristics symbols.

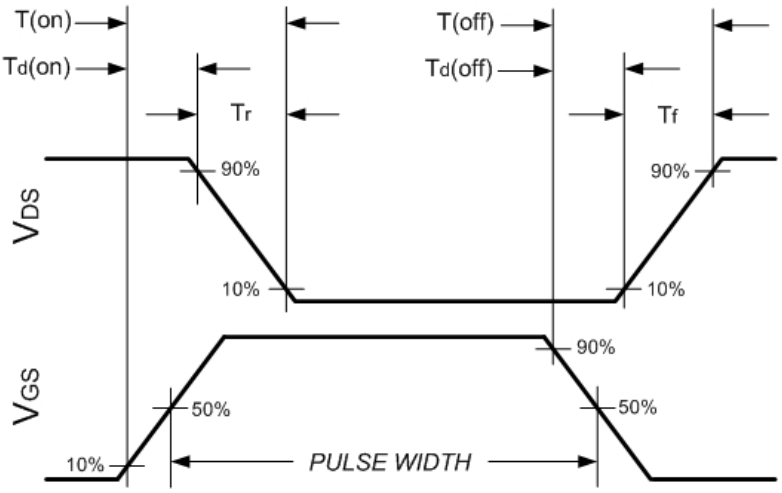


Figure 1. Switching Characteristics Waveforms and Symbols

TYPICAL ELECTRICAL CHARACTERISTICS

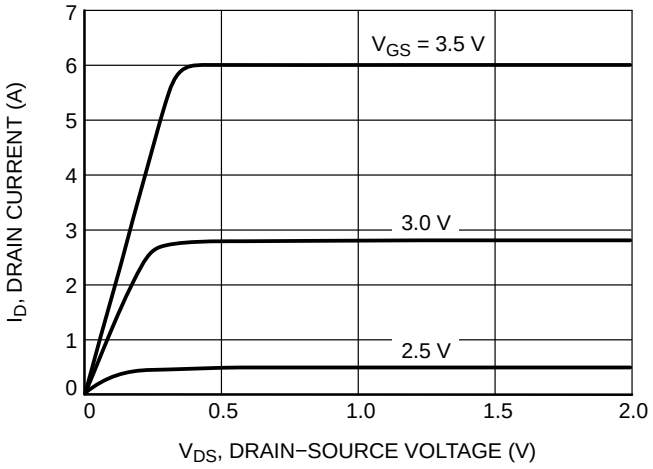


Figure 2. Drain Current vs. Drain−Source Voltage and Gate−Source Voltage

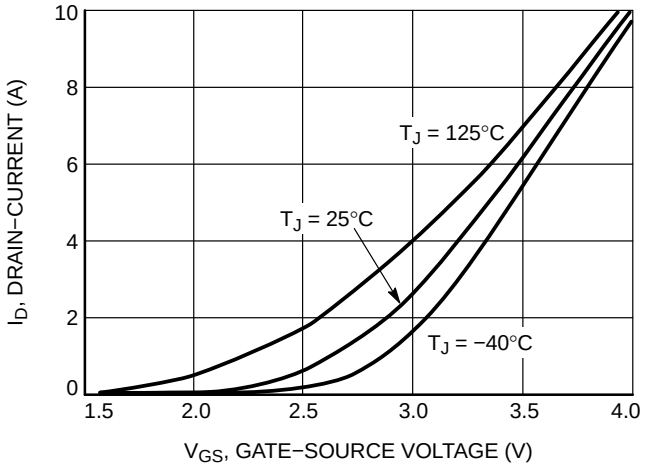


Figure 3. Transfer Function (pulsed). Pulse duration = 80 μs, duty cycle < 0.5%; V_{DS} = 2 V

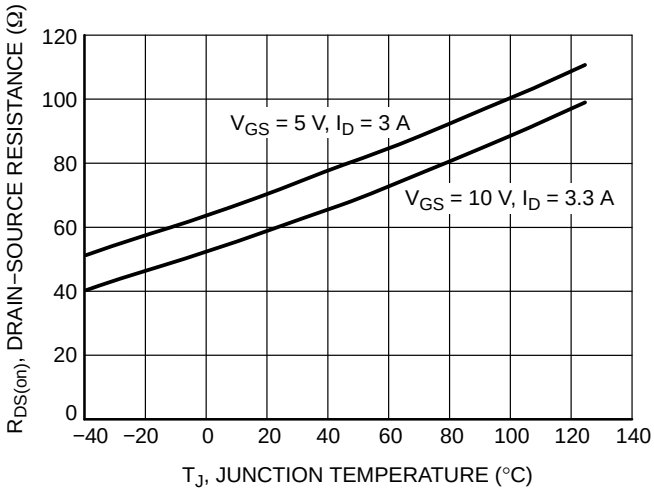


Figure 4. Drain−Source On Resistance vs. Junction Temperature

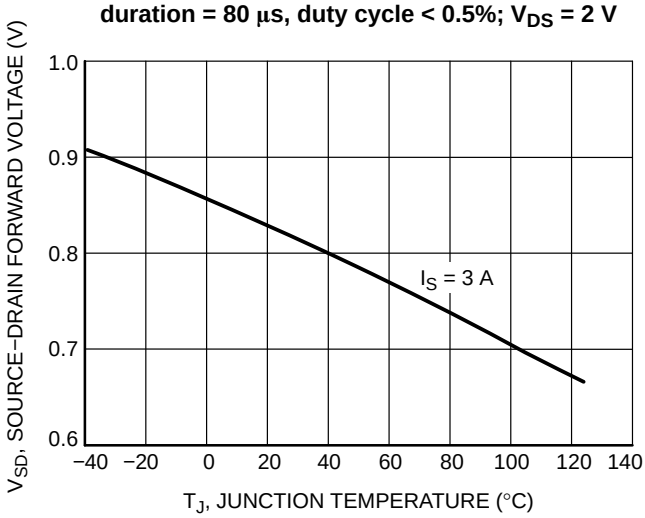


Figure 5. Body Diode Forward Voltage vs. Junction Temperature

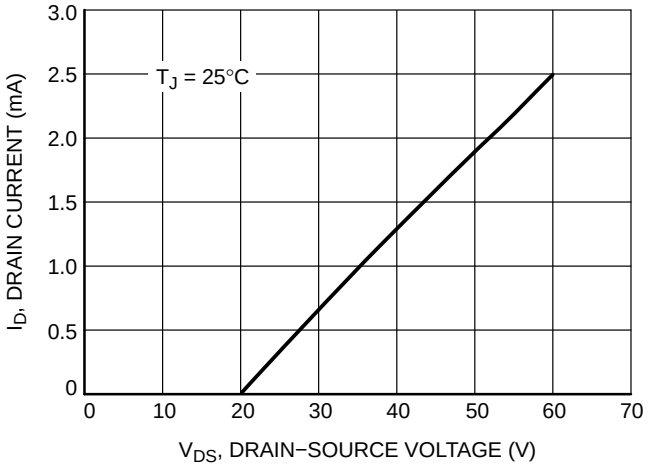


Figure 6. Off−State Drain Current vs. Drain−Source Voltage (includes feedback network current)

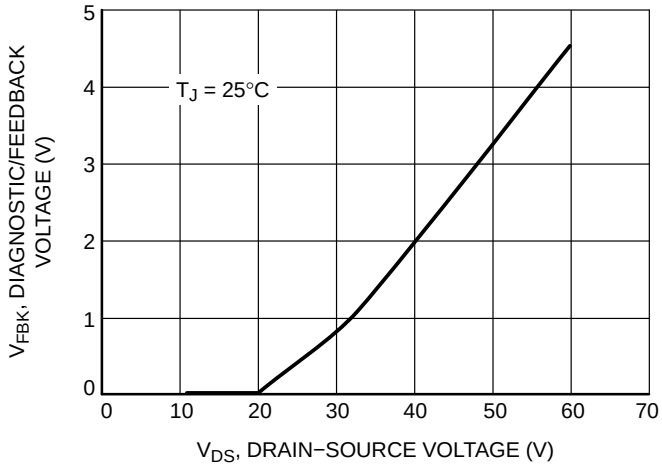


Figure 7. Diagnostic Feedback Voltage vs. Drain−Source Voltage

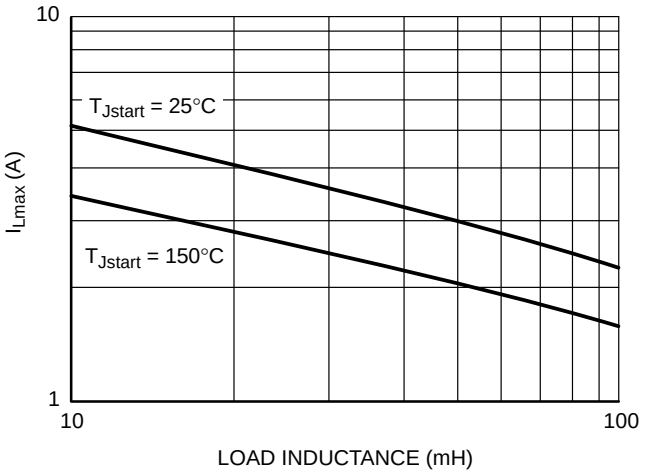


Figure 8. Single Pulse Maximum Switch−off Current vs. Load Inductance

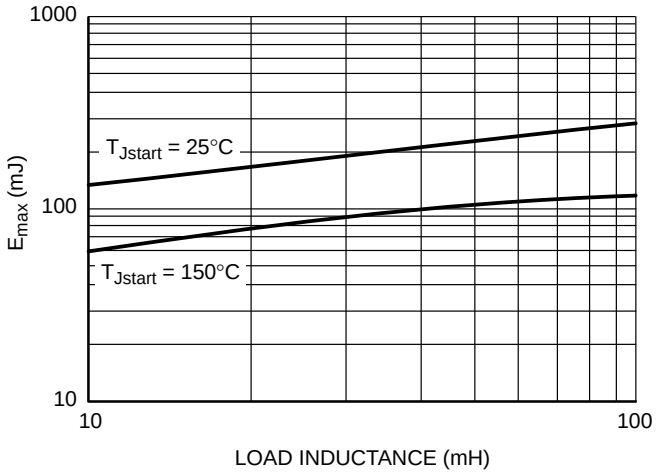


Figure 9. Single Pulse Maximum Switching Energy vs. Load Inductance

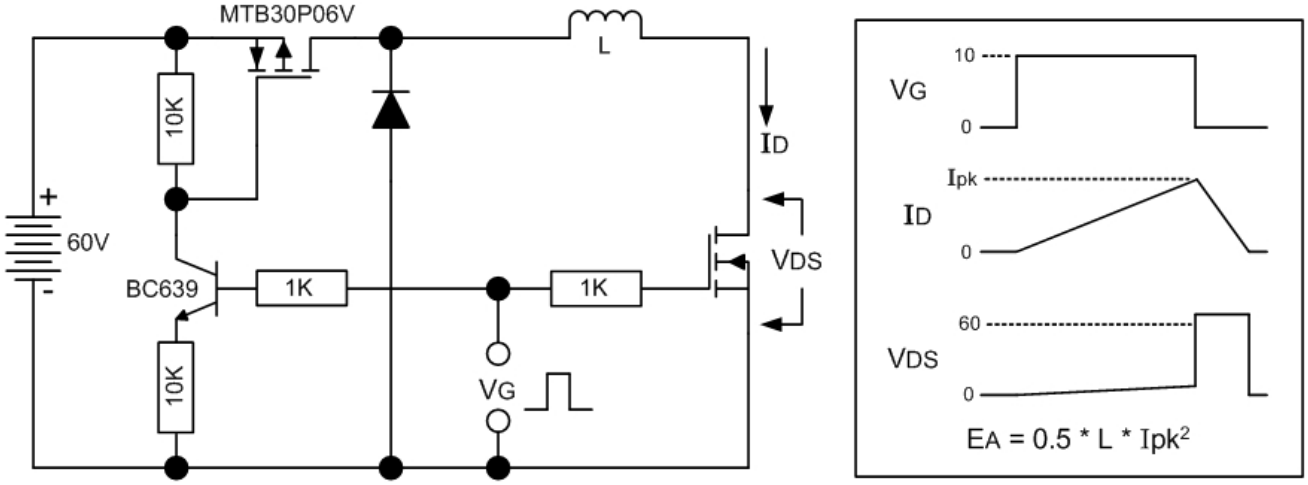


Figure 10. Single Pulse Peak Drain Current and Avalanche Energy Test Circuit

TYPICAL THERMAL RESPONSE CHARACTERISTICS

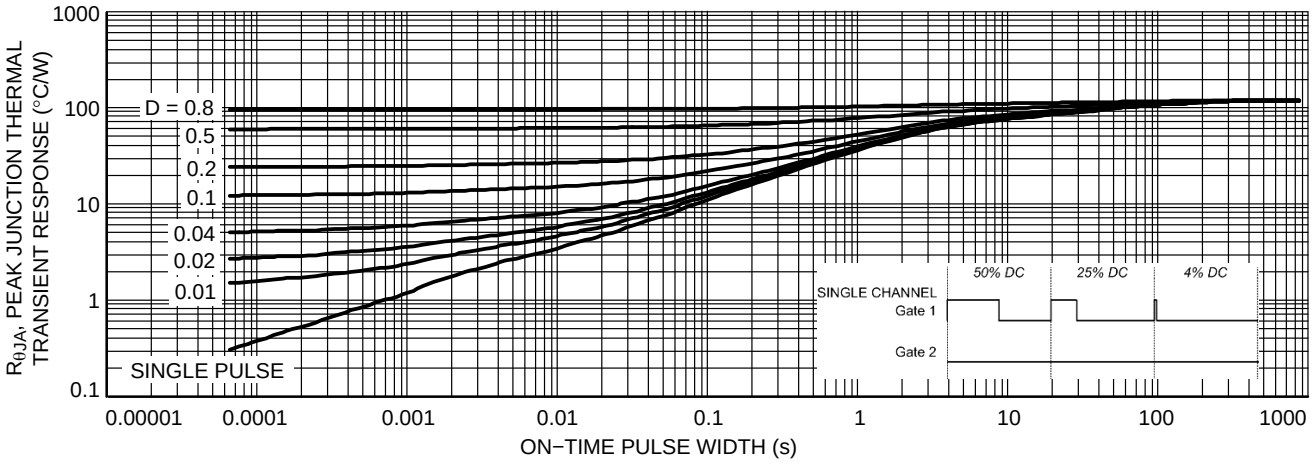


Figure 11. Single Channel Active; Mounted on Minimum−Pad Board

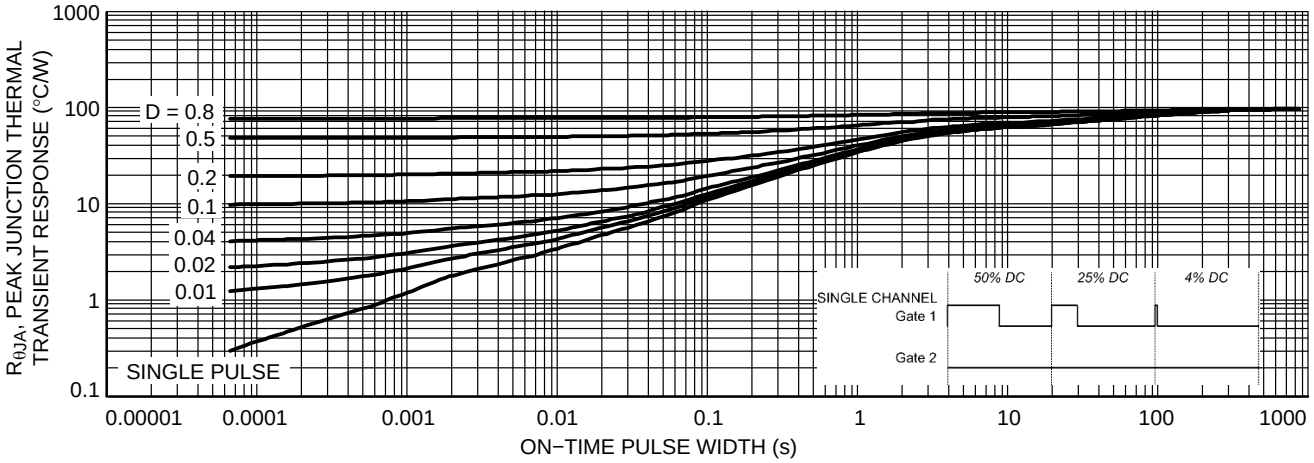


Figure 12. Single Channel Active; Mounted on 1 Sq. Inch Copper Spreader

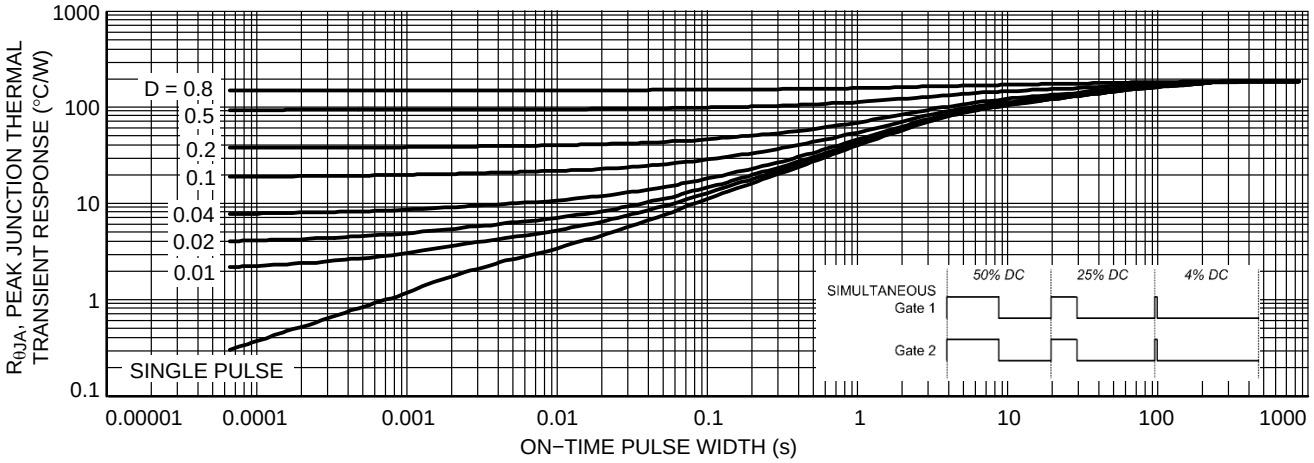


Figure 13. Both Channels Active; Mounted on Minimum−Pad Board

TYPICAL THERMAL RESPONSE CHARACTERISTICS

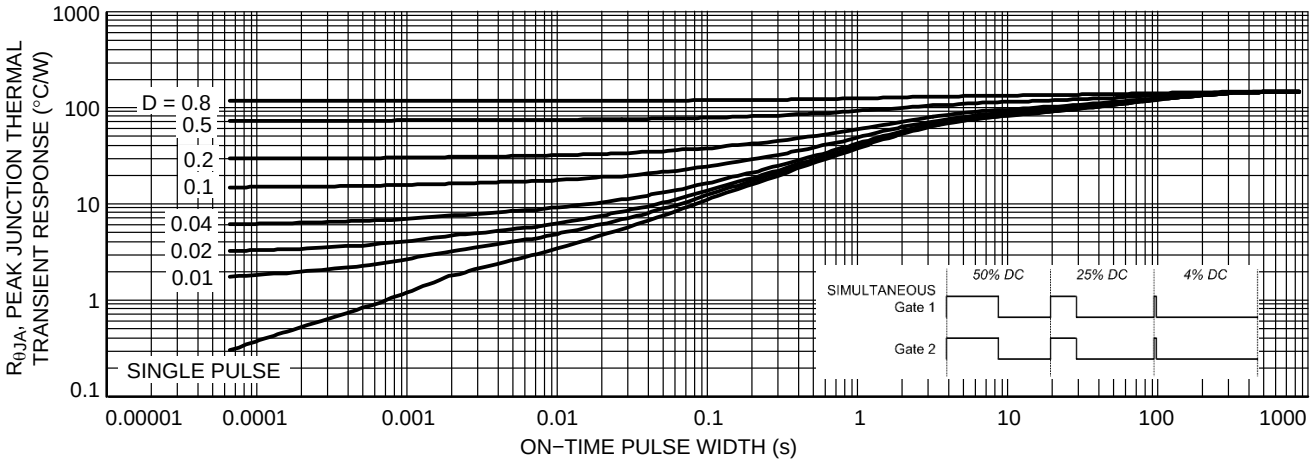


Figure 14. Both Channels Active; Mounted on 1 Sq. Inch Copper Spreader

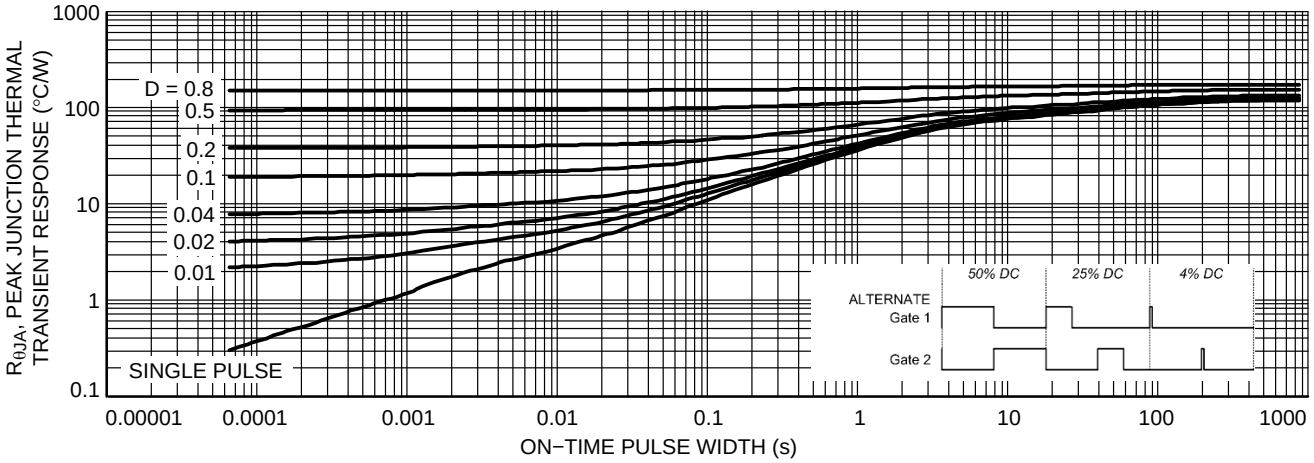


Figure 15. Channels Alternatively Active; Mounted on Minimum−Pad Board

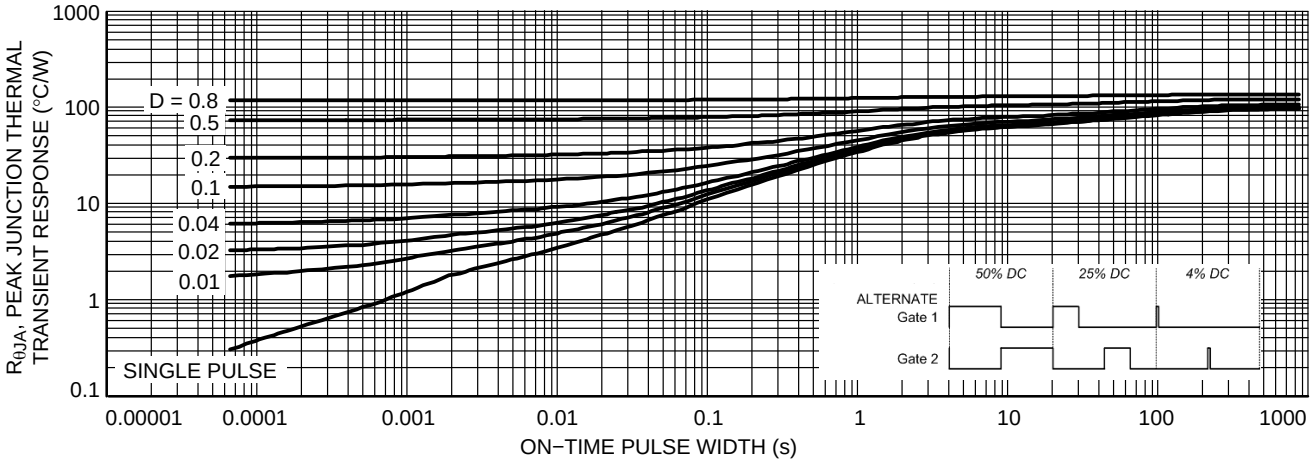


Figure 16. Channels Alternatively Active; Mounted on 1 Sq. Inch Copper Spreader

TYPICAL APPLICATION CIRCUIT

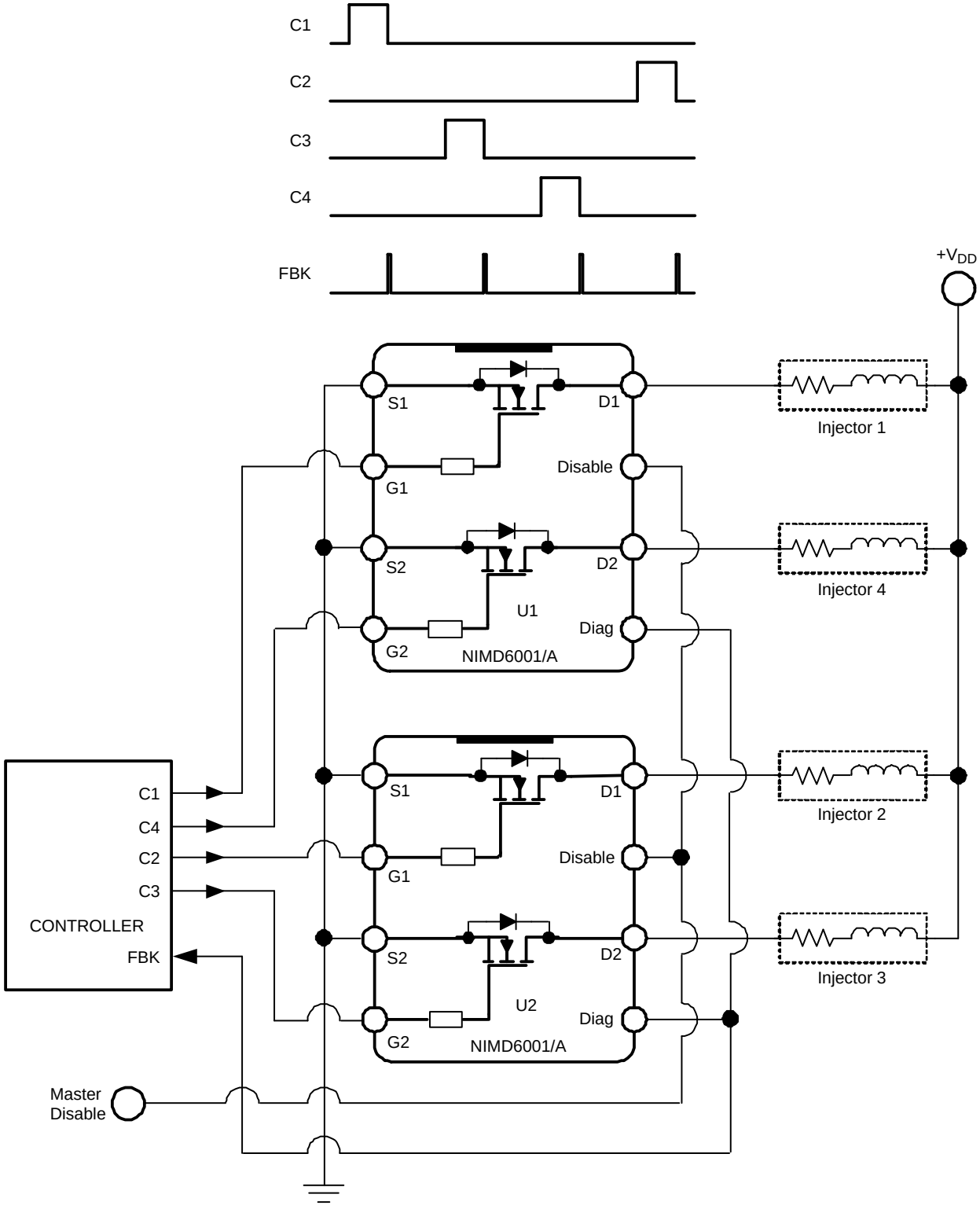


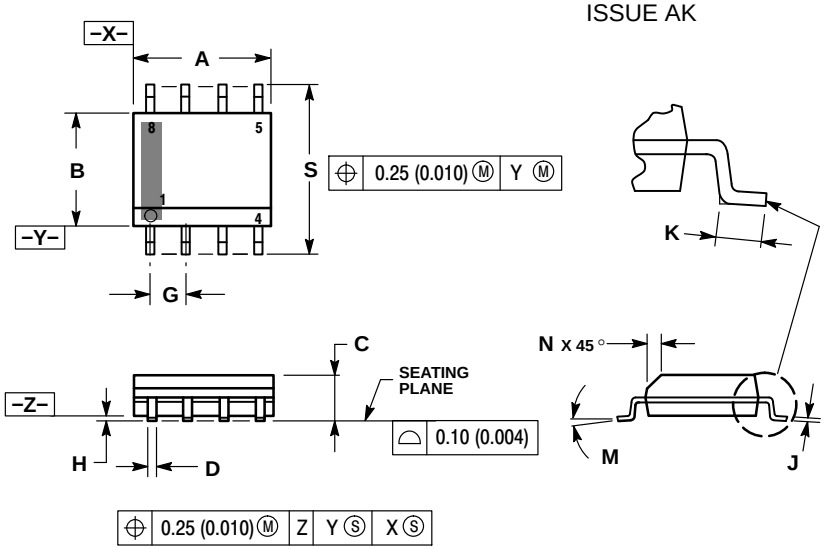
Figure 17. 4 Cylinder Engine Fuel Injection

- 4-Cycle engine; 1 injector pulse during intake stroke
- To optimize transient thermal resistance of the NIMD6001/A devices, the injector drive pulses are alternated between U1 and U2.
- Cylinder firing order is 1-3-4-2
- The coincident FBK pulse will be missing if any injector is open or shorted.

NIMD6001AN

PACKAGE DIMENSIONS

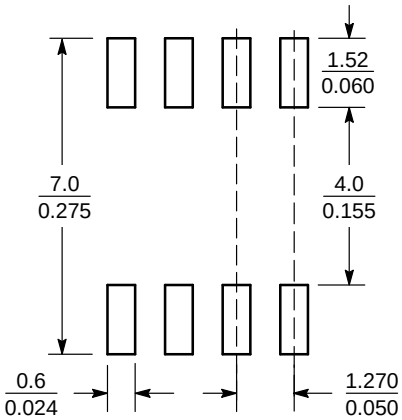
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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