NIS3120, NIS3121, NIS3220, NIS3221, NIS3320

Product Preview

12 V eFuse

Low Pin Count Electronic Fuse

The Low Pin Count series NIS3x2x provides full protection to systems and loads which may encounter large current conditions. These devices have a built−in soft start feature that ramps the output voltage to minimize inrush current from the system's power supply. Additionally, the NIS3x2x devices may be controlled by external circuitry via its active−high or active low disable pin and communicate status via its tri−state enable/fault pin. The devices features a thermal shutdown circuit with auto−retry to allow operation after the fault is cleared.

Features

- 95 mΩ Typical $R_{DS(on)}$
- Tri−State Enable and Fault Indicator pin
- Active−Low or Active−High Disable pin
- Internal Fixed Current limit
- Internal Undervoltage Lockout Circuit
- Internal Overvoltage Clamp Circuit
- Both Latching and Auto−Retry Options Available
- Integrated Current Monitoring
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Load Switching
- Motor Control
- Industrial

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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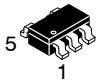
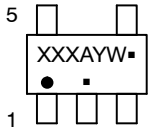


TSOP−5
CASE 483

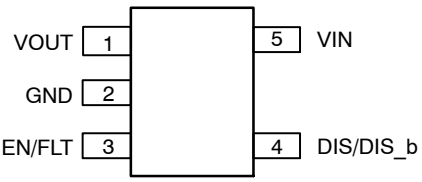
MARKING DIAGRAM



XXX	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Function	Description
1	VOUT	Voltage output
2	GND	Ground connection
3	EN/FLT	Tri−State Enable/FAULT pin. Stays at 3.3 V during normal operation, pulled to 1.4 V during thermal shut-down. Can be left floating or pulled low with Open−Drain/Open−Collector device to disable the output
4	DIS/DIS_b	Active−High/Active−Low disable pin. Refer to order table for polarity of the pin.
5	VIN	Positive input voltage to the device

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VIN, VOUT Pin Input Voltage to GND, operating, steady−state (Note 1)	$VIN_{(IN,EN,OUT)}$	−0.6 to 18	V
All Other pins	V_{dvdt}, V_{ILIM}, V_{PGOOD}, V_{FLAG}, V_{IMON}	−0.6 to 5.5	V
Thermal Resistance, Junction−to−Air 0.1 in^2 copper (Note 2) 0.5 in^2 copper (Note 2)	θ_{JA}	 TBD TBD	°C/W
Thermal Resistance, Junction−to−Lead	θ_{JL}	TBD	°C/W
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_{MAX}	TBD TBD	W mW/°C
Operating Temperature Range (Note 3)	T_J	−40 to 150	°C
Non−operating Temperature Range	T_J	−55 to 150	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. 1 oz copper, double−sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than maximum ratings for extended periods of time.

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
ON Resistance, T_J = 25°C	$R_{DS(on)}$		95	120	mΩ
ON Resistance, T_J = 85°C			TBD		
Continuous Current (T_A = 25°C, 0.5 sq in pad)	Id		1		A
Off State Output Voltage (V_{IN} = 24 V, V_{EN} = 0 V, T_A = 25°C)	Voff			50	mV
THERMAL SHUTDOWN					
Shutdown Temperature	T_{SD}		175		°C
Thermal Hysteresis (Decrease in die temperature for turn on)	T_{HYST}		40		°C
UNDERVOLTAGE PROTECTION					
Undervoltage Lockout (See Ordering Information)	V_{UVLO}		8.5		V
Undervoltage Lockout (See Ordering Information)	V_{UVLO}		4.7		V
Undervoltage Lockout Hysteresis	$V_{(UVLO)Hyst}$		TBD		V
Undervoltage Lockout Response Time	tV_{UVLO}			5	μs
OUTPUT CLAMPING VOLTAGE					
Output Clamping Voltage (V_{IN} = 18 V)	V_{CLAMP}	14		16	V
Output Clamping Voltage Response Time	t_{CLAMP}			5	μs

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
FORWARD CURRENT LIMIT					
NIS3120: Trip Current Limit	I_{TRIP}	0.9	1	1.1	A
NIS3120: Hold Current Limit	I_{HOLD}	0.54	0.6	0.66	A
NIS3121: Trip Current Limit	I_{TRIP}	1.35	1.5	1.65	A
NIS3121: Hold Current Limit	I_{HOLD}	0.9	1	1.1	A
NIS3220: Trip Current Limit	I_{TRIP}	1.8	2	2.2	A
NIS3220: Hold Current Limit	I_{HOLD}	1.35	1.5	1.65	A
NIS3221: Trip Current Limit	I_{TRIP}	2.25	2.5	2.75	A
NIS3221: Hold Current Limit	I_{HOLD}	1.8	2	2.2	A
NIS3320: Trip Current Limit	I_{TRIP}	2.7	3	3.3	A
NIS3320: Hold Current Limit	I_{HOLD}	2.25	2.5	2.75	A
Current Limit Error Tolerance	$I_{TRIP}/I_{HOLD(Tol)}$	−10		10	%
Current Limit Response Time	t_{ILIM}			10	μs
Short Circuit Trip Current	I_{SHORT}		2xILIM		μs
Short Circuit Response Time	t_{SHORT}			10	μs
TURN ON AND SLEW CONTROL					
Slew Rate On (No Load, Cin = 0.1μF, Cout=0.1μF)	SR(On)	0.7		1.9	ms
Slew Rate Off (No Load, Cin = 0.1μF, Cout=0.1μF)	SR(Off)		TBD		ms
Output On Delay Time (No Load, Cin = 0.1μF, Cout=0.1μF)	$t_{DLY(On)}$		200		μs
Enable On Delay Time (No Load, Cin = 0.1μF, Cout=0.1μF)	$t_{EN(On)}$		TBD		μs
Enable−Output On Delay Time (No Load, Cin = 0.1μF, Cout=0.1μF)	$t_{DLY(En)}$		TBD		μs
Output Off Delay Time (No Load, Cin = 0.1μF, Cout=0.1μF)	$t_{DLY(Off)}$		TBD		μs
Enable Off Delay Time	$t_{EN(Off)}$		TBD		μs
LOGIC INPUT/OUTPUT (NIS3x2x)					
Disable Pin Logic Level Low	$DIS_{(VIL)}$			0.4	V
Disable Pin Logic Level High	$DIS_{(VIH)}$	1.2			V
Input Logic Level Low (Output Disabled)	$EN_{(VIL)}$			0.3	V
Output Logic Level Low (Output Disabled)	$EN_{(VOL)}$			0.81	V
Output Logic Level Mid (Thermal Fault, Output Disabled)	$EN_{(MID)}$	0.82	1.4	1.95	V
Output Logic Level High (Output Disabled)	$EN_{(VOH)}$	1.96			V
Logic Low Sink Current (Venable = 0 V)	$EN_{(ISink)}$		15	25	μA
Logic High Leakage Current for External Switch (Venable = 3.3 V)	$EN_{(ILeak)}$			1	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	$EN_{(Fanout)}$		3		Units
SUPPLY CURRENT					
Bias Current Operational (V_{IN} = 12 V)	$I_{BIAS(ON)}$			300	μA
Bias Current Shutdown (V_{IN} = 12 V, Device disabled; NIS3x2x)	$I_{BIAS(OFF)}$			20	μA
Bias Current During Thermal Shutdown	$I_{Bias(Fault)}$		100	TBD	μA
ESD CHARACTERISTICS					
Human Body Model (All pins)	ESD−HBM		±2		kV
Charged Device Model (All pins)	ESD−CDM		±1		kV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

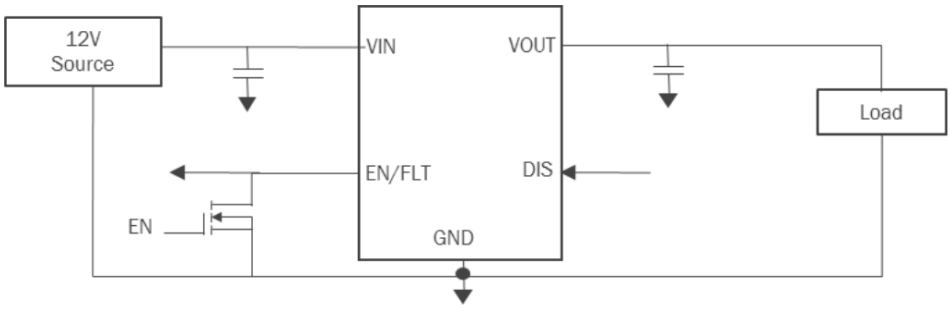


Figure 1. Typical Application Circuit

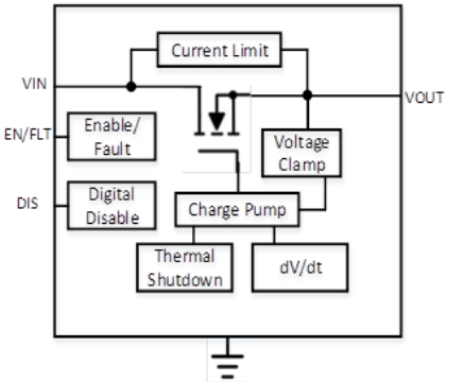


Figure 2. Block Diagram

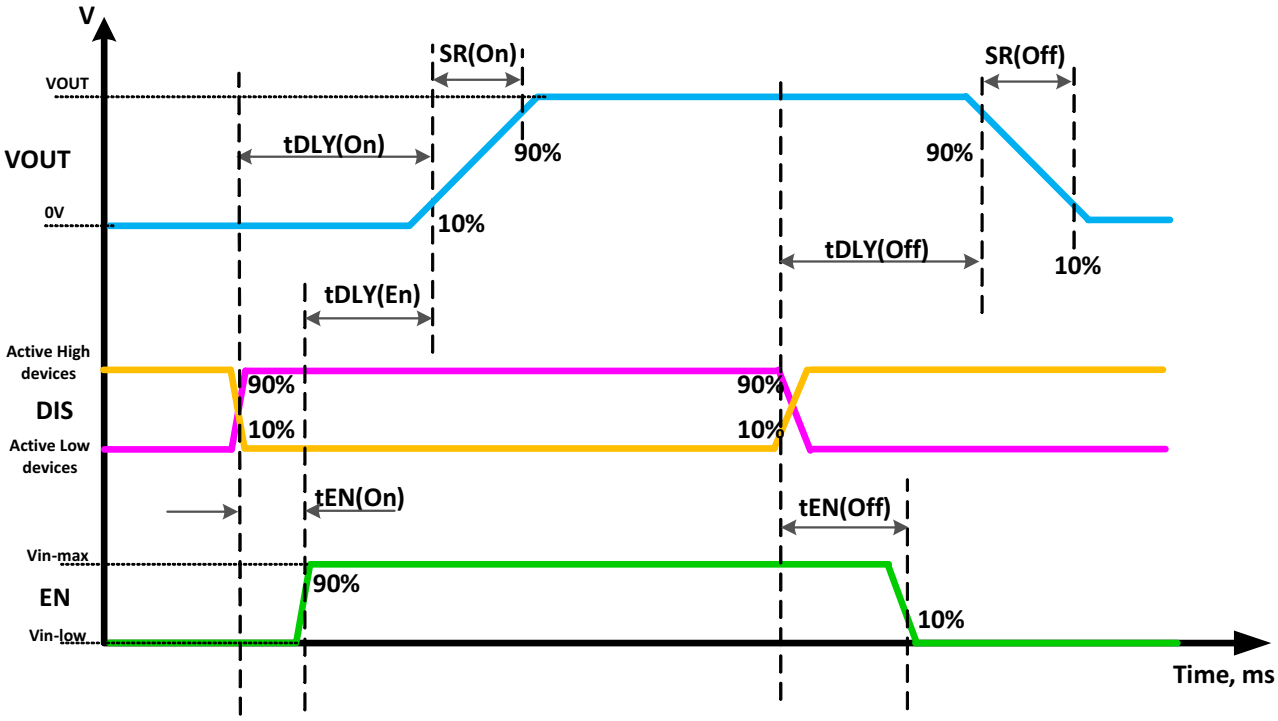


Figure 3. Turn on and Slew Rate Diagram

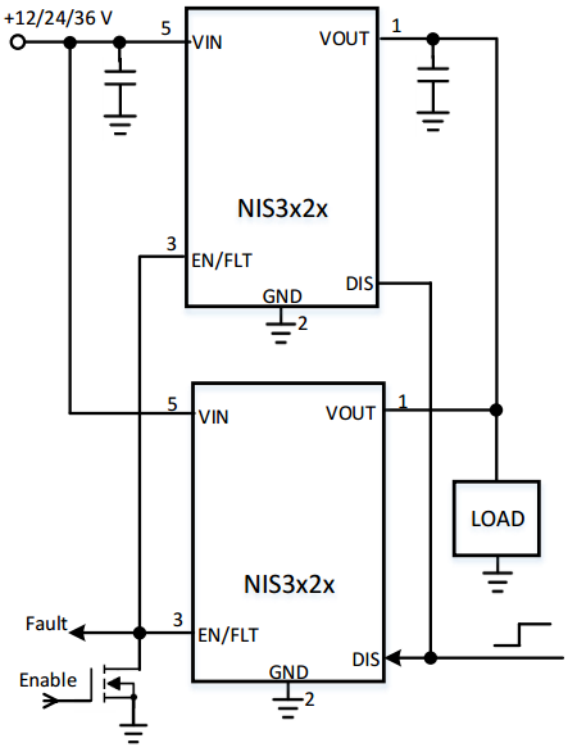


Figure 4. Paralleling Two NIS3x2x Devices

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature. On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage is controlled by internal fixed slew rate circuit that will slew from 0 V to the rated output voltage. The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level. An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage and ground. The NIS3x2x device also employs the control and fault monitoring pins.

Current Limit

The current limit circuit uses a reference and amplifier to control the peak current in the device. The structure allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor. The current limit circuit has a limiting value which is programmed into the chip. User can select the part number with desired programmed current limit.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the Vclamp voltage, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for a longer time, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level the output of the device will be disabled.

Turn On and Slew Rate Control

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor.

Refer to Figure 3 for definitions of slew rate and turn on delays.

Enable/Fault Pin

The Enable/Fault Pin is a multi−function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned−on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit. To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri−state operation, it should not be connected to any type of logic with an internal pull−up device. Do not connect external capacitor directly to this pin.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred.

If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto−retry devices. Since this is a latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled. This example is illustrated in Figure 4.

Disable Pin

The disable pin is a digital active low or active high pin (depending on the device selection) and it can be driven by external digital signal to manually shut down the output.

Thermal Protection

The NIS3x2x include an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. If a latching device is used, output power can be restored by either recycling the input power or toggling the disable pin. An auto−retry device will automatically try to restore output power on its own. The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 125°C for extended periods of time.

Latching vs. Auto−Retry

This device features two options regarding its reset ability after a thermal shutdown event. These are called latching and auto−retry which are respectively marked MT1 and MT2 as part number suffixes. Upon reaching a thermal shutdown state, a latching device (MT1) will remain shutdown with no power supplied to the output pin. The only way to reset the device is to either perform a power cycle on the VCC bus or toggle the disable pin. By doing either of these actions, the fault state is cleared and the device is allowed to pull−up the output to its normal, high state. Instead of remaining in thermal shutdown, an Auto−retry device (MT2) will automatically attempt to pull up the output once the die temperature cools to < 135°C. If the fault remains on the output during this attempt, the device will once again enter a short period of current limiting that will eventually lead to thermal shutdown for which the auto−retry process will repeat indefinitely.

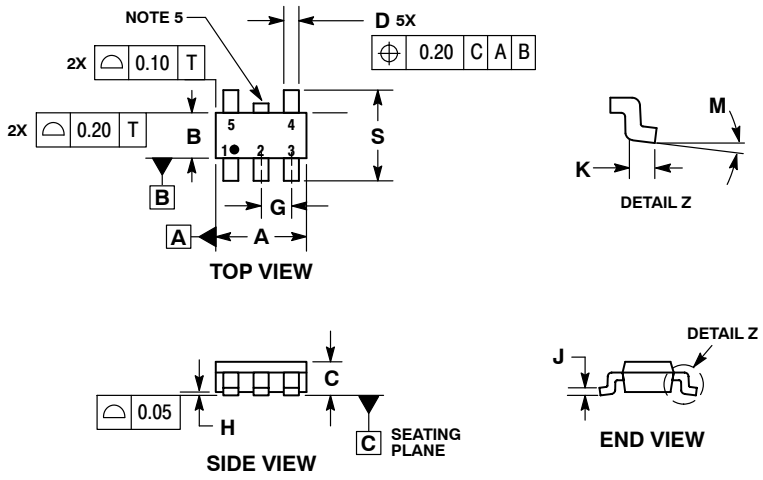
ORDERING INFORMATION

Part #	ITRIP, A	Disable Pin Polarity	OV Clamp, V	UVLO, V	Package	Auto−Retry/ Latch	Shipping†
NIS31202MR5T1G	1	Low	15	8.5	TSOP−5	Auto−Retry	TBD / Tape & Reel
NIS31204MR5T1G	1	Low	15	8.5	TSOP−5	Latch	
NIS31206MR5T1G	1	Low	Disabled	4.7	TSOP−5	Auto−Retry	
NIS31208MR5T1G	1	Low	Disabled	4.7	TSOP−5	Latch	
NIS31216MR5T1G	1.5	Low	Disabled	4.7	TSOP−5	Auto−Retry	
NIS31218MR5T1G	1.5	Low	Disabled	4.7	TSOP−5	Latch	
NIS32206MR5T1G	2	Low	Disabled	4.7	TSOP−5	Auto−Retry	
NIS32208MR5T1G	2	Low	Disabled	4.7	TSOP−5	Latch	
NIS32212MR5T1G	2.5	Low	15	8.5	TSOP−5	Auto−Retry	
NIS32214MR5T1G	2.5	Low	15	8.5	TSOP−5	Latch	
NIS33201MR5T1G	3	High	15	8.5	TSOP−5	Auto−Retry	
NIS33203MR5T1G	3	High	15	8.5	TSOP−5	Latch	
NIS33206MR5T1G	3	Low	Disabled	4.7	TSOP−5	Auto−Retry	
NIS33208MR5T1G	3	Low	Disabled	4.7	TSOP−5	Latch	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

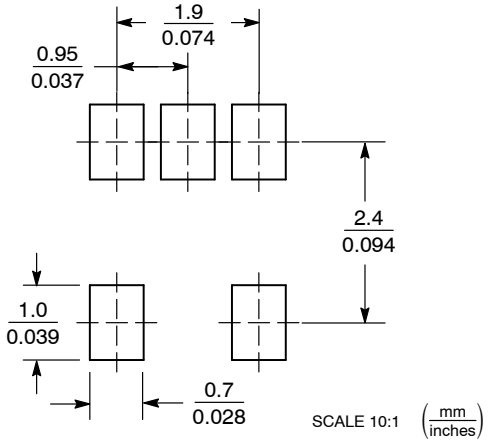
TSOP−5
CASE 483
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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