NIS6160, NIV6160

Product Preview

+40 V, 1 A Electronic Fuse

The NIS6160 is a cost effective, resettable fuse which can greatly enhance the reliability of a vehicle telematics unit from both catastrophic and shutdown failures. It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits and to protect the input side circuitry from reverse currents. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation. Its dual operation voltage of 14 and 24 V makes it ideal for use in both automotive and industrial applications respectively.

Features

- 190 mΩ Typical Rds(ON)
- Integrated Reverse Current Protection
- Output Voltage Power Good Indicator
- Digital Enable with Separate FLAG for Fault Identification
- Adjustable Output Voltage Slew Rate
- Adjustable Output Current Limit Protection with Thermal Shutdown
- Fast Response Overvoltage Clamp Circuit
- Internal Undervoltage Lockout Circuit
- Both Latching and Auto−Retry Options Available
- Integrated Current Monitoring
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive Telematics Unit
- Active Antenna
- Industrial
- Automotive Gateways
- Industrial Automation

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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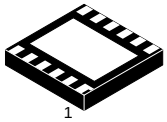


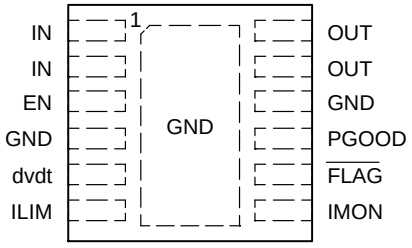
WDFNW12
3 x 3
CASE 515AJ

MARKING DIAGRAM

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Function	Description
1,2	IN	Positive input voltage to the device.
3	EN	When this pin is pulled low the eFuse is turned off. It can be used to enable or disable the output of the device by pulling it to ground using an open drain or open collector device, as it has an internal pull−up.
4,10	GND	Ground pin.
5	dvdt	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 1 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
6	ILIM	A resistor between this pin and the GND pin sets the overload and short circuit current limit levels.
7	IMON	Current monitoring pin. Connect a 1% tolerance RIMON resistor from this pin to Ground in order to read the voltage proportional to current load.
8	$\overline{\text{FLAG}}$	Open Drain fault pin. If a fault occurs, the voltage on this pin will be forced to a low state to signal a monitoring circuit the fault condition. The pin is floating when no fault is detected. Pin can be pulled high to 5 V logic rail with at least 10 kΩ resistor or left unconnected if not used.
9	PGOOD	Open Drain power good pin. If output voltage is less than input UVLO value, the voltage on this pin will be forced to a low state. The pin is floating when output voltage is higher than UVLO value. Pin can be pulled high to 5 V logic rail with at least 10 kΩ resistor or left unconnected if not used.
11,12	OUT	Source of the internal power FET and the output terminal of the fuse.
13	PAD	Connect to ground

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN,EN,OUT Pin Input Voltage to GND, operating, steady−state (Note 1)	$VIN_{(IN,EN,OUT)}$	−28 to +40	V
All Other pins	V_{dvdt}, V_{ILIM}, V_{PGOOD}, $V_{\overline{FLAG}}$, V_{IMON}	−0.3 to 5.5	V
Thermal Resistance, Junction−to−Air (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	TBD	°C/W
Thermal Characterization Parameter, Junction−to−Lead (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-L}	TBD	°C/W
Thermal Characterization Parameter, Junction−to−Board (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-B}	TBD	°C/W
Total Continuous Power Dissipation @ T_A = 25°C (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25°C	P_{max}	TBD TBD	W mW/°C
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Operating Junction Temperature Range (Note 2)	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than maximum ratings for extended periods of time.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 14 V, C_L = 100 μF, dvdt pin open, R_{LIMIT} = 60 kΩ, for typical values T_A = 25°C, min/max values are valid for T_A = −40°C to 125°C per AEC−Q100 grade 1 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
Delay Time (Enabling of chip to ID = 100 mA with 1 A resistive load)	Tdly		500		μs
ON Resistance T_J = 25°C T_J = 85°C T_J = 150°C	$R_{ds(ON)}$		190 TBD TBD	240	mΩ
Continuous Current (T_A = 25°C, 0.5 in^2 1 oz. Cu pad, 2−layer FR−4)	Id		1		A
Off State Leakage (V_{IN} = 24 V, V_{EN} = 0 V, T_A = 25°C)	Ioff		1		μA
THERMAL SHUTDOWN					
Shutdown Temperature	T_{SD}	150	175	200	°C
Thermal Hysteresis (Decrease in die temperature for turn on)	T_{HYST}		40		°C
UNDERVOLTAGE PROTECTION					
Undervoltage Lockout Falling	$V_{UVLO−f}$		2.9		V
Undervoltage Lockout Rising	$V_{UVLO−r}$		3.4		V
Undervoltage Lockout Hysteresis	$V_{(UVLO)Hyst}$		0.5		V
Undervoltage Lockout Response Time	tV_{UVLO}		2		μs
OUTPUT CLAMPING VOLTAGE					
Output Clamping Voltage (V_{IN} = 40 V)	V_{CLAMP}	30	33	36	V
Output Clamping Voltage Response Time	t_{VCLAMP}		2		μs
FORWARD CURRENT LIMIT					
Current Limit (R_{LIM} = open) (R_{LIM} = 60 kΩ) (R_{LIM} = 0 kΩ)	I_{LIM}		0.01 1.2 1.8		A
Circuit Breaker Response Time	t_{CB}		1		μs
Minimum Settable Current Limit	$I_{LIM(Min)}$		0.1		A
Circuit Breaker Current	I_{CB}		1.5 x I_{LIM}		A
Current Trip Timer	t_{TRIP}		500		μs
REVERSE CURRENT PROTECTION					
Reverse Current Blocking Threshold (V_{OUT}−V_{IN})	Vrev−th	40	60	80	mV
Reverse Current Blocking Response Time	Vrev−resp	5	7.5	10	μs
LOGIC INPUT/OUTPUT					
Logic Level Low, EN pin (Device Disabled)	$V_{IL(EN)}$			0.4	V
Logic Level High, EN pin (Device Enabled)	$V_{IH(EN)}$	1.2			V
De−glitch Filter−delay, EN pin	$t_{DLY(EN)}$	2		50	μs
Enable Pin Hysteresis	EN_{Hys}		0.1		V
Output Voltage Low ($\overline{FLAG}$, PG pins)	V_{OL}			0.2	V
Logic High Sink Current ($\overline{FLAG}$, PG pins)	I_O			0.5	mA
SLEW RATE CONTROL					
Output Voltage Ramp Time	t_{slew}		1		ms
LOAD CURRENT MONITORING					
Load Monitor Sense Current (RIMON = TBD)	I_{SENSE}		1		mA/A

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 14 V, C_L = 100 μF, dvdt pin open, R_{LIMIT} = 60 kΩ, for typical values T_A = 25°C, min/max values are valid for T_A = −40°C to 125°C per AEC−Q100 grade 1 unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT						
Bias Current Operational	(V_{IN} = 24 V, V_{EN} = 5 V) (V_{IN} = 14 V, V_{EN} = 5 V)	$I_{BIAS(ON)}$		TBD TBD		μA
Bias Current Shutdown	(V_{IN} = 24 V, V_{EN} = 0 V) (V_{IN} = 14 V, V_{EN} = 5 V)	$I_{BIAS(OFF)}$		TBD TBD		μA
ESD CHARACTERISTICS						
Human Body Model (All pins)		ESD−HBM		±2		kV
Charged Device Model (All pins)		ESD−CDM		±1		kV
ISO 10605 (150 pF/330 Ω)		ESD−ISO		±6		kV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PROTECTION FEATURES

Protection	Min	Typ	Max	Unit	Test Conditions
Ground Loss Disable time	5			μs	Resistor from GND pin to Ground goes from 100 mΩ to 1 MΩ
ISO7637−2	−300			V	Pulse 1, 500 pulses
	112			V	Pulse 2a, 500 pulses
	20			V	Pulse 2b, 10 pulses
	−200			V	Pulse 3a, 1 hour
	200			V	Pulse 3b, 1 hour
ISO16750−2	40			V	Test B, U_N = 24 V
ISO7637−3	112			V	Pulse 2a, Level IV
	−150			V	Pulse 3a, Level IV
	150			V	Pulse 3b, Level IV
JESD78	−100		+100	mA	Class II
IEC−61967−4			80 (150−300 kHz) 58 (0.5−2 MHz) 50 (5−10 MHz) 40 (10−100 MHz) 30 (100−300 MHz)	dBμV	VIN = 13.5 V/1 A 150 Ω method
IEC 62132−4 ISO 11452−7	35 (1−110 MHz) 24 (110−1000 MHz)			dBm	VIN = 13.5 V F = 1−1000 MHz CW, AM (1 kHz, 80%)

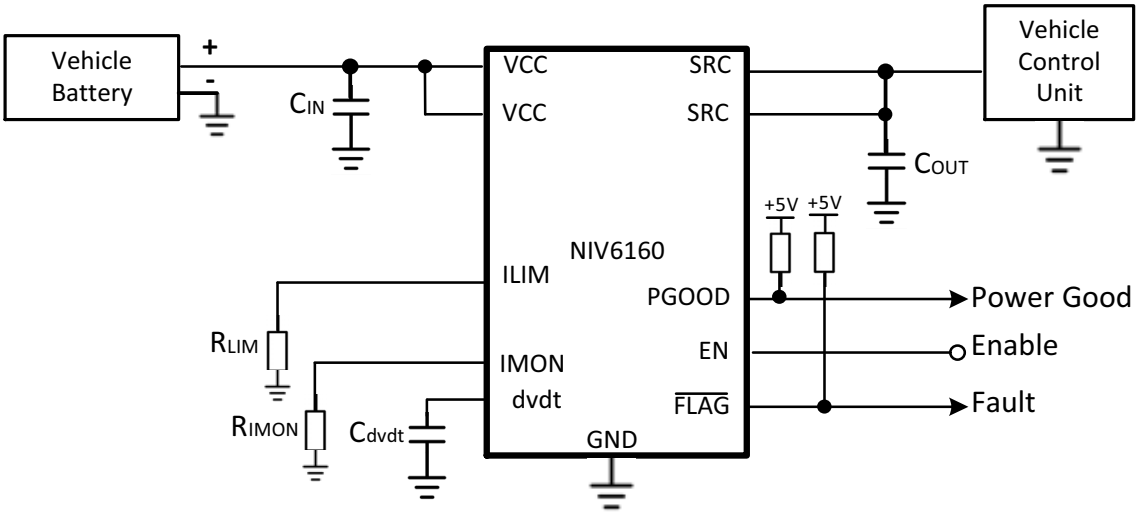


Figure 1. Typical Application Circuit

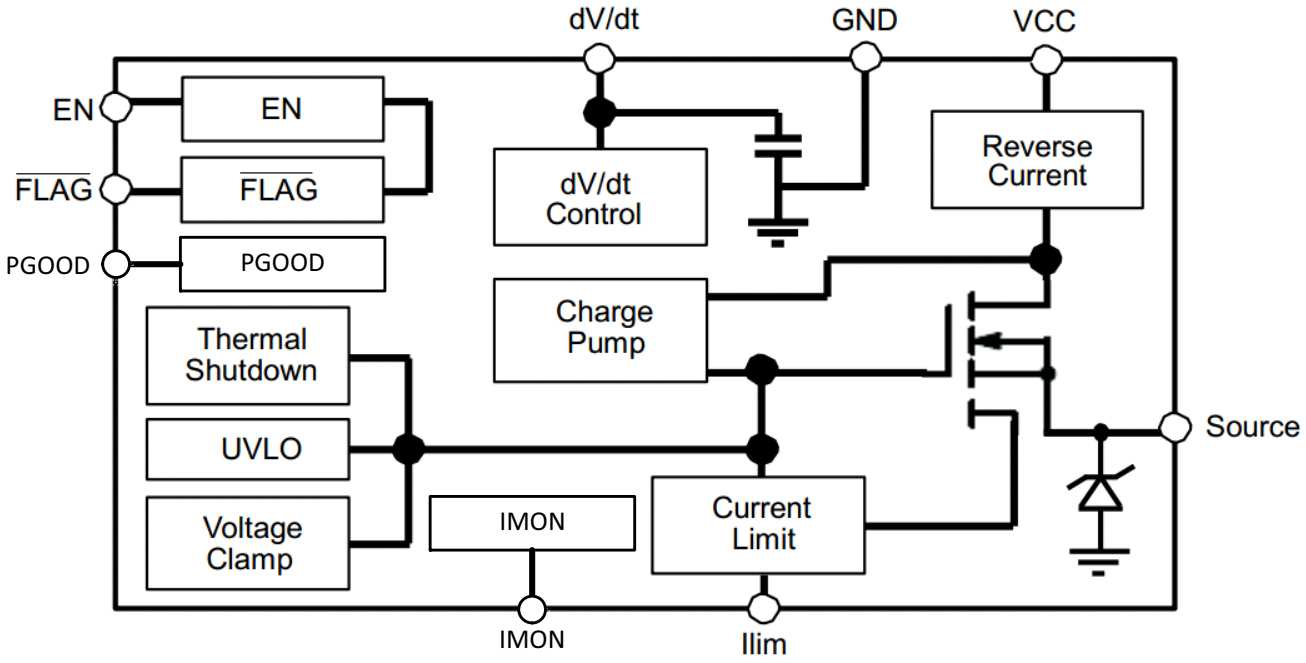


Figure 2. Block Diagram

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature. On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage can be controlled by an external dv/dt circuit that will slew from 0 V to the rated output voltage in the desired time. The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip. The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level. An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (VCC) and ground. The device also employs the load current monitoring feature as well as indicator pins such as PGOOD and $\overline{\text{FLAG}}$.

Overcurrent Protection

Overcurrent protection circuit is monitoring the load current and allows the load to draw current as long as its level is within allowable overcurrent range defined by ILIM and ICB. The ILIM is the overcurrent limit set by RLIM resistor, and ICB is a circuit breaker level which is 1.5x of ILIM; as long as the load is drawing current not exceeding the ICB level the FET is on, if the current level exceeds the ICB level the FET is turned off. If during the overcurrent mode the internal temperature for the channel FET exceeds the threshold level, the FET will be shut off. Additional device options offer a overcurrent trip timer which starts counting right after the load current exceeds the ILIM level, once the predetermined amount of time elapsed the channel will be shut off. Examples of a typical operation for such scheme is shown in Figure 3.

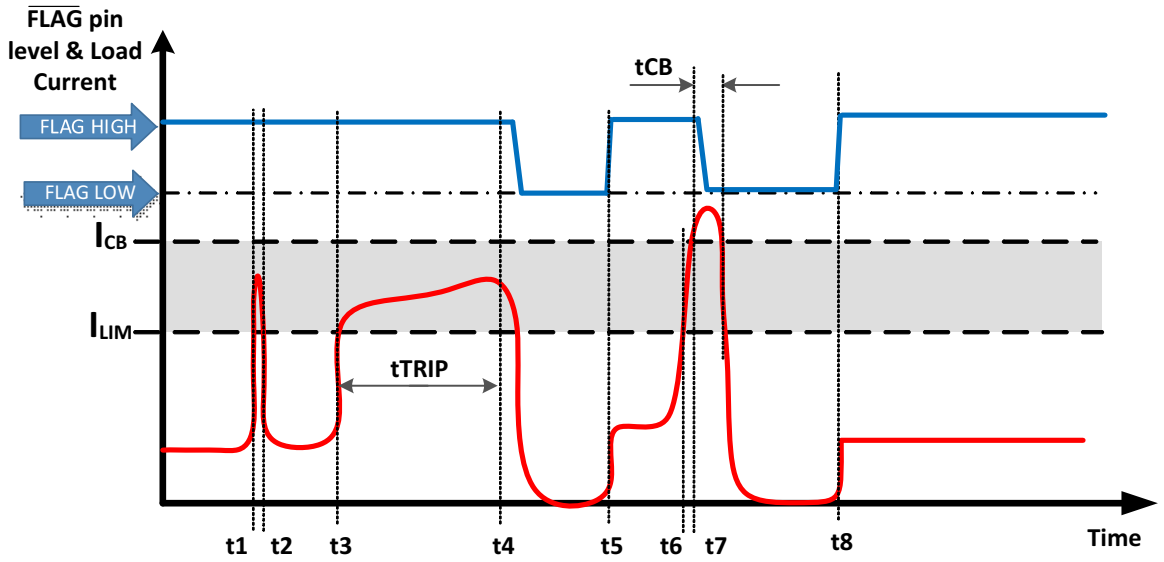


Figure 3. Overcurrent Protection Example Diagram

NOTE: t1: Current above I_{LIM}, t_{TRIP} counter started
t2: Current went below I_{LIM} before t_{TRIP} reached final count value. t_{TRIP} counter cleared, normal operation resumes
t3: Current above I_{LIM}, t_{TRIP} counter started. Device lets a load to draw as much current as it needs **as long as** it is below ICB and FET is not overheat
t4: Device is shut down due to: A) t_{TRIP} timer ran out, OR B) Thermal shutdown, OR C) Current reached above ICB. $\overline{\text{FLAG}}$ is pulled Low.
t5: Device restarted when FET temperature reduced by 40°C (Auto−Retry version only; Latched version will require manual restart with EN pin)
t6: Output short happened (or severe overload)
t7: Current reached ICB level (output short is one reason). The device is immediately shut down within t_{CB} time. $\overline{\text{FLAG}}$ pulled low
t8: FET cooled down by 40°C (For Auto−Retry), OR device manually restarted (Latch Mode) and FET is below 40°C; normal operation resumed

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds the Vclamp voltage, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for a longer time, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level the output of the device will be disabled.

Load Current Monitoring

The current monitor “IMON” pin provides a small current proportional to the main device current which is passing through the device. This pin should have a decoupling capacitor to filter out internal sampling noise. A resistor connected between the IMON pin and GND converts the IMON current into a GND referenced voltage. This pin can be floated if the feature is not required by application.

Slew Rate Control

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor. The default ramp time

is approximately 1 ms. This can be modified by adding an external capacitor at the dv/dt pin.

This pin includes an internal current source. Since the current level is very low, it is important to use a ceramic capacitor or any other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit.

Enable Pin

The Enable feature provides a digital interface to control the output of the eFuse, without the need of any additional interface logic. When the EN pin is pulled high (above 1.2 V) by any external digital control circuitry the eFuse switches to its on state. When the EN pin is pulled low (below 0.4 V) the eFuse output is turned off. All fault conditions will be cleared when the eFuse is reset through the EN pin.

$\overline{\text{FLAG}}$ Pin

The $\overline{\text{FLAG}}$ Pin sends information to other devices regarding the state of the chip. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. When this pin is low, the output of the eFuse is turned off. When this pin is in high impedance the output of the eFuse is turned on. There are four conditions that will set the $\overline{\text{FLAG}}$ pin to low and subsequently turn the device off:

1. EN pin set to Logic Level Low (Output Disabled)
2. Thermal fault
3. UVLO − Undervoltage Lockout
4. Reverse current fault

The $\overline{\text{FLAG}}$ is an open−drain output pin; when used, it is supposed to be pulled up to 5 V supply. It can be left unconnected if the pin is not used in the application.

PGOOD Pin

The open−drain PG pin will be in high impedance state if the output voltage at the OUT pin is within normal operating range. The normal operating voltage range for the OUT pin is between minimum UVLO and maximum Output Clamp voltage. The PGOOD is an open−drain output pin; when used, it is supposed to be pulled up to 5 V supply. It can be left unconnected if the pin is not used in the application.

Thermal Protection

The NIS6160, NIV6160 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. If a latching device is used, output power can be restored by either recycling the input power or toggling the enable pin. An auto−retry device will automatically try to restore output power on its own. The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 125°C for extended periods of time.

Latching vs. Auto−Retry

This device features two options regarding its reset ability after a thermal shutdown event. These are called latching and auto−retry which are respectively marked MT1 and MT2 as part number suffixes. Upon reaching a thermal shutdown state, a latching device (MT1) will remain shutdown with no power supplied to the output (SRC pins). The only way to reset the device is to either perform a power cycle on the VCC bus or pull the EN pin low (<0.4 V). By doing either of these actions, the fault state is cleared and the device is allowed to pull−up the output to its normal, high state. Instead of remaining in thermal shutdown, an Auto−retry device (MT2) will automatically attempt to pull up the output once the die temperature cools to < 135°C. If the fault remains on the output during this attempt, the device will once again enter a short period of current limiting that will eventually lead to thermal shutdown for which the auto−retry process will repeat indefinitely.

Reverse Current Protection

The NIS6160 also provides a reverse current protection feature. If the input voltage becomes less than the output voltage by more than the Vrev−th threshold amount, the reverse blocking FET will shut off and the reverse current will be stopped within a short amount of time defined as Vrev−resp. Once the input and output voltage difference is less than the Vrev−th threshold the blocking FET will turn back on and reverse current protection deactivates. Typical operation of this feature is shown in Figure 4.

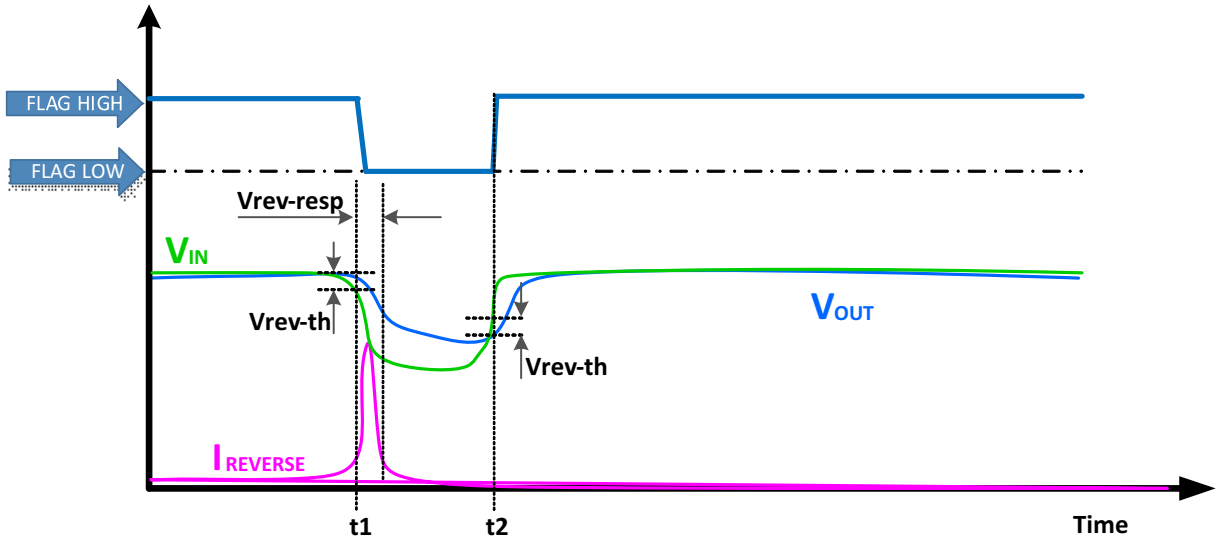


Figure 4. Reverse Current Protection Diagram

NOTE: t1: V_{IN} dropped below V_{OUT} by more than $\mathbf{V_{rev-th}}$ value. $I_{reverse}$ starts flowing. FET turned off. $\overline{FLAG}$ pulled Low. $I_{reverse}$ blocked within $\mathbf{V_{rev-resp}}$ time. V_{OUT} naturally discharges depending on C_{OUT}
t2: V_{IN} rises back to original value. Once V_{IN} is more than V_{OUT} by $\mathbf{V_{rev-th}}$ value. FET is turned back on. $\overline{FLAG}$ is released (pulled high). V_{OUT} starts following V_{IN} again

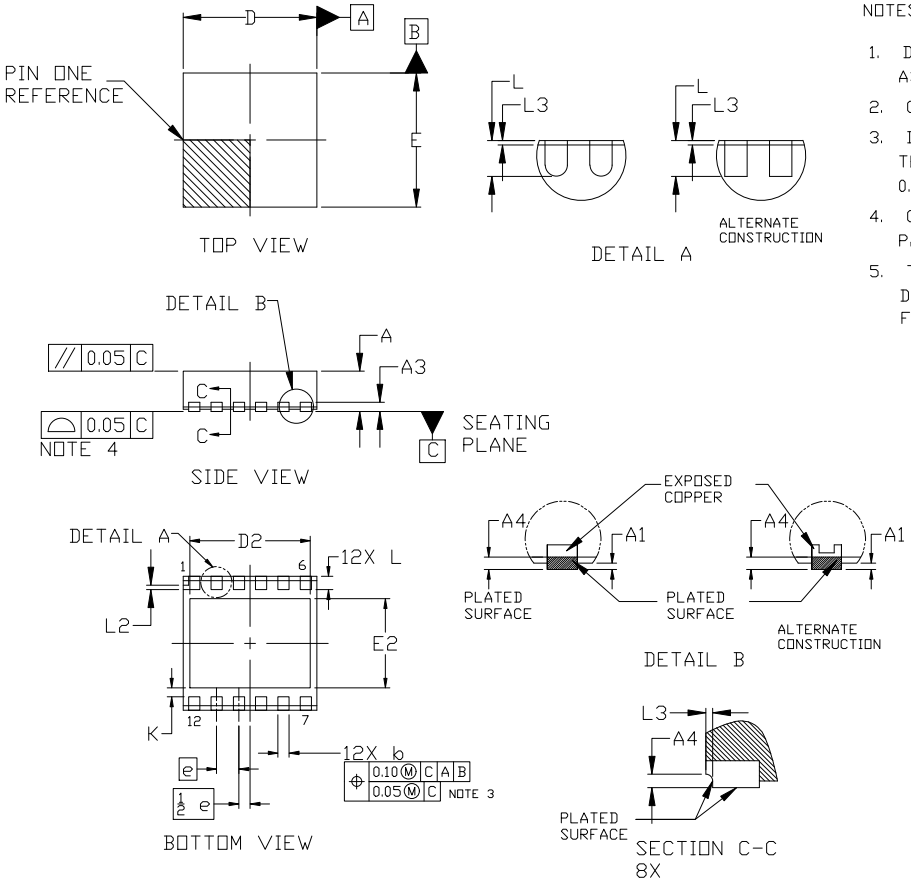
ORDERING INFORMATION

Device	Shutdown Version	Marking	Package	Shipping†
NIS6160MT1TWG	Latching	TBD	WDFNW12, 3x3 mm (Pb−Free)	TBD / Tape & Reel
NIV6160MT1TWG*	Latching	TBD		
NIS6160MT2TWG	Auto−Retry	TBD		
NIV6160MT2TWG*	Auto−Retry	TBD		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

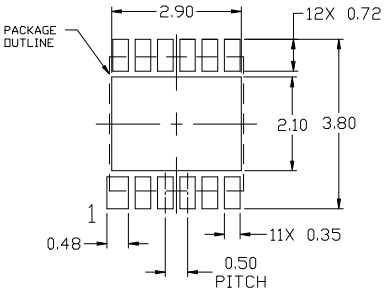
WDFNW12 3x3, 0.5P
CASE 515AJ
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	2.60	2.70	2.80
E	2.90	3.00	3.10
E2	1.90	2.00	2.10
e	0.50 BSC		
K	0.20	---	---
L	0.25	0.30	0.35
L2	0.10 REF		
L3	---	---	0.10



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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