NIS7080, NIV7080

Product Preview

+48 V Electronic Fuse

The NIS7080 is a cost effective, resettable electronic fuse which is designed to protect the load from overcurrent events, overvoltage conditions, short circuits and other faults. It includes a programmable overvoltage and undervoltage protection, adjustable internal FET power limiting, thermal protection, selectable auto−retry and latch behavior, programmable restart, insertion delay and fault timers, load current monitoring, fault and power good indicator pins and digital enable pin. The NIS7080 is perfectly suitable for typical 48 V operation in various industrial and automotive applications and the input voltage of the device is tolerant to +80 V.

Features

- 55 mΩ Typical Rds(ON)
- Programmable Overvoltage and Undervoltage Protection
- Active−Low Open−Drain Power Good Indicator
- Active−Low Open−Drain FAULT Pin Indicator
- Pin Selectable Auto−Restart/Latch Operation Mode
- Pin Selectable Circuit Breaker Operation Mode
- Adjustable Output Current Limit Protection
- Adjustable Power Limiting for Internal FET
- Adjustable FAULT Pin Timer
- Adjustable Restart Timer for Auto−Restart Mode Operation
- Adjustable Hot−Plug Insertion Delay
- Integrated Current Monitoring
- Digital Active−Low Enable Pin
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive
- Telecom
- Industrial
- Industrial Power Supplies
- Servers
- Power Tools
- Battery Management
- Lighting Systems

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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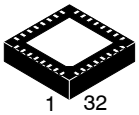
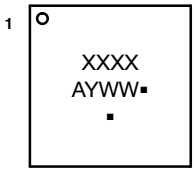


LQFN32 5x5, 0.5P
CASE 487AA

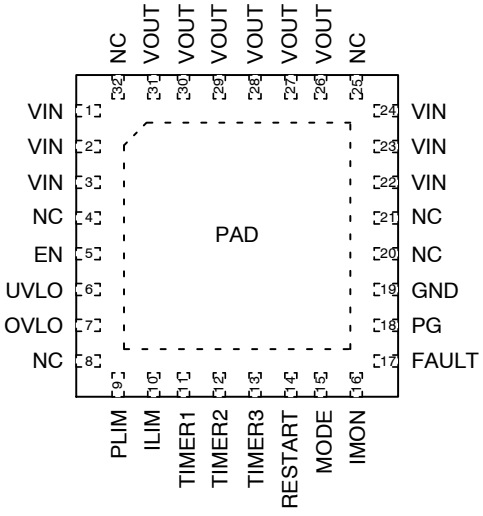
MARKING DIAGRAM



XXXX	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Function	Description
1,2,3,22,23,24	VIN	Input Voltage
4,8,20,21,25,32	NC	Do Not Connect
5	EN	Active Low Enable pin. Default pull down. By default, device is enabled. Pull High to disable.
6	UVLO	Undervoltage Lockout adjustment
7	OVLO	Overvoltage Lockout adjustment pin
15	MODE	Operation mode. Connect to GND or leave floating for power/current limit mode. Tie to logic high for circuit breaker only mode.
9	PLIM	Power Limit pin adjusted by resistor
10	ILIM	Current Limit pin adjusted by resistor
11	TIMER1	FAULT Timer value adjustment pin. Connect capacitor to GND
12	TIMER2	RESTART Timer value adjustment pin. Connect capacitor to GND
13	TIMER3	INSERTION DELAY Timer value adjustment pin. Connect capacitor to GND
14	RESTART	Auto−Retry/Latch mode select pin. Tie to GND or leave floating for auto−restart. Connect to logic High for Latch mode.
16	IMON	Current Monitoring Resistor connection pin
17	FAULT	Active Low FAULT pin. Leave floating if not used or pull up to +5 V with 10 kΩ pull up resistor.
18	PG	Active Low Power Good pin. Leave floating if not used or pull up to +5 V with 10 kΩ pull up resistor.
19	GND	Must be connected to Ground
26,27,28,29,30,31	OUT	Output Voltage
33(PAD)	PAD	Can be left floating or connected to Ground plane for better thermals

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT Pin Input Voltage to GND, operating, steady−state (Note 1)	$V_{IN/OUT}$	−0.6 to +80	V
All Other pins	Vpin	−0.6 to 5.5	V
Thermal Resistance, Junction−to−Air 0.1 in^2 copper (Note 2) 0.5 in^2 copper (Note 2)	θ_{JA}	 TBD TBD	°C/W
Thermal Resistance, Junction−to−Lead	θ_{JL}	TBD	°C/W
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_{MAX}	TBD TBD	W mW/°C
Operating Temperature Range (Note 3)	T_J	−40 to 125	°C
Non−operating Temperature Range	T_J	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. 1 oz copper, double−sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than maximum ratings for extended periods of time.

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
ON Resistance, T_J = 25°C	$R_{ds(ON)}$		55		mΩ
ON Resistance, T_J = 85°C			TBD		
Continuous Current (Ta = 25°C, 0.5 sq in pad)	Id		8		A
Off State Leakage (V_{IN} = 48 V, V_{EN} = 5 V, Ta = 25°C)	Ioff		1		μA
THERMAL SHUTDOWN					
Shutdown Temperature	T_{SD}		175		°C
Thermal Hysteresis (Auto−Restart Mode only)	T_{HYST}		40		°C
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout	V_{UVLO}		Adj.		V
Undervoltage Lockout Default Value (No R1,R2,R3 connected)	V_{UVLO}		8		V
Undervoltage Lockout Threshold value	V_{UV}		TBD		V
Undervoltage Lockout Hysteresis	$V_{(UVLO)Hyst}$		0.1		V
Undervoltage Lockout Response Time	t_{UVLO}		5		μs
Power On Reset Threshold voltage	V_{POR}		6		V
Power On Reset Threshold voltage Hysteresis	$V_{POR(Hyst)}$		0.1		V
OVERVOLTAGE LOCKOUT					
Overvoltage Lockout	V_{OVLO}		Adj.		V
Overvoltage Lockout Threshold value	V_{OV}		TBD		V
Overvoltage Lockout Hysteresis	$V_{(OVLO)Hyst}$		0.1		V
Output Clamping Voltage Response Time	t_{OVLO}		5		μs
FORWARD CURRENT LIMIT					
Current Limit (R_{LIM} = TBD)	I_{LIM}		Adj.		A
Circuit Breaker Level	I_{CB}		1.5 x I_{LIM}		A
Current Limit Response Time	t_{ILIM}		10		μs
Circuit Breaker Response Time	t_{CB}		1		μs
INTERNAL FET POWER LIMIT					
Internal FET Power Limit Threshold (RPLIM = TBD)	$PLIM_{TH}$		Adj.		W
Power Limit Threshold Current	I_{PLIM}		TBD		μA
LOGIC INPUT/OUTPUT					
Logic Level Low, EN pin (Device Enabled)	$V_{IL(EN)}$			0.8	V
Logic Level High, EN pin (Device Disabled)	$V_{IH(EN)}$	2			V
Output Voltage Low (FAULT, PGOOD pins)	V_{OL}			0.3	V
Logic High Sink Current (FAULT, PGOOD pins)	I_O		0.5		mA
POWER GOOD					
Power Good VIN−VOUT threshold voltage	$V_{PGOOD(Th)}$		1		V
TIMER CONTROL					
Timer Pin Threshold voltage, TIMER1,2,3	$V_{TIMER(Th)}$		4		V
Timer Pin Current Source value	I_{TIMER}		TBD		μA
LOAD CURRENT MONITORING					
Load Monitor Sense Current (RIMON = TBD)	I_{SENSE}		1		mA/A
Current Sense Measurement Error	$I_{SENSE(Err)}$		10		%

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT					
Bias Current Operational (V_{IN} = 48 V, V_{EN} = 0 V)	$I_{BIAS(ON)}$		TBD		μA
Bias Current Shutdown (V_{IN} = 48 V, V_{EN} = 5 V)	$I_{BIAS(OFF)}$		TBD		μA
ESD CHARACTERISTICS					
Human Body Model (All pins)	ESD−HBM		±2		kV
Charged Device Model (All pins)	ESD−CDM		500		V
IEC61000−4−2 (VIN, VOUT pins	IEC		4		kV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PROTECTION FEATURES

Protection	Min	Typ	Max	Unit	Test Conditions
Ground Loss Disable time	5			μs	Resistor from GND pin to Ground goes from 100 mΩ to 1 MΩ
ISO7637−2	−300			V	Pulse 1, 500 pulses
	112			V	Pulse 2a, 500 pulses
	20			V	Pulse 2b, 10 pulses
	−200			V	Pulse 3a, 1 hour
	200			V	Pulse 3b, 1 hour
ISO16750−2	40			V	Test B, U_N = 24 V
ISO7637−3	112			V	Pulse 2a, Level IV
	−150			V	Pulse 3a, Level IV
	150			V	Pulse 3b, Level IV
JESD78	−100		+100	mA	Class II
IEC−61967−4			80 (150−300 kHz) 58 (0.5−2 MHz) 50 (5−10 MHz) 40 (10−100 MHz) 30 (100−300 MHz)	dBμV	VIN = 13.5 V / 1 A 150 Ω method
IEC 62132−4 ISO 11452−7	35 (1−110 MHz) 24 (110−1000 MHz)			dBm	VIN = 13.5 V F = 1−1000 MHz CW, AM (1 kHz, 80%)

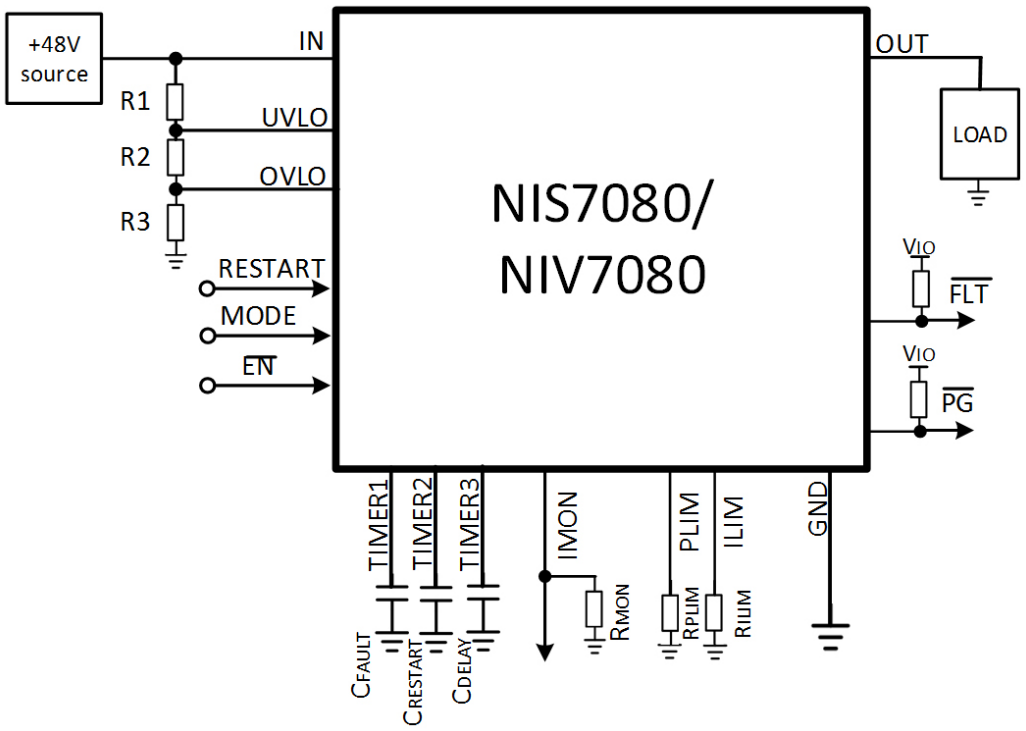


Figure 1. Typical Application Circuit

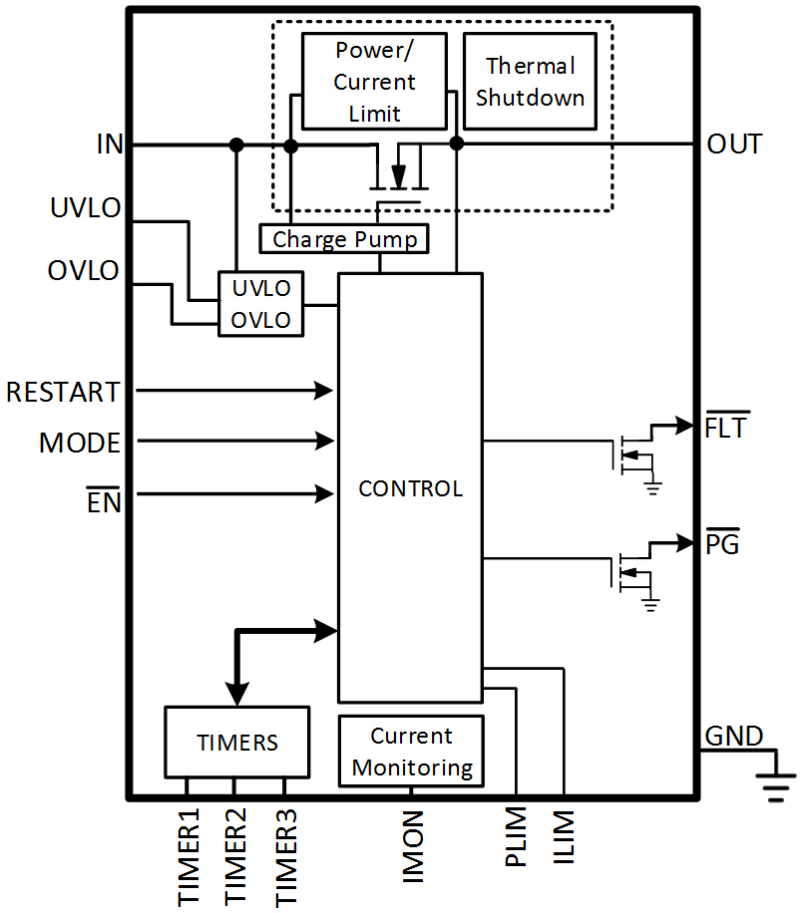
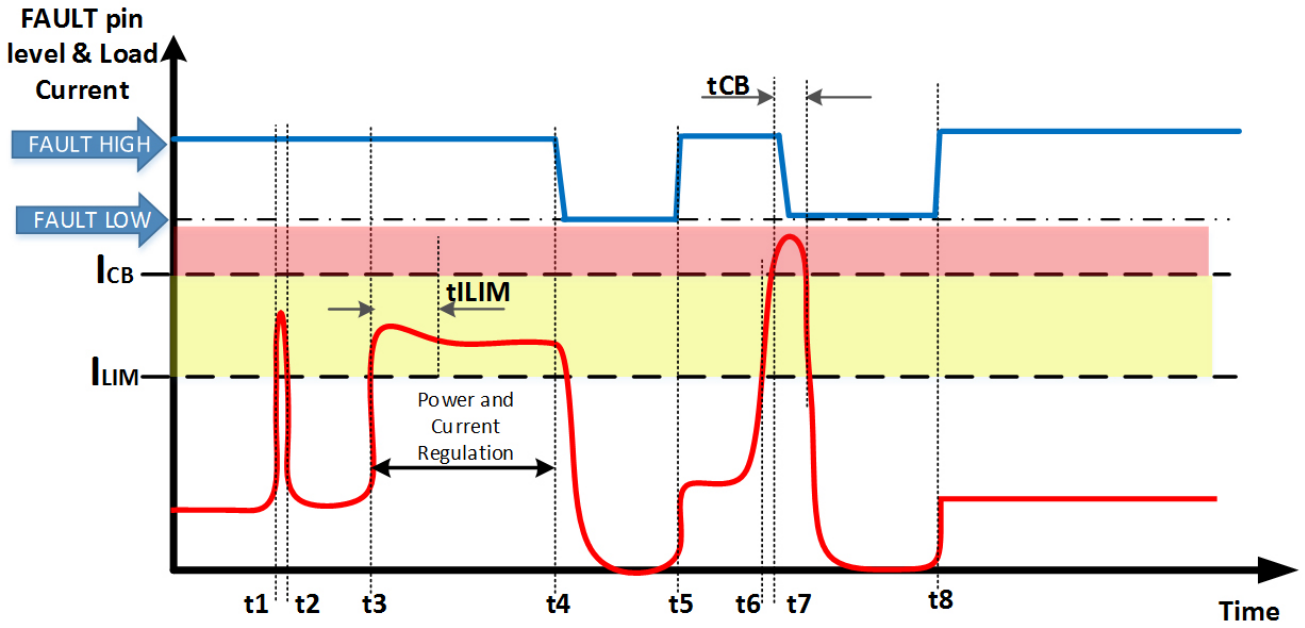
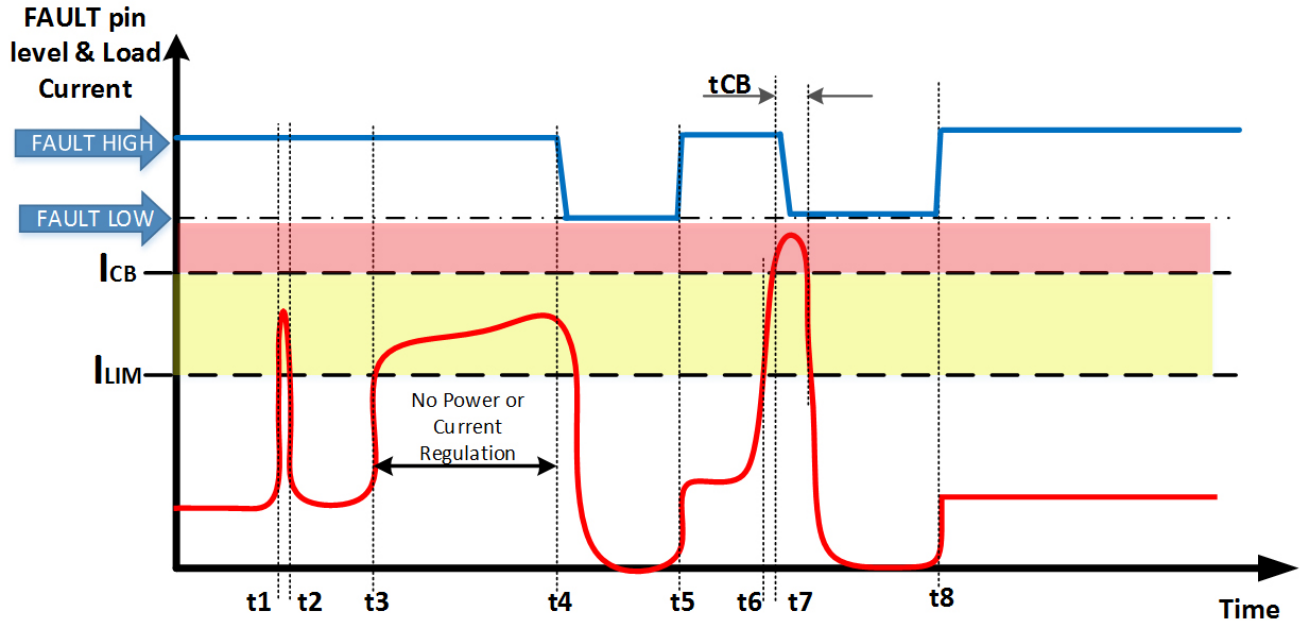


Figure 2. Block Diagram



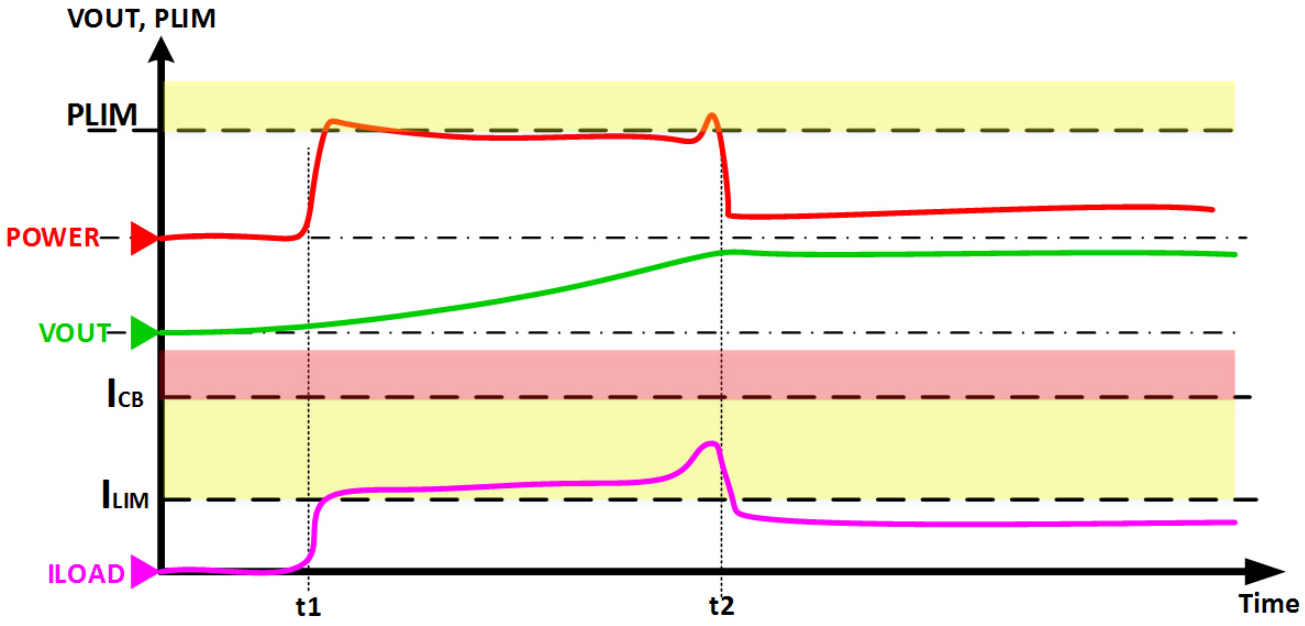
t1: Current above I_{LIM}, FAULT counter started
t2: Current went below I_{LIM} before FAULT reached final count value. FAULT counter cleared, normal operation resumes
t3: Current above I_{LIM}, FAULT counter started. Device regulates current and power delivered to a load.
t4: Device is shut down due to: A) FAULT timer ran out, OR B) Thermal shutdown, OR C) Current reached above ICB. FAULT pin is pulled Low.
t5: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart)
t6: Output short happened (or severe overload)
t7: Current reached ICB level (output short is one reason). The device is immediately shut down within t_{CB} time. FAULT pin pulled low
t8: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto−Restart); normal operation resumed

Figure 3. Power and Current Limit Operation



t1: Current above I_{LIM}, FAULT counter started
t2: Current went below I_{LIM} before tTRIP reached final count value. FAULT counter cleared, normal operation resumes
t3: Current above I_{LIM}, FAULT counter started. Device lets a load to draw as much current as it needs as long as it is below ICB and FET is not overheat
t4: Device is shut down due to: A) FAULT timer ran out, OR B) Thermal shutdown, OR C) Current reached above ICB. FAULT pin is pulled Low.
t5: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto−Restart)
t6: Output short happened (or severe overload)
t7: Current reached ICB level (output short is one reason). The device is immediately shut down within t_{CB} time. FAULT pin pulled low
t8: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart); normal operation resumed

Figure 4. Circuit Breaker Operation



t1: Device enabled into a load and large output capacitance. Load current and Output Voltage start rising. Power/Current limit regulation in Action. FAULT timer is not started during this phase. If Current gets over ICB or if thermal limit of FET reached. The device is shutdown.
t2: VOUT reached the target level. PG is pulled low. Load current settles down. External capacitor charged. At this point the device will be either in Power/Current limiting mode or in Circuit Breaker only mode; depending on the MODE pin selection.

Figure 5. Startup into Capacitive Load

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current, dissipated power in the internal FET and die temperature. On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits and the state of the Enable pin. The output voltage ramp time is controlled by the internal power limit circuit which limits the power dissipated by the conduction FET to the level defined by user through PLIM pin. The device will remain on as long as load current does not exceed the circuit breaker level, enable pin is not driven high or the temperature does not exceed the 175°C limit that is programmed into the chip.

When configured for power and current limiting operation, upon the overcurrent condition the internal power and current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the externally set current limit level as well as limit the power dissipated by the internal FET to the externally set power limit.

When configured for circuit breaker operation the load current and the power dissipated by the internal FET is limited only during the startup; after startup, during normal operation upon the overcurrent event, the load is allowed to draw as much current as it needs as long as it does not exceed the circuit breaker level and internal FET temperature does not exceed 175°C. The device also employs the load current monitoring feature, configurable fault/restart/insertion delay timers, operating mode selection pin, auto−restart/latch behavior selection pin and an indicator pins for power good and fault status.

Operating Mode Selection (MODE pin)

The device offers two overcurrent protection modes: Circuit Breaker operation mode and Power/Current limit operation mode. The desired operation mode is selected using the MODE pin. If MODE pin is grounded or left floating, the device is in power/current limit mode. If the MODE pin is tied to logic High, the device is in circuit breaker mode.

Power and Current Limit Mode

The power and current limit operation mode is selected by connecting the MODE pin to ground or leaving it floating. If the operation mode needs to be changed the device needs to be restarted by removing the input voltage or re−cycling the enable pin.

The current limit circuit uses a reference and amplifier to control the conducted current in the internal FET of the device. The structure allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor. The measured load current is compared to the current limit set by the resistor at the ILIM pin and the set current limit is maintained by the device. The measured load current is also multiplied by the voltage measured across the internal FET's drain and source and the product is compared to the power limit set by the resistor at PLIM pin, thus both the conducted current and power dissipated by the internal FET is limited by the device during an overcurrent event.

Once the load current exceeds the ILIM level the device enters the power and current limit mode and the FAULT timer starts counting. If the measured load current abruptly exceeds the circuit breaker level while the device is in power and current limit mode, for example due to the sudden output short to ground or if the internal FET temperature reaches 175°C the device will shut off the internal FET immediately. The device will shut down the FET also if the FAULT timer reached its value set by the user.

The current limit circuit has a limiting value which is programmed by connecting a resistor from the ILIM pin to GND. The power limit is set by the resistor connected between the PLIM pin and ground. It is recommended to have a 1% or better tolerance resistors for current and power limit programming. The diagram in Figure 3. shows a typical behavior of the device when configured for power and current limit mode.

Circuit Breaker Mode

The circuit breaker mode is selected by connecting the MODE pin to logic high. If the operation mode needs to be changed the device needs to be restarted by removing the input voltage or re−cycling the enable pin.

In this operating mode, the load current is measured by the internal sense circuitry. If the load current is exceeding the ILIM level set by a user the FAULT timer starts counting, however; neither the load current nor the power dissipated by the internal FET is limited. This mode avoids the voltage droop at the output during the overcurrent event and allows the load to draw as much current or power as it needs during the short overcurrent events, however; if the load current exceeds the circuit breaker level, if the FAULT timer runs out or if the internal FET temperature reaches 175°C the device will shut down the internal FET immediately.

The diagram in Figure 4. shows a typical behavior of the device when configured for circuit breaker operation mode.

Startup into Capacitive Load

During the startup, the power and current limit operation mode is active regardless of the MODE pin state. After the startup, when VOUT pin voltage is within 1V of VIN pin voltage and PGOOD pin is pulled low, the mode of operation is selected by the state of the MODE pin. This ensures that the device, even if configured for the latch mode operation, will successfully startup into large capacitive load without shutting down due to the internal FET overheat.

The output voltage ramp time when starting into capacitive load will depend on the power dissipated by the

internal FET and the capacitor energy as well as the current limit setting. The equation to compute the ramp time will be:

$t_{Ramp} = (C_{LOAD} * V_{IN}^2)/(2 * P_{LIM}) + (C_{LOAD} * P_{LIM})/(2 * I_{LIM}^2)$

Where tRamp is time required for output voltage to reach input voltage, C_{LOAD} is output capacitance, V_{IN} is input voltage and P_{LIM} is the limit for the power dissipated in the internal FET.

Overvoltage and Undervoltage Lockout

The overvoltage and undervoltage lockout circuitry monitors the value of the input voltage not to exceed the threshold window set by the user. The threshold window for input voltage is set by connecting three resistors between input terminal, UVLO pin, OVLO pin and ground as shown in Figure 1. With internal threshold voltages for overvoltage and undervoltage – V_{OV} and V_{UV}, user can configure the overvoltage and undervoltage threshold windows using following equations:

$V_{OVLO} = (V_{OV} * R3) / (R1 + R2 + R3)$

$V_{UVLO} = (R2 + R3) * V_{UV} / (R1 + R2 + R3)$

Configurable Timers (TIMER1, TIMER2, TIMER3)

The NIS7080 employs configurable timers for fault timer, auto restart timer and insertion delay timer. The timers are configured externally by connecting the capacitor from TIMERx pin to ground. Each TIMERx pin has an internal current source which starts charging the capacitor connected to that pin once the timer is started. Once the voltage at the TIMERx pin charges up and reaches the internally programmed threshold value, the associated timer resets and generates an event. The larger capacitance connected to TIMERx pin will created larger time delays.

Load Current Monitoring

The current monitor “IMON” pin provides a small current proportional to the main device current which is passing through the internal FET. This pin should have a decoupling capacitor to filter out internal sampling noise. A resistor connected between the IMON pin and GND converts the IMON current into a GND referenced voltage. This pin can be floated if the feature is not required by application.

FAULT Indicator Pin and Fault Timer (TIMER1)

The FAULT pin is an active−low open−drain pin indicating the host system about overcurrent shutdown. The FAULT pin has a fault timer TIMER1 associated with it which starts counting once the load current exceeds the I_{LIM} level. If the timer runs out the internal FET will be turned off and FAULT pin will be pulled low by device indicating the fault condition.

The FAULT pin will be pulled low immediately if internal FET temperature reaches 175°C or if the load current exceeds circuit breaker I_{CB} level.

Enable Pin

The Enable pin is digital active low with internal pull down and provides a digital interface to control the output of the eFuse, without the need of any additional interface logic. When the EN pin is pulled low the device switches to its on state. When the EN pin is driven high, the eFuse output is turned off. All fault conditions will be cleared when the eFuse is reset through the Enable pin.

Power Good Indicator Pin (PGOOD)

The internal monitoring circuitry measures the output and input voltage. As soon as output voltage reaches the input voltage within 1 V threshold margin the PGOOD signal is pulled low indicating the host system about power good state. The pin can be left floating if not used, or pulled to logic high with 10 kΩ resistor.

Auto−Restart Delay (TIMER2)

When device is configured for auto−restart mode and the internal circuitry turned off the FET, the current source on TIMER2 pin starts charging the capacitor connected between TIMER2 pin and ground. Once the voltage on that pin reaches the internally programmed threshold value the device will attempt to turn the internal FET again. Adding larger capacitor to this pin increases the auto−restart time between faults.

Thermal Protection

The NIS7080, NIV7080 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. If the device is configured in latching mode, output power can be restored by either recycling the input power or toggling the enable pin. An auto−retry mode configured device mode will automatically try to restore output power on its own after the TIMER2 runs out. The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 125°C for extended periods of time.

Hot−Plug Insertion Delay (TIMER3)

The device features a hot−plug insertion delay which allows a delay between application of input voltage and time when the voltage on the VOUT pin starts rising. This feature is useful in situations where it is desirable to turn on the output after the input transient of hot−plug settled down. User can control the insertion delay by connecting the capacitor to TIMER3 pin, larger capacitor will increase the delay. Once the voltage at the VIN pin reaches 6 V, the power on reset is active and the TIMER3 current source starts charging the external capacitor; once the capacitor is charged to the internally programmed threshold value the

TIMER3 timer runs out and the internal FET is turned on to bring VOUT pin to the voltage level of VIN.

Latch and Auto−Retry Pin Configuration

This device allows user to configure the latch or auto−retry operation using the RESTART pin. If the RESTART pin is grounded or left floating, the part is configured in auto−restart mode. If the pin is connected to logic High, the part is configured for Latch mode operation. Once the state of the pin is changed the eFuse needs to be restarted either by cycling the input power or toggling the Enable pin.

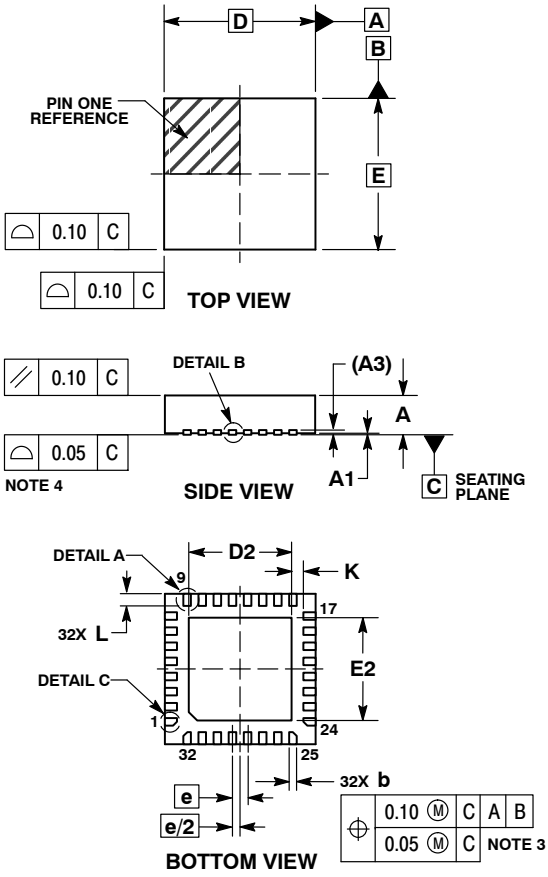
ORDERING INFORMATION

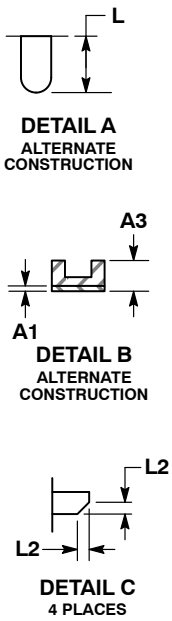
Device	Marking	Package	Shipping †
NIS7080	TBD	WDFNW12, 3x3 mm (Pb – Free)	TBD / Tape & Reel
NIV7080	TBD		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

LQFN32 5x5, 0.5P
CASE 487AA
ISSUE A

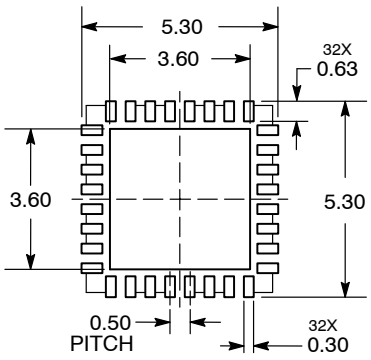




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	1.20	1.40
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.30	3.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L2	0.13 REF	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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