NIS9080, NIV9080

Product Preview

+48 V Electronic Fuse with Gate Driver

The NIS9080 is a cost effective, resettable electronic fuse which is designed to protect the load from overcurrent events, overvoltage conditions, short circuits and other faults. It includes a programmable overvoltage and undervoltage protection, adjustable internal FET power limiting, thermal protection, selectable auto−retry and latch behavior, programmable restart, insertion delay and fault timers, load current monitoring, fault and power good indicator pins and digital enable pin. The NIS9080 is perfectly suitable for typical 48 V operation in various industrial and automotive applications and the input voltage of the device is tolerant to +80 V. In addition to the internal FET for conducting current, NIS9080 also incorporates a gate driver for controlling the external FET.

Features

- Internal FET with 55 mΩ Typical Rds(ON)
- Gate Driver for External FET
- PMBus Digital Interface
- Remote Temperature Sensing
- Programmable Overvoltage and Undervoltage Protection
- Active−Low Open−Drain Power Good Indicator
- Active−Low Open−Drain FAULT Pin Indicator
- Pin Selectable Auto−Restart/Latch Operation Mode
- Pin Selectable Circuit Breaker Operation Mode
- Adjustable Output Current Limit Protection
- Adjustable Power Limiting for Internal FET
- Adjustable FAULT Pin Timer
- Adjustable Restart Timer for Auto−Restart Mode Operation
- Adjustable Hot−Plug Insertion Delay
- Integrated Current Monitoring
- Digital Active−Low Enable Pin
- NIV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Automotive
- Telecom
- Industrial

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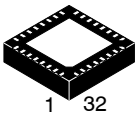
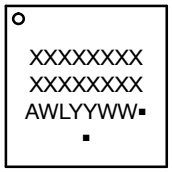


LQFN32
5 x 5
CASE 487AA

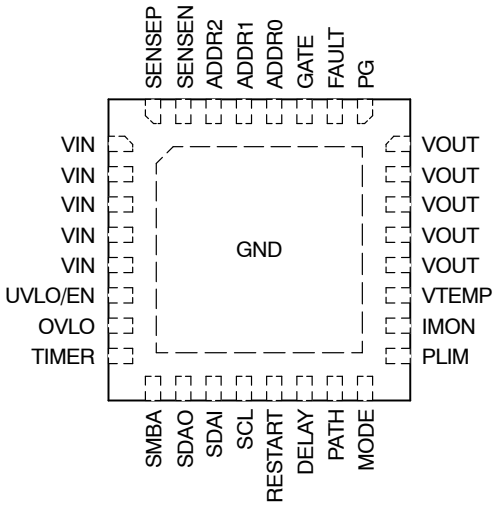
MARKING DIAGRAM



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Function	Description
1,2,3,4,5	VIN	Input Voltage
6	UVLO/EN	Undervoltage Lockout adjustment and Enable pin
7	OVLO	Overvoltage Lockout adjustment pin
8	TIMER	Fault Timer (Connect capacitor to ground for fault timer configuration)
9	SMBA	PMBus Alert line
10	SDAO	PMBus data output pin
11	SDAI	PMBUs data input pin
12	SCL	PMBus clock
13	RESTART	Auto−Retry / Latch operation. If tied High, the Latch mode is on. If grounded or floated the Auto−Retry mode is on. Connecting external capacitor to ground from this pin ensures Auto−Retry mode with restart delay dependent on capacitor value.
14	DELAY	Adding capacitor to ground from this pin defines insertion time delay. Tying Low, leaving floating or tying High removes the delay − no delay added to start the FET.
15	PATH	Power Path selection. Tie High for external FET, tie low or leave floating for internal channel FET.
16	MODE	Capacitive precharging mode selection. Tie High for capacitive precharge mode selection. Tie low or leave floating if not using this feature.
17	PLIM	Power Limit Resistor pin
18	IMON	Current Monitoring Resistor connection pin
19	VTEMP	Remote Temperature Sensing Pin
20,21,22,23,24	VOUT	Output Voltage
25	PG	Power Good Pin (Open Drain)
26	FAULT	FAULT pin (Open Drain)
27	GATE	Gate Control Pin
28	ADDR0	PMBus address selection line
29	ADDR1	PMBus address selection line
30	ADDR2	PMBus address selection line
31	SENSEN	RSENSE Kelvin sensing pin Negative
32	SENSEP	RSENSE Kelvin sensing pin Positive
33 (Pad)	Ground	Ground connection

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT Pin Input Voltage to GND, operating, steady−state (Note 1)	$V_{IN/OUT}$	−0.6 to +80	V
All Other pins	Vpin	−0.6 to 5.5	V
Thermal Resistance, Junction−to−Air 0.1 in² copper (Note 2) 0.5 in² copper (Note 2)	θ_{JA}	 TBD TBD	°C/W
Thermal Resistance, Junction−to−Lead	θ_{JL}	TBD	°C/W
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_{MAX}	TBD TBD	W mW/°C
Operating Temperature Range (Note 3)	T_J	−40 to 125	°C
Non−operating Temperature Range	T_J	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.
2. 1 oz copper, double−sided FR4.
3. Thermal limit is set above the maximum thermal rating. It is not recommended to operate this device at temperatures greater than maximum ratings for extended periods of time.

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
ON Resistance, T_J = 25°C	$R_{ds(ON)}$		55		mΩ
ON Resistance, T_J = 85°C			TBD		
Continuous Current (T_A = 25°C, 0.5 sq in pad)	I_d		8		A
Off State Leakage (V_{IN} = 48 V, V_{EN} = 5 V, T_A = 25°C)	I_{off}		1		μA
GATE DRIVER					
Total Gate Charge of External FET(s)	$Q_{G(Tot)}$		TBD		nC
Gate Turn On Time (V_{GS} = 0.5 V to V_{GS} = 12 V)	$t_{Gate(On)}$			TBD	μs
Gate Turn Off Time (Transition of V_{GS} to < 0.5 V)	$t_{Gate(Off)}$			TBD	μs
Gate to source for External FET (V_{GS} while On)	$V_{GS(On)}$	12		15	V
Gate to source for External FET (V_{GS} while Off)	$V_{GS(Off)}$			0.4	V
Gate Voltage UVLO	$V_{GS(UVLO)}$	10			V
Gate Voltage UVLO trip time	$V_{GS(UVLO-BLANK)}$			100	μs
External FET Turn−On value at output (Default value, External Mode with Precharge)	$V_{OUTPRCHRG}$		$2xV_{UVLO}$	$V_{IN(Max)}$	V
THERMAL SHUTDOWN					
Shutdown Temperature	T_{SD}		175		°C
Thermal Hysteresis (Auto−Restart Mode only)	T_{HYST}		20		°C
Thermal swing shutdown threshold	TSW		60		°C
REMOTE TEMPERATURE SENSING					
VTEMP Pin Current High Level	$V_{TEMP(IHigh)}$		TBD		μA
VTEMP Pin Current Low Level	$V_{TEMP(ILow)}$		TBD		μA
VTEMP Pin Temperature Sensing accuracy	$V_{TEMP(acc)}$		10		°C
VTEMP Pin Current Pulse rate	$V_{TEMP(rate)}$		1		kHz
VTEMP Pin shutdown temperature threshold	$V_{TEMP(th)}$		140		°C
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout	V_{UVLO}		Adj.		V
Undervoltage Lockout Default Value (No R1,R2,R3 connected)	V_{UVLO}		8		V
Undervoltage Lockout Threshold value	V_{UV}		TBD		V
Undervoltage Lockout Hysteresis	$V_{(UVLO)Hyst}$		0.1		V
Undervoltage Lockout Response Time	t_{UVLO}		5		μs
Power On Reset Threshold voltage	V_{POR}		6		V
Power On Reset Threshold voltage Hysteresis	$V_{POR(Hyst)}$		0.1		V
OVERVOLTAGE LOCKOUT					
Overvoltage Lockout	V_{OVLO}		Adj.		V
Overvoltage Lockout Threshold value	V_{OV}		TBD		V
Overvoltage Lockout Hysteresis	$V_{(OVLO)Hyst}$		0.1		V
Output Clamping Voltage Response Time	t_{OVLO}		5		μs
FORWARD CURRENT LIMIT					
Current Limit (R_{LIM} = TBD)	I_{LIM}		Adj.		A
Circuit Breaker Level	I_{CB}		1.5 x I_{LIM}		A
Current Limit Response Time	t_{ILIM}		10		μs

Table 3. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
FORWARD CURRENT LIMIT					
Circuit Breaker Response Time	t_{CB}		1		μs
POWER LIMIT					
Internal FET Power Limit Threshold (R_{PLIM} = TBD)	P_{LIMTH}		Adj.		W
Power Limit Threshold Current	I_{PLIM}		TBD		μA
LOGIC INPUT/OUTPUT					
Logic Level Low (Digital Pins)	$V_{IL(EN)}$			0.8	V
Logic Level High (Digital Pins)	$V_{IH(EN)}$	2			V
Output Voltage Low (FAULT, PGOOD and Digital Pins)	V_{OL}			0.3	V
Output Voltage High (Digital Pins)	V_{OH}	3			V
Logic High Sink Current (FAULT, PGOOD pins)	I_O		0.5		mA
POWER GOOD					
Power Good VIN−VOUT threshold voltage	$V_{PGOOD(Th)}$		1		V
TIMER CONTROL					
Timer Pin Threshold voltage, TIMER, DELAY, RESTART pins	$V_{TIMER(Th)}$		4		V
Timer Pin Current Source value	I_{TIMER}		TBD		μA
Auto−Retry timeout			100		ms
LOAD CURRENT MONITORING					
Load Monitor Sense Current (R_{IMON} = TBD)	I_{SENSE}		1		mA/A
Current Sense Measurement Error	$I_{SENSE(Err)}$		10		%
SUPPLY CURRENT					
Bias Current Operational (V_{IN} = 48 V, V_{EN} = 0 V)	$I_{BIAS(ON)}$		TBD		μA
Bias Current Shutdown (V_{IN} = 48 V, V_{EN} = 5 V)	$I_{BIAS(OFF)}$		TBD		μA
ESD CHARACTERISTICS					
Human Body Model (All pins)	ESD−HBM		±2		kV
Charged Device Model (All pins)	ESD−CDM		500		V
IEC61000−4−2 (V_{IN}, V_{OUT} pins	IEC		4		kV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. AUTOMOTIVE PROTECTION FEATURES

Protection	Min	Typ	Max	Unit	Test Conditions
AUTOMOTIVE PROTECTION FEATURES (NIV9080)					
Ground Loss Disable time	5			μs	Resistor from GND pin to Ground goes from 100 mΩ to 1MΩ
ISO7637−2	−300			V	Pulse 1, 500 pulses
	112			V	Pulse 2a, 500 pulses
	20			V	Pulse 2b, 10 pulses
	−200			V	Pulse 3a, 1 hour
	200			V	Pulse 3b, 1 hour
ISO16750−2	40			V	Test B, U_N = 24 V
ISO7637−3	112			V	Pulse 2a, Level IV
	−150			V	Pulse 3a, Level IV
	150			V	Pulse 3b, Level IV
JESD78	−100		+100	mA	Class II
IEC−61967−4			80 (150−300 kHz) 58 (0.5−2 MHz) 50 (5−10 MHz) 40 (10−100 MHz) 30 (100−300 MHz)	dBμV	V_{IN}=13.5 V/1 A 150 Ω method
IEC 62132−4 ISO 11452−7	35 (1−110MHz) 24 (110−1000MHz)			dBm	V_{IN}=13.5 V F = 1−1000 MHz CW, AM (1 kHz, 80%)

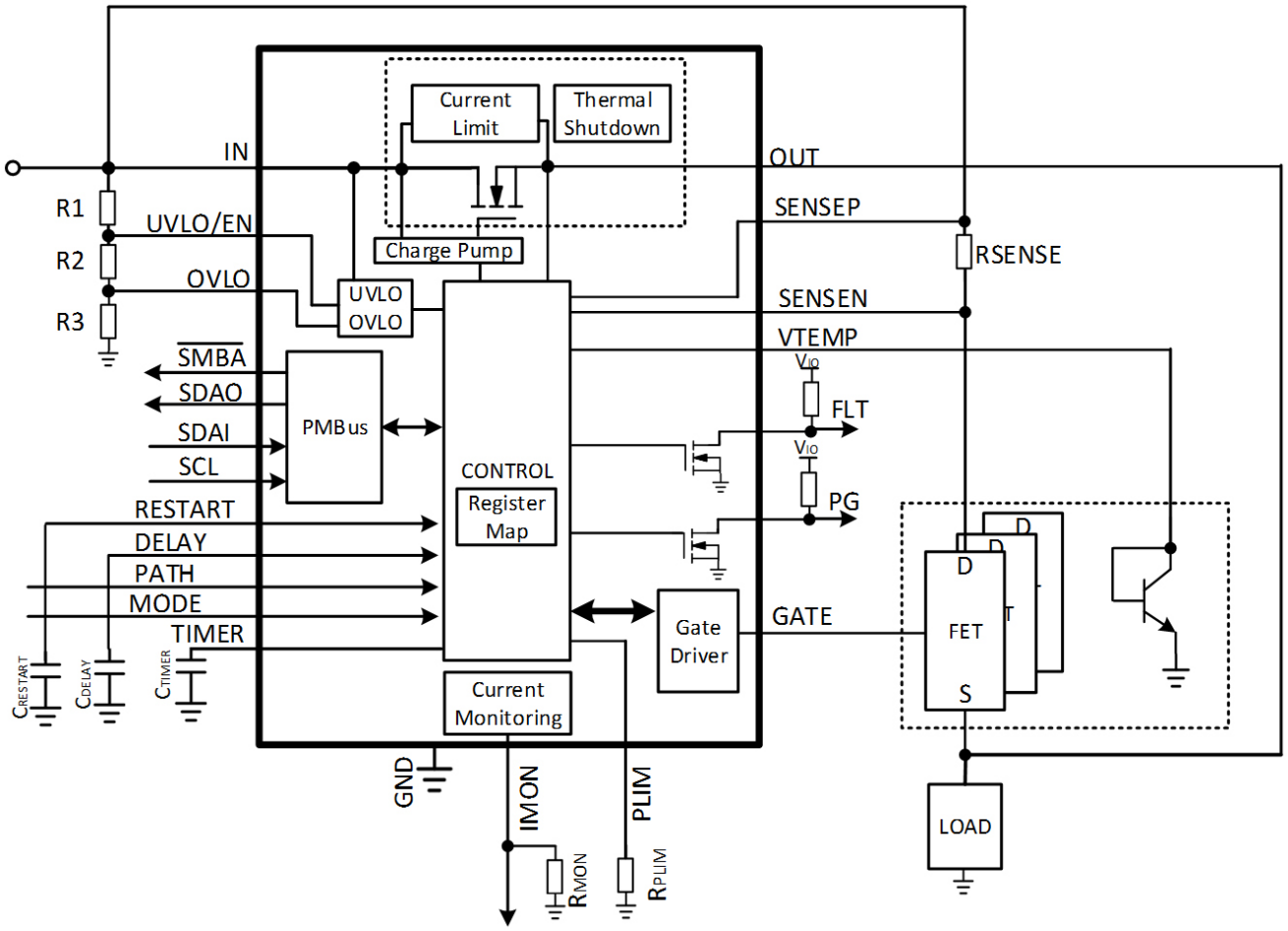
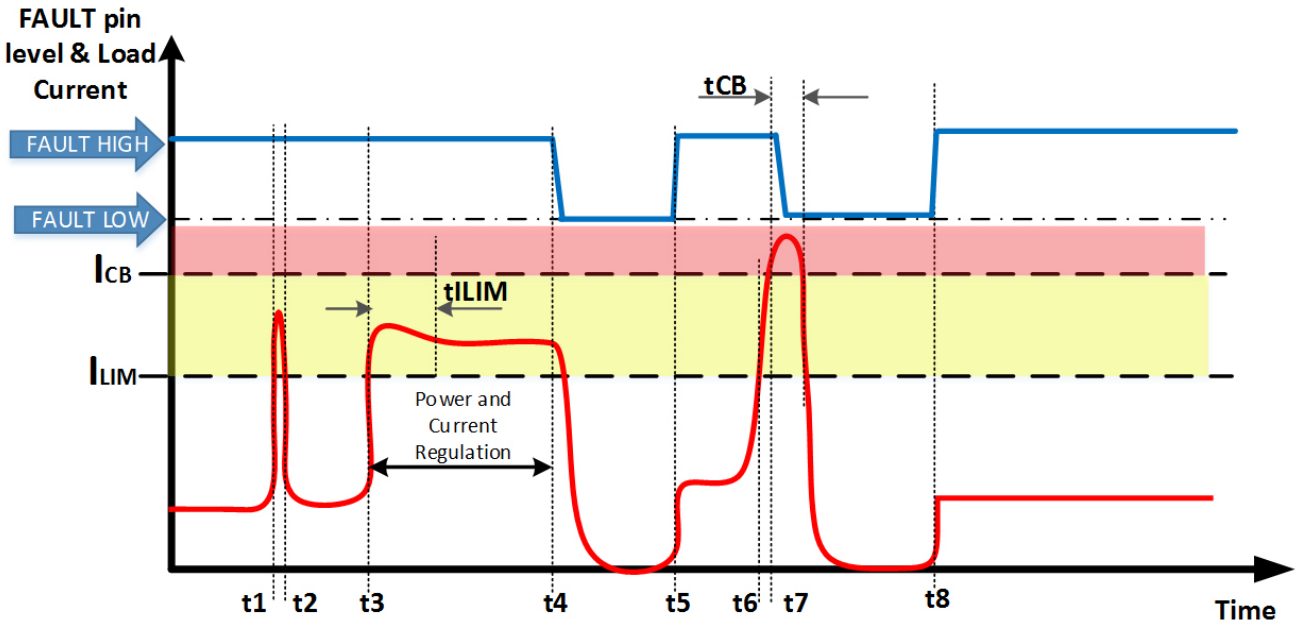
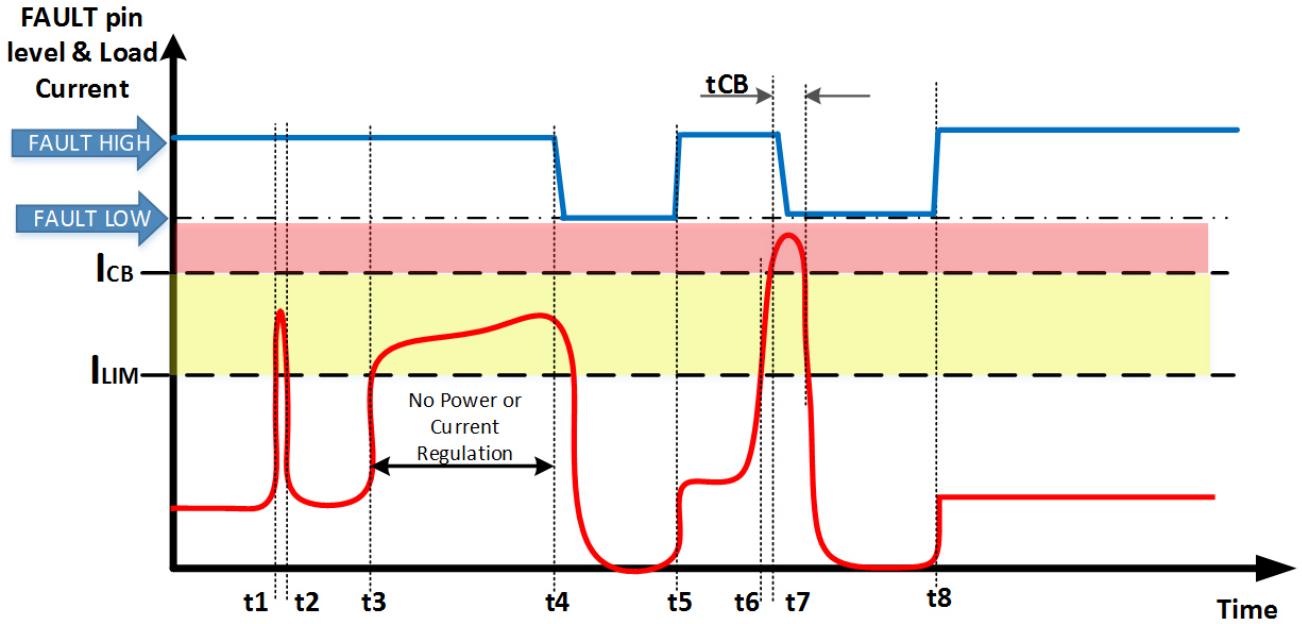


Figure 1. Typical Application and Block Diagram



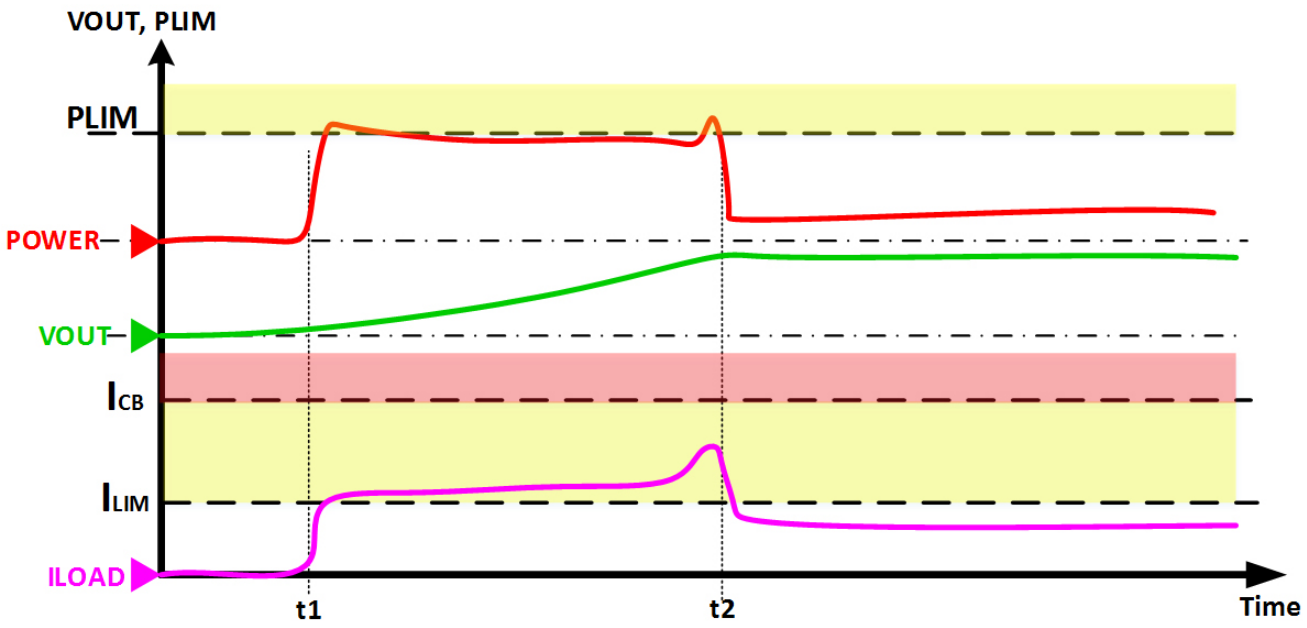
t1: Current above ILIM, FAULT counter started
t2: Current went below ILIM before FAULT reached final count value. FAULT counter cleared, normal operation resumes
t3: Current above ILIM, FAULT counter started. **Device regulates current and power delivered to a load.**
t4: Device is shut down due to: A) FAULT timer ran out, OR B) Thermal shutdown, OR C) Current reached above ICB. FAULT pin is pulled Low.
t5: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart)
t6: Output short happened (or severe overload)
t7: Current reached ICB level (output short is one reason). The device is immediately shut down within tCB time. FAULT pin pulled low
t8: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart); normal operation resumed

Figure 2. Power and Current Limit Operation (Internal Mode or External Mode)



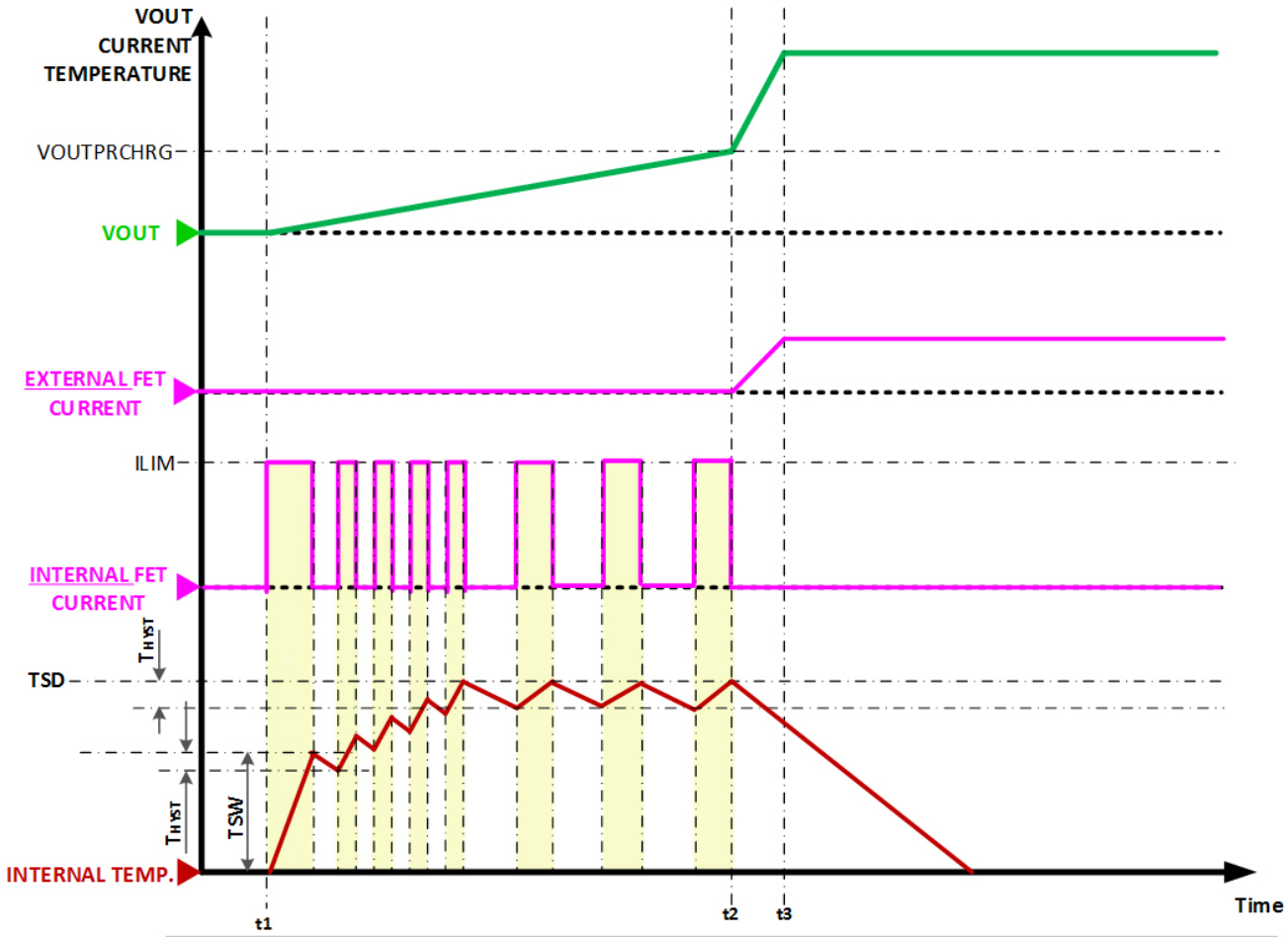
t1: Current above ILIM, FAULT counter started
t2: Current went below ILIM before tTRIP reached final count value. FAULT counter cleared, normal operation resumes
t3: Current above ILIM, FAULT counter started. Device lets a load to draw as much current as it needs **as long as** it is below ICB and FET is not overheat
t4: Device is shut down due to: A) FAULT timer ran out, OR B) Thermal shutdown, OR C) Current reached above ICB. FAULT pin is pulled Low.
t5: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart)
t6: Output short happened (or severe overload)
t7: Current reached ICB level (output short is one reason). The device is immediately shut down within tCB time. FAULT pin pulled low
t8: FET temperature reduced by 40°C, device restarted manually or restart timer ran out (If configured to Auto-Restart); normal operation resumed

Figure 3. Circuit Breaker Operation (Internal Mode Only)



t1: Device enabled into a load and large output capacitance. Load current and Output Voltage start rising. Power/Current limit regulation in Action. FAULT timer is not started during this phase. If Current gets over ICB or if thermal limit of FET reached. The device is shutdown.
t2: VOUT reached the target level. PG is pulled low. Load current settles down. External capacitor charged. At this point the device will be either in Power/Current limiting mode or in Circuit Breaker only mode; depending on the MODE pin selection.

Figure 4. Startup into Capacitive Load (Internal or External Power Path, No Precharging)



t1: device enabled into highly capacitive load. Internal FET works in auto-retry mode with thermal shutdown. VOUT is gradually rising.
t2: VOUT reached VOUTPRCHRG voltage level. Internal FET is turned off. Gate driver turns On external FET. VOUT now rises rapidly to a target voltage
t3: VOUT reached target level within VIN.

Figure 5. Capacitive Load Output Precharging (External Power Path with Precharging)

Table 5. DEVICE OPERATING MODES AND POWER PATH SELECTION

Power Path Configuration	Path	Mode
External	High	Low
External with Precharging	High	High
Internal (Power and Current Limit)	Low	Low
Internal (Circuit Breaker)	Low	High

Table 6. DEVICE SETTINGS ACCESSIBLE THROUGH PMBus INTERFACE

Parameter	Read	Write	Configurable Externally?*	External Setting has Priority?**	PMBus Alert?***
Input Voltage	•				
Output Voltage	•				
Current through internal FET	•				
Current measured through external FET	•				
Internal FET temperature	•				•
Temperature measured with external BJT sensor	•				•
Internal FET On Slew Rate	•	•			
Internal FET shutdown time	•	•			
Current Limit Setting for internal FET	•	•			
Power Limit setting for external FET	•	•	•	•	•
Current Limit, ILIM	•	•			
Circuit Breaker Current Limit, ICB	•	•			
Timer delay, FAULT timer configuration	•	•	•	•	
RESTART pin / Timer configurable	•	•	•	•	
Insertion delay pin / Timer configurable	•	•	•	•	
PATH pin configurable	•	•	•	•	
MODE pin configurable	•	•	•	•	
UVLO outside range bit	•				
OVLO outside range bit	•				
BIST: Gate Driver good	•				
BIST: Charge Pump good	•				
BIST: Fault Logic Good	•				
BIST: FET Check OK	•				
BIST: Current Monitor Good	•				
Sleep Mode On	•	•			
FAULT Bit	•				•
PGOOD Bit	•				
Auto−Retry timeout	•	•			

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current, dissipated power in the internal FET and die temperature. On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits and the state of the Enable pin. The output voltage ramp time is controlled by the internal power limit circuit which limits the power dissipated by the conduction FET to the level defined by user through PLIM pin. The device will remain on as long as load current does not exceed the circuit breaker level, enable pin is not driven high or the temperature does not exceed the 175°C limit that is programmed into the chip.

When configured for power and current limiting operation, upon the overcurrent condition the internal power and current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the externally set current limit level as well as limit the power dissipated by the internal FET to the externally set power limit.

When configured for circuit breaker operation the load current and the power dissipated by the internal FET is limited only during the startup; after startup, during normal operation upon the overcurrent event, the load is allowed to draw as much current as it needs as long as it does not exceed the circuit breaker level and internal FET temperature does not exceed 175°C. The device also employs a gate driver for controlling the external FETs in high current applications.

Operating Mode Selection

The device offers various operating modes both with internal and external power path. Refer to Table 5 for information on setting the desired mode of operation as well as power path selection.

When configured for internal power path, the device offers two overcurrent protection modes: Circuit Breaker operation mode and Power/Current limit operation mode.

When external power path is selected, only power and current limit operation mode is available. In that case, power and current limit is programmed for an external FET. When external power path is selected with precharging feature, power and current limit mode is active only after the output voltage is precharged to a specific value VOUTPRCHRG, until that, the internal FET is conducting current in auto−restart mode.

Power and Current Limit Mode

The current limit circuit uses a reference and amplifier to control the conducted current in the internal FET of the device. The structure allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor. The measured load current is compared to the current limit set by the resistor at the ILIM pin and the set current limit is maintained by the device. The measured load current is also multiplied by the voltage measured across the internal FET's drain and source and the product is compared to the power limit set by the resistor at PLIM pin, thus both the conducted current and power dissipated by the internal FET is limited by the device during an overcurrent event.

Once the load current exceeds the ILIM level the device enters the power and current limit mode and the FAULT timer starts counting. If the measured load current abruptly exceeds the circuit breaker level while the device is in power and current limit mode, for example due to the sudden output short to ground or if the internal FET temperature reaches 175°C the device will shut off the internal FET immediately. The device will shut down the FET also if the FAULT timer reached its value set by the user.

The current limit circuit has a limiting value which is programmed by connecting a resistor from the ILIM pin to GND. The power limit is set by the resistor connected between the PLIM pin and ground. It is recommended to have a 1% or better tolerance resistors for current and power limit programming. The diagram in Figure 3. shows a typical behavior of the device when configured for power and current limit mode.

Circuit Breaker Mode

In this operating mode, the load current is measured by the internal sense circuitry. If the load current is exceeding the ILIM level set by a user the FAULT timer starts counting, however; neither the load current nor the power dissipated by the internal FET is limited. This mode avoids the voltage droop at the output during the overcurrent event and allows the load to draw as much current or power as it needs during the short overcurrent events, however; if the load current exceeds the circuit breaker level, if the FAULT timer runs out or if the internal FET temperature reaches 175°C the device will shut down the internal FET immediately.

The diagram in Figure 4. shows a typical behavior of the device when configured for circuit breaker operation mode. This mode is available only when the device is configured for Internal Power path.

Startup into Capacitive Load with Power Limit Feature

During the startup, the power and current limit operation mode is active regardless of the MODE pin state. After the startup, when VOUT pin voltage is within 1V of VIN pin voltage and PGOOD pin is pulled low, the mode of operation is selected by the state of the MODE pin. This ensures that the device, even if configured for the latch mode operation, will successfully startup into large capacitive load without shutting down due to the internal FET overheat.

The output voltage ramp time when starting into capacitive load will depend on the power dissipated by the internal FET and the capacitor energy as well as the current limit setting. The equation to compute the ramp time will be:

$tRamp = (C_{LOAD} * V_{IN}^2)/(2 * P_{LIM}) + (C_{LOAD} * P_{LIM})/(2 * I_{LIM}^2)$

Where tRamp is time required for output voltage to reach input voltage, C_{LOAD} is output capacitance, V_{IN} is input voltage and P_{LIM} is the limit for the power dissipated in the internal FET. Same conditions also apply when the external FET is used for power path.

Startup into Capacitive Load with Precharging (External Power Path)

If the device is configured for external power path with precharging feature as shown with appropriate settings in Table 5, then upon enabling only the internal FET is conducting current in auto retry mode, as soon as the output reaches VOUTPRCHRG voltage level the internal FET is turned off and the gate driver turns on the external FET. This allows to minimize the inrush current from large capacitive load while at the same time reach the target output voltage as soon as possible. In this mode the internal FET is working in auto retry mode, where it is conducting current but as soon as it overheats the FET shuts down until its temperature is not cooled down by 40°C, once the temperature is reduced internal FET again turns on and precharges the output voltage to the value of the input voltage. Typical diagram of output precharging to VIN level in this mode is shown in Figure 6.

Overvoltage and Undervoltage Lockout

The overvoltage and undervoltage lockout circuitry monitors the value of the input voltage not to exceed the threshold window set by the user. The threshold window for input voltage is set by connecting three resistors between input terminal, UVLO pin, OVLO pin and ground as shown in Figure 1. With internal threshold voltages for overvoltage and undervoltage – V_{OV} and V_{UV}, user can configure the overvoltage and undervoltage threshold windows using following equations:

$V_{OVLO} = (V_{OV} * R3) / (R1 + R2 + R3)$

$V_{UVLO} = (R2 + R3) * V_{UV} / (R1 + R2 + R3)$

Additionally, user can disable the device by shoring EN/UVLO pin to ground using open drain external driver.

Auto−Retry Control (RESTART pin)

The NIS9080 allows to control the Auto−Retry behavior in a required by application way. If the RESTART pin is tied to logic High, the device is operating in latch mode – upon fault event, the device is disabled and needs to be power−cycled or re−enabled manually by user. If the RESTART pin is grounded, the device is working in auto−retry mode, where upon a failure the device is making an attempt to restart the power FET (both internal or external depending on the setup). Connecting a capacitor to ground from this pin allows user to control the auto retry time after the fault occurred.

An Auto−Retry timeout feature ensures that in a case of the permanent output to ground short the device stops auto restarting after predetermined default amount of time which can also be adjusted through the digital interface

Load Current Monitoring

The current monitor “IMON” pin provides a small current proportional to the main device current which is passing through the internal FET. This pin should have a decoupling capacitor to filter out internal sampling noise. A resistor connected between the IMON pin and GND converts the IMON current into a GND referenced voltage. This pin can be floated if the feature is not required by application.

FAULT Indicator Pin and Fault Timer (TIMER pin)

The FAULT pin is an active−low open−drain pin indicating the host system about overcurrent shutdown. The FAULT pin has a fault timer TIMER pin associated with it which starts counting once the load current exceeds the I_{LIM} level. If the timer runs out the internal FET will be turned off and FAULT pin will be pulled low by device indicating the fault condition.

The FAULT pin will be pulled low immediately if internal FET temperature reaches 175°C or if the load current exceeds circuit breaker I_{CB} level.

Power Good Indicator Pin (PGOOD)

The internal monitoring circuitry measures the output and input voltage. As soon as output voltage reaches the input voltage within 1 V threshold margin the PGOOD signal is pulled low indicating the host system about power good state. The pin can be left floating if not used, or pulled to logic high with 10 kOhm resistor.

Remote Temperature Sensing

The device also features a remote temperature sensing feature, where user can connect external diode connected BJT to the VTEMP pin. The VTEMP pin sends high and low current pulses every 1 ms and the voltage developed on that pin due to this current pulse is proportional to the temperature experienced by the external BJT. The external BJT should be placed in the vicinity of the external power FETs conducting current for precise accurate external FET temperature sensing.

Internal Thermal Protection

The NIS9080, NIV9080 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. If the device is configured in latching mode, output power can be restored by either recycling the input power or toggling the enable pin. An auto−retry mode configured device mode will automatically try to restore output power on its own after the TIMER2 runs out. The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 125°C for extended periods of time.

The device also monitors the thermal difference between the internal FET and the circuit in the control die. If that thermal difference exceeds the TSW value the internal FET is turned off and restrted after the difference is decreased by THYST value.

Hot−Plug Insertion Delay (DELAY pin)

The device features a hot−plug insertion delay which allows a delay between application of input voltage and time when the voltage on the VOUT pin starts rising. This feature is useful in situations where it is desirable to turn on the output after the input transient of hot−plug settled down. User can control the insertion delay by connecting the capacitor to DELAY pin, larger capacitor will increase the delay. Once the voltage at the VIN pin reaches 6 V, the power on reset is active and the DELAY pin current source starts charging the external capacitor; once the capacitor is charged to the internally programmed threshold value the DELAY timer runs out and the internal device is turned on to bring VOUT pin to the voltage level of VIN.

PMBus Digital Interface

The device features a standardized PMBus interface for digital communication. User can read and write configuration data through the internal register map. The measurements of power/voltage/current are being read in 12−bit 2's complement binary format. All internal measurements of power/current are normalized to a 200 μΩ RSNS resistor value; that can be further scaled/calibrated by a host system/user for other environment and other values of sense resistor. Refer to Table 6. for information on programmable/readable parameters of the device through digital interface.

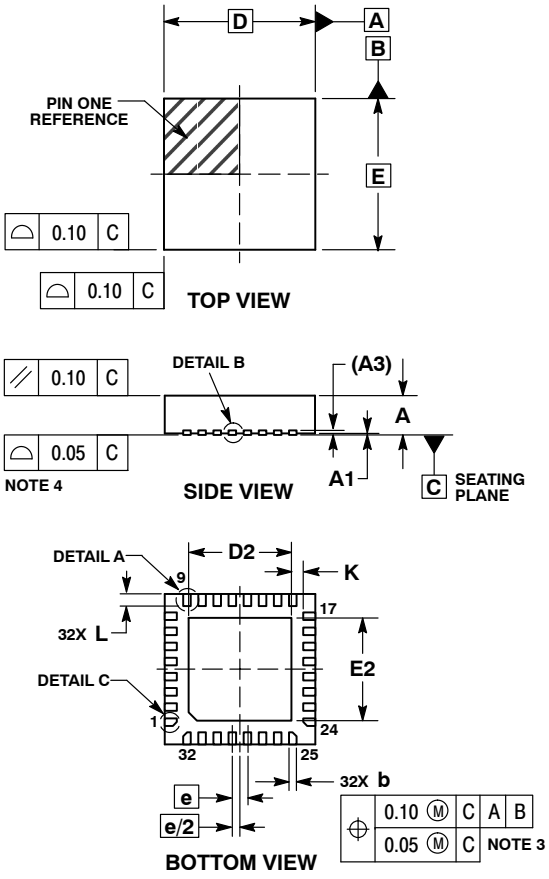
ORDERING INFORMATION

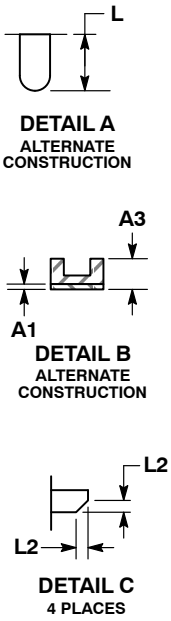
Device	Marking	Package	Shipping†
NIS9080	TBD	LQFN32, 5x5 mm (Pb−Free)	TBD / Tape & Reel
NIV9080	TBD		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

LQFN32 5x5, 0.5P
CASE 487AA
ISSUE A

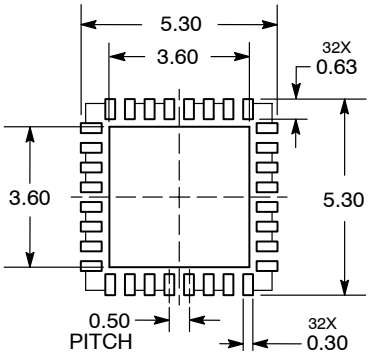




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	1.20	1.40
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.30	3.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L2	0.13 REF	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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