

NL17SZ04E

Single Inverter

The NL17SZ04E is an inverter in three tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

Features

- Tiny SOT-353 Package
- 24 mA Sink and Source Output Capability
- Over-Voltage Tolerant Inputs and Outputs
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

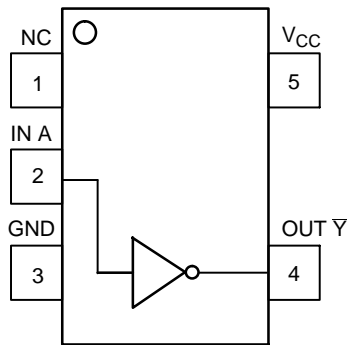


Figure 1. Pinout (Top View)

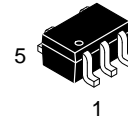


Figure 2. Logic Symbol



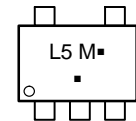
ON Semiconductor®

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SOT-353/SC70-5/SC-88A
DF SUFFIX
CASE 419A

MARKING DIAGRAMS



L5 = Specific Device Marking

M = Date Code*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	NC
2	IN A
3	GND
4	OUT Y
5	V _{CC}

FUNCTION TABLE

Input	Output
A	Y
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage	-0.5 to +6.5	V
V_O	DC Output Voltage Active Mode, High or Low State (Note 1) Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	-50	mA
I_O	DC Output Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$
T_J	Junction Temperature Under Bias	+150	$^{\circ}C$
θ_{JA}	Thermal Resistance (Note 2)	350	$^{\circ}C/W$
P_D	Power Dissipation in Still Air at 85 $^{\circ}C$	186	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
ESD	ESD Classification Human Body Model (Note 3) Charged Device Model (Note 4)	4000 1000	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125 $^{\circ}C$ (Note 5)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	Operating 1.65 Data Retention 1.5	5.5 5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage	(High or Low State) 0 ($V_{CC} = 0\text{ V}$)	V_{CC} 5.5	V
V_{OUT}	DC Output Voltage (SOT-953 Package)	(High or Low State)	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ $V_{CC} = 3.0\text{ V} \pm 0.3\text{ V}$ $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95 2.3 to 5.5	$0.75 V_{CC}$ $0.7 V_{CC}$			$0.75 V_{CC}$ $0.7 V_{CC}$		V
V_{IL}	Low-Level Input Voltage		1.65 to 1.95 2.3 to 5.5			$0.25 V_{CC}$ $0.3 V_{CC}$		$0.25 V_{CC}$ $0.3 V_{CC}$	V
V_{OH}	High-Level Output Voltage $V_{IN} = V_{IL}$	$I_{OH} = -100\ \mu\text{A}$	1.65 to 5.5	$V_{CC} - 0.1$	V_{CC}		$V_{CC} - 0.1$		V
		$I_{OH} = -4\ \text{mA}$	1.65	1.29	1.52		1.29		
		$I_{OH} = -8\ \text{mA}$	2.3	1.9	2.1		1.9		
		$I_{OH} = -12\ \text{mA}$	2.7	2.2	2.4		2.2		
		$I_{OH} = -16\ \text{mA}$	3.0	2.4	2.7		2.4		
		$I_{OH} = -24\ \text{mA}$	3.0	2.3	2.5		2.3		
		$I_{OH} = -32\ \text{mA}$	4.5	3.8	4.0		3.8		
V_{OL}	Low-Level Output Voltage $V_{IN} = V_{IH}$	$I_{OL} = 100\ \mu\text{A}$	1.65 to 5.5		0.0	0.1		0.1	V
		$I_{OH} = 4\ \text{mA}$	1.65		0.08	0.24		0.24	
		$I_{OL} = 8\ \text{mA}$	2.3		0.20	0.3		0.3	
		$I_{OL} = 12\ \text{mA}$	2.7		0.22	0.4		0.4	
		$I_{OL} = 16\ \text{mA}$	3.0		0.28	0.4		0.4	
		$I_{OL} = 24\ \text{mA}$	3.0		0.38	0.55		0.55	
		$I_{OL} = 32\ \text{mA}$	4.5		0.42	0.55		0.55	
I_{IN}	Input Leakage Current	$V_{IN} = 5.5\ \text{V}$ or GND	1.65 to 5.5		± 0.1			± 1.0	μA
I_{OFF}	Power Off Leakage Current	$V_{IN} = 5.5\ \text{V}$ or $V_{OUT} = 5.5\ \text{V}$	0			1		10	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = 5.5\ \text{V}$ or GND	5.5			1		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS $t_R = t_F = 2.5$ ns

Symbol	Parameter	Condition	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 and 4)	$R_L = 1\text{ M}\Omega, C_L = 15\text{ pF}$	1.65 1.8		5.3 4.4	11.4 9.5		12.0 10.0	ns
		$R_L = 1\text{ M}\Omega, C_L = 15\text{ pF}$	2.5 ± 0.2		3.5	6.5		7.0	
		$R_L = 1\text{ M}\Omega, C_L = 15\text{ pF}$	3.3 ± 0.3		2.1	4.5		4.7	
		$R_L = 500\ \Omega, C_L = 50\text{ pF}$			2.9	5.5		5.2	
		$R_L = 1\text{ M}\Omega, C_L = 15\text{ pF}$	5.0 ± 0.5		1.8	3.9		4.1	
		$R_L = 500\ \Omega, C_L = 50\text{ pF}$			2.4	4.3		4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{ V}, V_I = 0\text{ V or }V_{CC}$	> 2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, $V_{CC} = 3.3\text{ V}, V_I = 0\text{ V or }V_{CC}$ 10 MHz, $V_{CC} = 5.5\text{ V}, V_I = 0\text{ V or }V_{CC}$	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

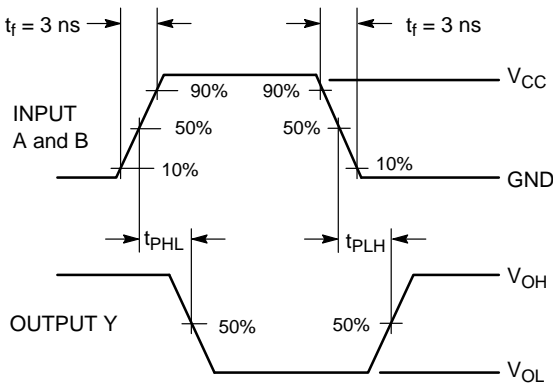


Figure 3. Switching Waveform

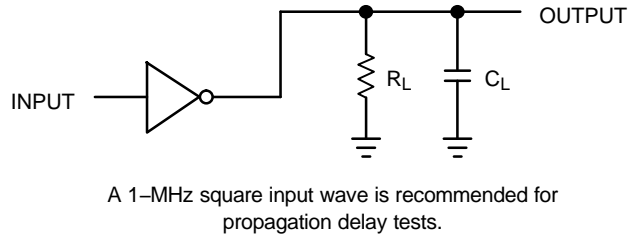


Figure 4. Test Circuit

ORDERING INFORMATION

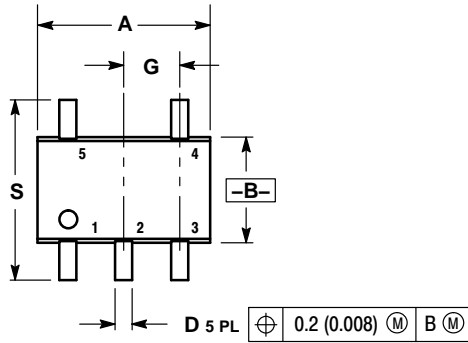
Device	Package	Shipping†
NL17SZ04EDFT2G	SC-88A/SOT-353/SC-70-5 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

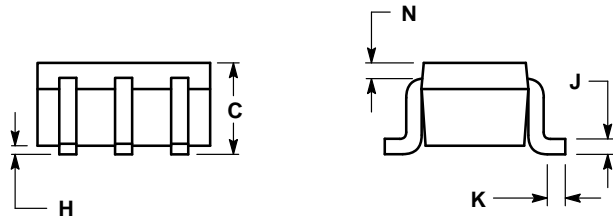
SC-88A (SC-70-5/SOT-353) CASE 419A-02 ISSUE L



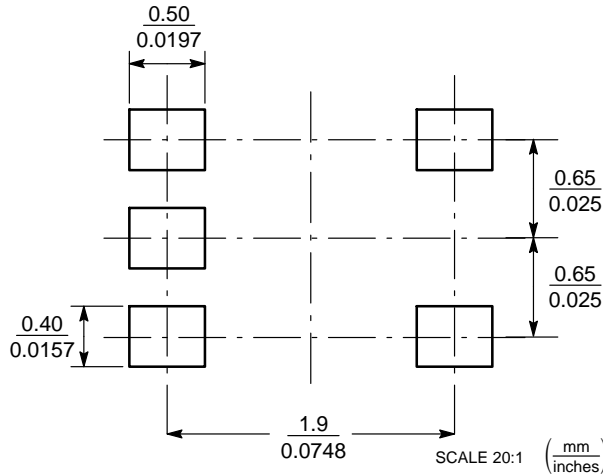
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



SOLDER FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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