

# NLA9306

## Dual Bidirectional I<sup>2</sup>C-bus and SMBus Voltage-Level Translator

The NLA9306 is a dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator with an enable (EN) input.

### Features

- 2-bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I<sup>2</sup>C-Bus Applications
- Standard-Mode, Fast-Mode, and Fast-Mode Plus I<sup>2</sup>C-Bus and SMBus Compatible
- Less Than 1.5 ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I<sup>2</sup>C-Bus Devices and Multiple Masters
- Allows Voltage Level Translation Between:
  - ◆ 1.0 V  $V_{ref(1)}$  and 1.8 V, 2.5 V, 3.3 V or 5 V  $V_{bias(ref)(2)}$
  - ◆ 1.2 V  $V_{ref(1)}$  and 1.8 V, 2.5 V, 3.3 V or 5 V  $V_{bias(ref)(2)}$
  - ◆ 1.8 V  $V_{ref(1)}$  and 3.3 V or 5 V  $V_{bias(ref)(2)}$
  - ◆ 2.5 V  $V_{ref(1)}$  and 5 V  $V_{bias(ref)(2)}$
  - ◆ 3.3 V  $V_{ref(1)}$  and 5 V  $V_{bias(ref)(2)}$
- Provides Bidirectional Voltage Translation With No Direction Pin
- Low 3.5  $\Omega$  ON-State Connection Between Input and Output Ports Provides Less Signal Distortion
- Open-Drain I<sup>2</sup>C-Bus I/O Ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V Tolerant I<sup>2</sup>C-Bus I/O Ports to Support Mixed-Mode Signal Operation
- High-Impedance SCL1, SDA1, SCL2 and SDA2 Pins for EN = LOW
- Lock-Up Free Operation
- Flow Through Pinout for Ease of Printed-Circuit Board Trace Routing
- Packages Offered:
  - ◆ US8, UQFN8, UDFN8
- ESD Performance: 2000 V Human Body Model
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



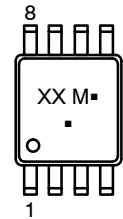
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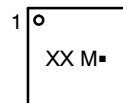
### MARKING DIAGRAMS



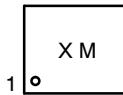
US8  
US SUFFIX  
CASE 493



UQFN8  
MU SUFFIX  
CASE 523AN



UDFN8  
1.45 x 1.0  
CASE 517BZ



XX, X = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
M = Date Code  
■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

**Function Description**

The NLA9306 is a dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.6 V (V<sub>ref(1)</sub>) and 1.8 V to 5.5 V (V<sub>bias(ref)(2)</sub>).

The NLA9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (R<sub>on</sub>) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The NLA9306 is not a bus buffer that provides both level translation and physical capacitance isolation to either side of the bus when both sides are connected. The NLA9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The NLA9306 can be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's

bus. The NLA9306 has a standard open-collector configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2 MHz.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port, when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (V<sub>pu(D)</sub>) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

**FUNCTIONAL DIAGRAM**

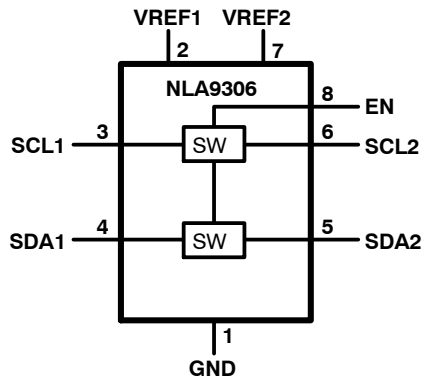


Figure 1. Logic Diagram

# NLA9306

## PIN ASSIGNMENTS

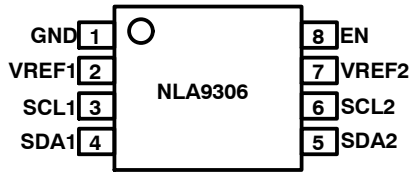


Figure 2. US8 Pinouts

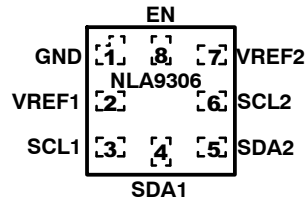


Figure 3. UQFN8 Pinout (Top Thru View)

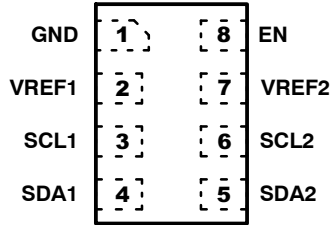


Figure 4. UDFN8 Pinout (Top Thru View)

Table 1. PIN DESCRIPTION

Pin	Description
GND	Ground
VREF1	Low-voltage side reference supply voltage for SCL1 and SDA1
SCL1	Serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
SDA1	Serial data, low-voltage side; connect to VREF1 through a pull-up resistor
SDA2	Serial data, high-voltage side; connect to VREF2 through a pull-up resistor
SCL2	Serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
VREF2	High-voltage side reference supply voltage for SCL2 and SDA2
EN	Switch enable input; connect to VREF2 and pull-up through a high resistor

Table 2. FUNCTION TABLE

Input EN (Note 1)	Function
Low	Disconnect
High	SCL1 = SCL2; SDA1 = SDA2

1. EN is controlled by the  $V_{bias(ref)(2)}$  logic levels and should be at least 1 V higher than  $V_{ref(1)}$  for best translator operation.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{ref(1)}$	Reference Voltage (Note 2)	-0.5 to +7.0	V
$V_{bias(ref)(2)}$	Reference Bias Voltage (Note 3)	-0.5 to +7.0	V
$V_{IN}$	Input Voltage	-0.5 to +7.0	V
$V_{I/O}$	Input / Output Pin Voltage	-0.5 to +7.0	V
$I_{CH}$	DC Channel Current	128	mA
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	$T_L = 260$	°C
$T_J$	Junction Temperature Under Bias	$T_J = 150$	°C
$\theta_{JA}$	Thermal Resistance (Note 2)	$\theta_{JA} = 150$	°C/W
$P_D$	Power Dissipation in Still Air at 85°C	$P_D = 833$	mW
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Mode (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 N/A > 1000	V
$I_{LATCHUP}$	Latchup Performance Above $V_{CC}$ and Below GND at 125°C (Note 6)	$\pm 100$	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
3. Tested to ANSI / ESDA / JEDEC JS-001-2017.
4. JEDEC recommends that ESD qualification to EIA / JESD22-A115-A (Machine Model) be discontinued per JEDEC / JEP172A.
5. Tested to EIA / JESD22-C101-F.
6. Tested to EIA / JESD78 Class II.

**Table 4. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
$V_{ref(1)}$	Reference Voltage (1) (Note 7) <span style="float: right;">VREF1</span>	0	5.5	V
$V_{bias(ref)(2)}$	Reference Bias Voltage (2) (Note 7) <span style="float: right;">VREF2</span>	0	5.5	V
$V_{I/O}$	Input / Output Pin Voltage SCL1, SDA1, SCL2, SDA2	0	5.5	V
$V_{I(EN)}$	Control Pin Input Voltage EN	0	5.5	V
$I_{sw(pass)}$	Pass Switch Current	0	64	mA
$T_A$	Operating Free-Air Temperature	-55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7.  $V_{(ref)(1)} \leq V_{bias(ref)(2)} - 1$  V for best results in level shifting applications.

**Table 5. DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Conditions	T <sub>A</sub> = -55°C to +125°C			Unit
			Min	Typ (Note 8)	Max	
V <sub>IK</sub>	Input Clamping Voltage	I <sub>I</sub> = -18 mA; V <sub>I(EN)</sub> = 0 V			-1.2	V
I <sub>IH</sub>	High-Level Input Current	V <sub>I</sub> = 5 V; V <sub>I(EN)</sub> = 0 V			5	μA
C <sub>I(EN)</sub>	EN Pin Input Capacitance	V <sub>I</sub> = 3 V or 0 V		7.1		pF
C <sub>I/O(off)</sub>	OFF-State I/O Pin Capacitance SCLn, SDAn	V <sub>O</sub> = 3 V or 0 V; V <sub>I(EN)</sub> = 0 V		4	6	pF
C <sub>I/O(on)</sub>	ON-State I/O Pin Capacitance SCLn, SDAn	V <sub>O</sub> = 3 V or 0 V; V <sub>I(EN)</sub> = 3 V		9.3	13.1	pF
R <sub>ON</sub>	ON-State Resistance <sup>(2)(3)</sup> SCLn, SDAn	V <sub>I</sub> = 0 V; I <sub>O</sub> = 64 mA V <sub>I(EN)</sub> = 4.5 V V <sub>I(EN)</sub> = 3 V V <sub>I(EN)</sub> = 2.3 V V <sub>I(EN)</sub> = 1.5 V		2.4 3.0 3.8 9.0	5.0 6.0 8.0 20	Ω
		V <sub>I</sub> = 2.4 V; I <sub>O</sub> = 15 mA V <sub>I(EN)</sub> = 4.5 V V <sub>I(EN)</sub> = 3 V		4.8 46	7.5 80	
		V <sub>I</sub> = 1.7 V; I <sub>O</sub> = 15 mA V <sub>I(EN)</sub> = 2.3 V		40	80	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. All typical values are at T<sub>A</sub> = 25°C.

9. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

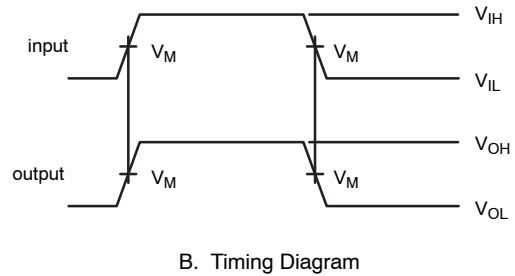
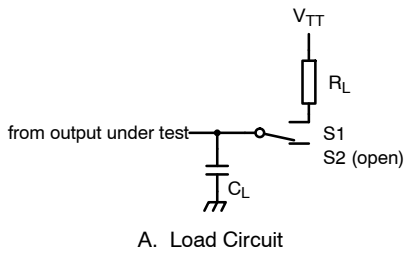
10. Guaranteed by design.

**Table 6. AC ELECTRICAL CHARACTERISTICS (Translating Down) – Values Guaranteed by Design**

Symbol	Parameter	Test Condition	Load Condition	T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Max	
<b>SEE FIGURE 4 LOAD SWITCH AT S2 POSITION</b>						
t <sub>PLH</sub>	Low-to-High Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	V <sub>I(EN)</sub> = 3.3 V; V <sub>IH</sub> = 3.3 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 1.15 V	C <sub>L</sub> = 15 pF	0	0.6	ns
			C <sub>L</sub> = 30 pF	0	1.2	
			C <sub>L</sub> = 50 pF	0	2.0	
t <sub>PHL</sub>	High-to-Low Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 2.5 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 0.75 V	C <sub>L</sub> = 15 pF	0	0.75	ns
			C <sub>L</sub> = 30 pF	0	1.5	
			C <sub>L</sub> = 50 pF	0	2.0	
t <sub>PLH</sub>	Low-to-High Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 2.5 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 0.75 V	C <sub>L</sub> = 15 pF	0	0.6	ns
			C <sub>L</sub> = 30 pF	0	1.2	
			C <sub>L</sub> = 50 pF	0	2.0	
t <sub>PHL</sub>	High-to-Low Propagation Delay, from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 2.5 V; V <sub>IL</sub> = 0 V; V <sub>M</sub> = 0.75 V	C <sub>L</sub> = 15 pF	0	0.75	ns
			C <sub>L</sub> = 30 pF	0	1.5	
			C <sub>L</sub> = 50 pF	0	2.5	

**Table 7. AC ELECTRICAL CHARACTERISTICS** (Translating Up) – Values Guaranteed by Design

Symbol	Parameter	Test Condition	Load Condition	T <sub>A</sub> = -55°C to +125°C		Unit
				Min	Max	
<b>SEE FIGURE 4 LOAD SWITCH AT S1 POSITION</b>						
t <sub>PLH</sub>	Low-to-High Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	V <sub>I(EN)</sub> = 3.3 V; V <sub>IH</sub> = 2.3 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 3.3 V; V <sub>M</sub> = 1.15 V	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 15 pF	0	0.5	ns
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 30 pF	0	1.0	
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	0	1.75	
t <sub>PHL</sub>	High-to-Low Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	V <sub>I(EN)</sub> = 3.3 V; V <sub>IH</sub> = 2.3 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 3.3 V; V <sub>M</sub> = 1.15 V	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 15 pF	0	0.8	ns
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 30 pF	0	1.65	
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	0	2.75	
t <sub>PLH</sub>	Low-to-High Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 1.5 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 2.5 V; V <sub>M</sub> = 0.75 V	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 15 pF	0	0.5	ns
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 30 pF	0	1.0	
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	0	1.75	
t <sub>PHL</sub>	High-to-Low Propagation Delay, from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	V <sub>I(EN)</sub> = 2.5 V; V <sub>IH</sub> = 1.5 V; V <sub>IL</sub> = 0 V; V <sub>TT</sub> = 2.5 V; V <sub>M</sub> = 0.75 V	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 15 pF	0	1.0	ns
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 30 pF	0	2.0	
			R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	0	3.3	



S1 = translating up; S2 = translating down.

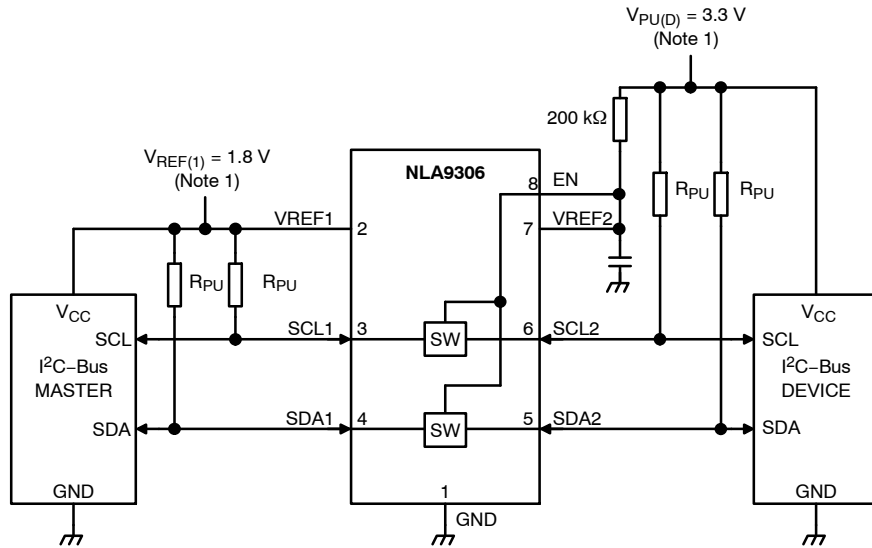
C<sub>L</sub> includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>0</sub> = 50 Ω; t<sub>r</sub> ≤ 2 ns; t<sub>f</sub> ≤ 2 ns.

The outputs are measured one at a time, with one transition per measurement.

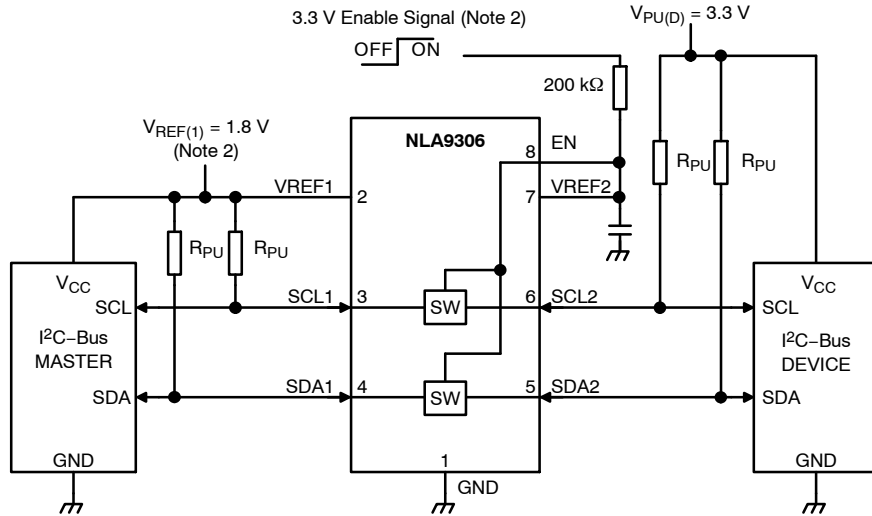
**Figure 5. Load Circuit for Outputs**

APPLICATION INFORMATION



1. The applied voltages at  $V_{ref(1)}$  and  $V_{pu(D)}$  should be such that  $V_{bias(ref)(2)}$  is at least 1 V higher than  $V_{ref(1)}$  for best translator operation.

Figure 6. Typical Application (Switch Always Enabled)



2. In the Enabled mode, the applied enable voltage and the applied voltage at  $V_{ref(1)}$  should be such that  $V_{bias(ref)(2)}$  is at least 1 V higher than  $V_{ref(1)}$  for best translator operation.

Figure 7. Typical Application (Switch Enable Control)

**Bidirectional Translation**

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side  $V_{pu(D)}$  through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I<sup>2</sup>C-bus master output can be totem-pole or open-drain (pull-up resistors may be required) and the I<sup>2</sup>C-bus device output can be totem-pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to  $V_{pu(D)}$ ). However, if either output is totem-pole, data must be

unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ( $V_{ref(1)}$ ) is connected to the processor core power supply voltage. When VREF2 is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V  $V_{pu(D)}$  power supply, and  $V_{ref(1)}$  is set between 1.0 V and ( $V_{pu(D)} - 1$  V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to  $V_{pu(D)}$ .

**Table 8. APPLICATION OPERATING CONDITIONS** Refer to Figure 6.

Symbol	Parameter	Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
V <sub>bias(ref)(2)</sub>	Reference Bias Voltage (2)		V <sub>ref(1)</sub> + 0.6	2.1	5	V
V <sub>I(EN)</sub>	EN Pin Input Voltage		V <sub>ref(1)</sub> + 0.6	2.1	5	V
V <sub>ref(1)</sub>	Reference Voltage (1)		0	1.5	4.4	V
I <sub>sw(pass)</sub>	Pass Switch Current			14		mA
I <sub>ref</sub>	Reference Current	Transistor		5		μA
T <sub>amb</sub>	Ambient Temperature	Operating in free-air	-55		+125	°C

11. All typical values are at T<sub>amb</sub> = 25 °C.

**Sizing Pull-up Resistor**

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, the pull-up resistor value is calculated as:

$$R_{PU} = \frac{V_{PU(D)} - 0.35 \text{ V}}{0.015 \text{ A}} \quad (\text{eq. 1})$$

The following table summarizes resistor reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor values shown in the +10% column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the NLA9306 device at 0.175 V, although the 15 mA only applies to current flowing through the NLA9306 device.

**Table 9. PULLUP RESISTOR VALUES** Calculated for V<sub>OL</sub> = 0.35 V; assumes output driver V<sub>OL</sub> = 0.175 V at stated current.

V <sub>pu(D)</sub>	Pullup Resistor Value (Ω)					
	15 mA		10 mA		3 mA	
	Nominal	+10% (Note 12)	Nominal	+10% <sup>(1)</sup>	Nominal	+10% (Note 12)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

12. +10% to compensate for V<sub>CC</sub> range and resistor tolerance.

**Maximum Frequency Calculation**

The maximum frequency is totally dependent upon the specifics of the application and the device can operate > 33 MHz. Basically, the NLA9306 behaves like a wire with the additional characteristics of transistor device physics and should be capable of performing at higher frequencies if used correctly.

Here are some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NLA9306 close to the processor.
- The trace length should be less than half the time of flight to reduce ringing and reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher the drive strength (up to 15 mA), the higher the frequency the device can use.

In a 3.3 V to 1.8 V direction level shift, if the 3.3 V side is being driven by a totem pole type driver no pull-up

resistor is needed on the 3.3 V side. The capacitance and line length of concern is on the 1.8 V side since it is driven through the ON resistance of the NLA9306. If the line length on the 1.8 V side is long enough there can be a reflection at the chip/terminating end of the wire when the transition time is shorter than the time of flight of the wire because the NLA9306 looks like a high-impedance compared to the wire. If the wire is not too long and the lumped capacitance is not excessive the signal will only be slightly degraded by the series resistance added by passing through the NLA9306. If the lumped capacitance is large the rise time will deteriorate, the fall time is much less affected and if the rise time is slowed down too much the duty cycle of the clock will be degraded and at some point the clock will no longer be useful. So the principle design consideration is to minimize the wire length and the capacitance on the 1.8 V side for the clock path. A pull-up resistor on the 1.8 V side can also be used to trade a slower fall time for a faster rise time and can also reduce the overshoot in some cases.



# NLA9306

## ORDERING INFORMATION

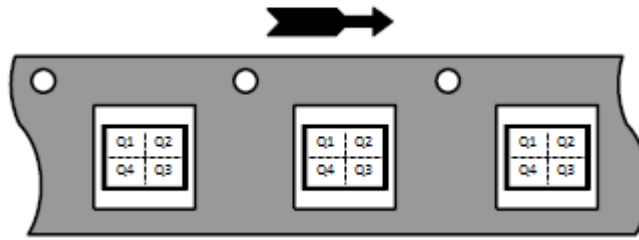
Device	Marking	Pin 1 Orientation (See below)	Package	Shipping <sup>†</sup>
NLA9306MUQ1TCG	AY	Q4	UQFN8 (Pb-Free)	3000 / Tape & Reel
NLA9306MU3TAG	D	Q1	UDFN8 (Pb-Free)	3000 / Tape & Reel
NLA9306MU3TCG	D	Q4	UDFN8 (Pb-Free)	3000 / Tape & Reel
NLA9306USG (In Development)	TBD	Q4	US8 (Pb-Free)	3000 / Tape & Reel
NLVA9306USG* (In Development)	TBD	Q4	US8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

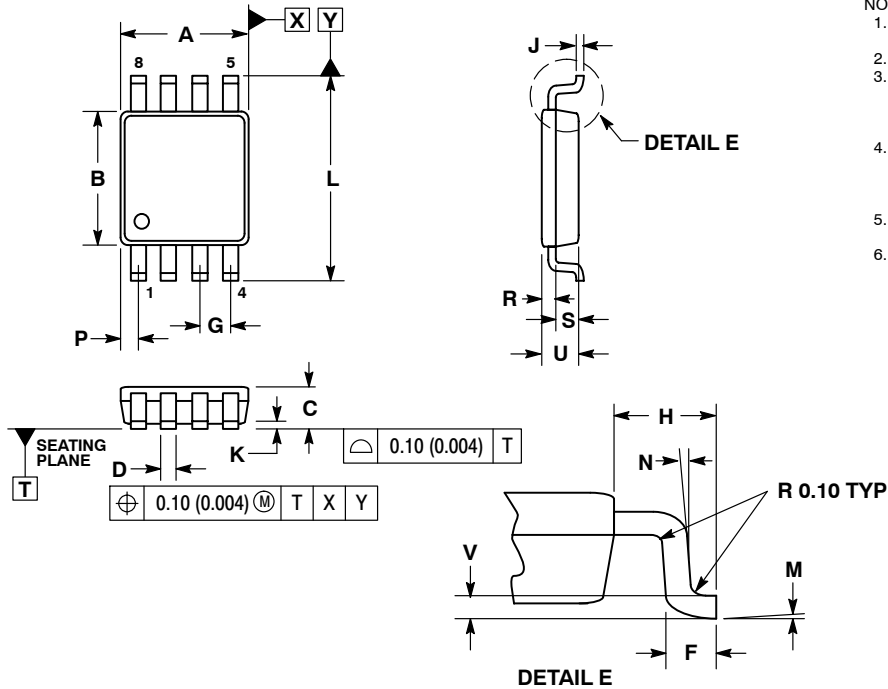
Direction of Feed



# NLA9306

## PACKAGE DIMENSIONS

US8  
CASE 493  
ISSUE D

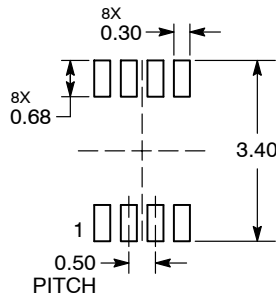


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED  $\pm 0.0508\text{MM}$  (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

**RECOMMENDED SOLDERING FOOTPRINT\***



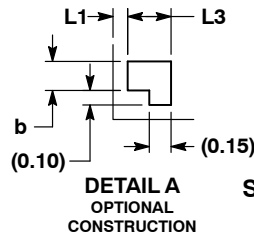
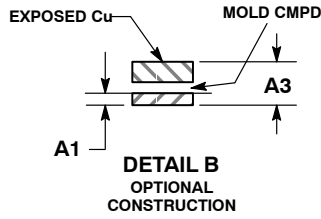
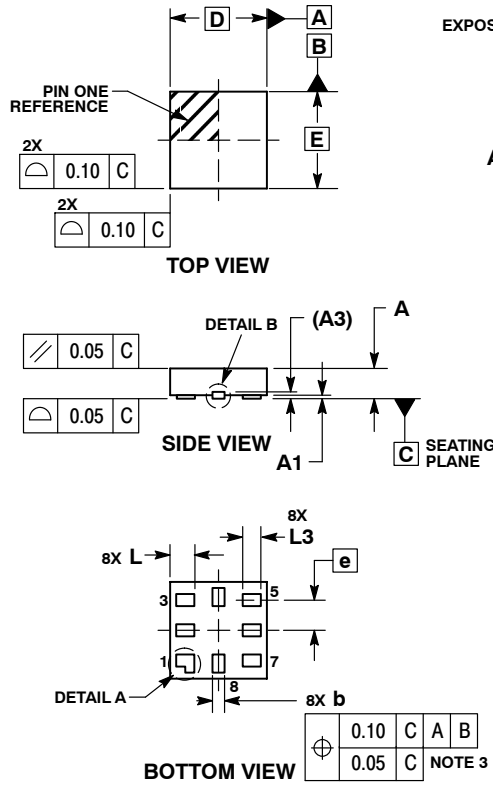
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLA9306

## PACKAGE DIMENSIONS

UQFN8, 1.6x1.6, 0.5P  
CASE 523AN  
ISSUE O

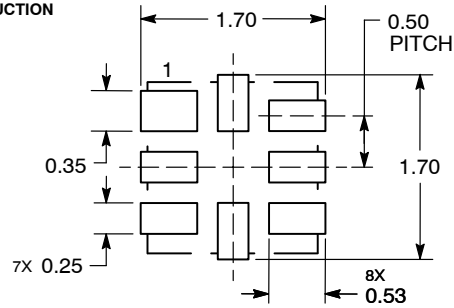


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	1.60	BSC
E	1.60	BSC
e	0.50	BSC
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

**SOLDERING FOOTPRINT\***



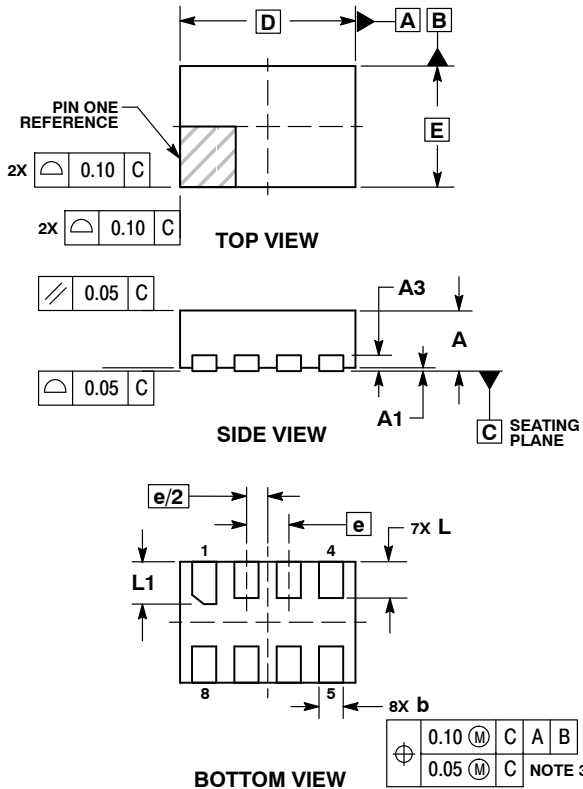
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NLA9306

## PACKAGE DIMENSIONS

UDFN8, 1.45x1, 0.35P  
CASE 517BZ  
ISSUE O

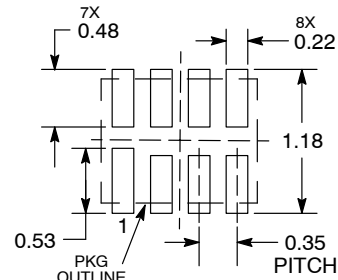


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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