NLGTL2014

Product Preview

4-Bit LVTTL to GTL Translator

The NLGTL2014 is a 4−bit translating transceiver that can be used to interface 3.3 V LVTTL ICs to the GTL bus. A direction pin is provided to configure the IC as either a GTL to LVTTL receiver or a LVTTL to GTL transmitter. The NLGTL2014 is pin−for−pin backward compatible to the GTL2005 (labels for A and B ports are interchanged).

Features

- Functions as either a GTL−/GTL/GTL+ Receiver or Transmitter
- V_{CC} Operating Range of 3.0 to 3.6 V with 5 V Tolerant LVTTL Inputs
- V_{REF} Adjustable from 0.5 V to $V_{CC}/2$
- Partial Power−down Permitted Single Channel/High−Drive
- Available in TSSOP−14 and UQFN12 Packages
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS−Compliant

Typical Applications

- Networking Servers
- Base Communication Stations
- PCs

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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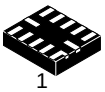
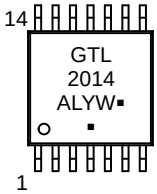


UQFN−12
MU SUFFIX
CASE 523AE

TSSOP−14
DT SUFFIX
CASE 948G

MARKING DIAGRAMS

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package



TSSOP−14

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

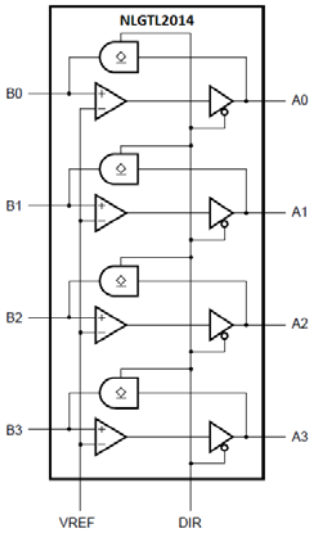


Figure 1. Logic Diagram

Table 1. FUNCTION TABLE

Input	Output	
DIR	**A (LVTTL)**	**B (GTL)**
H	Input	Bn = An
L	An = Bn	Input

Pin Assignments

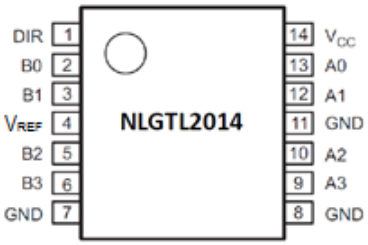


Figure 2. TSSOP−14

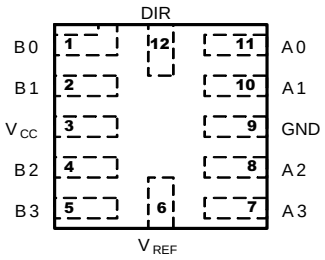


Figure 3. UQFN12 (Top Thru View)

Table 2. PIN DESCRIPTIONS

Symbol	Pin Number		Description
	TSSOP−14	UQFN12	
DIR	1	12	Direction Control Input (LVTTL)
B0	2	1	Data I/Os (GTL)
B1	3	2	
B2	5	4	
B3	6	5	
A3	9	7	Data I/Os (LVTTL)
A2	10	8	
A1	12	10	
A0	13	11	
VREF	4	6	GTL Reference Voltage
V_{CC}	14	3	Supply Voltage
GND	7, 8, 11 (Note 1)	9	Ground

1. For proper operation, pins 7, 8 and 11 of the TSSOP−14 package must be connected together externally to system GND.

Table 3. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		−0.5 to +4.6	V
I_{IK}	Input Clamp Current	V_I < GND	−50	mA
V_I	Input Voltage	A Port B Port	−0.5 to +7.0 −0.5 to 4.6	V
I_{OK}	Output Clamp Current	V_O < GND	−50	mA
V_O	Output Voltage	Output in OFF or HIGH State A Port B Port	 −0.5 to +7.0 −0.5 to 4.6	V
I_{OL}	LOW Level Output Current	Current Into Any Output in the LOW State A Port B Port	 32 80	mA
I_{OH}	HIGH Level Output Current	Current out of Any Output in the HIGH State A Port	 −32	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Mode (Note 3) Charged Device Model (Note 4)	2000 2000	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±500	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
3. Tested to EIA / JESD22−A114−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{TT} (Note 7)	Termination Voltage	GTL−	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference Voltage	Overall	0.5	2/3 V_{TT}	V_{CC}/2	V
		GTL−	0.5	0.6	0.63	
		GTL	0.76	0.8	0.84	
		GTL+	0.87	1.0	1.1	
V_I	Input Voltage	B Port	0	V_{TT}	3.6	V
		Except B Port	0	3.3	5.5 (Note 8)	
V_{IH}	HIGH−Level Input Voltage	B Port	V_{REF} + 0.050	−	−	V
		Except B Port	2	−	−	
V_{IL}	LOW−Level Input Voltage	B Port	−	−	V_{REF} − 0.050	V
		Except B Port	−	−	0.8	
I_{OH}	HIGH−Level Output Current	A Port	−	−	−16	V
I_{OL}	LOW−Level Output Current	A Port	−	−	16	V
		B Port	−	−	40	
T_A	Operating Free−Air Temperature		−40	−	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

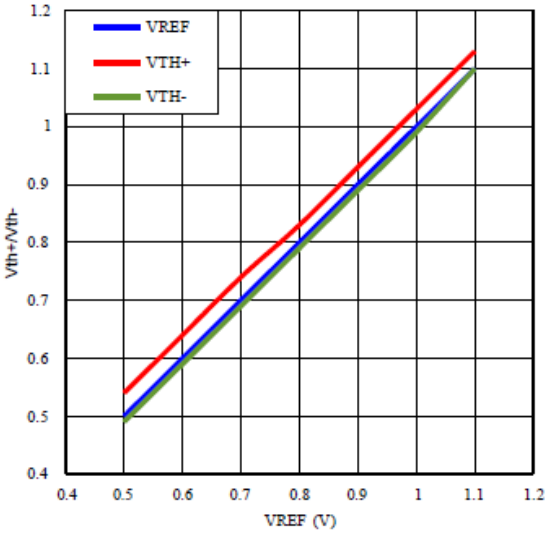
6. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
7. V_{TT} maximum of 3.6 V shall have resistor sized so I_{OL} maximum is not exceeded.
8. The V_I(max) of a LVTTL port is 3.6 V if configured as an output (DIR=L).

Table 5. STATIC CHARACTERISTICS

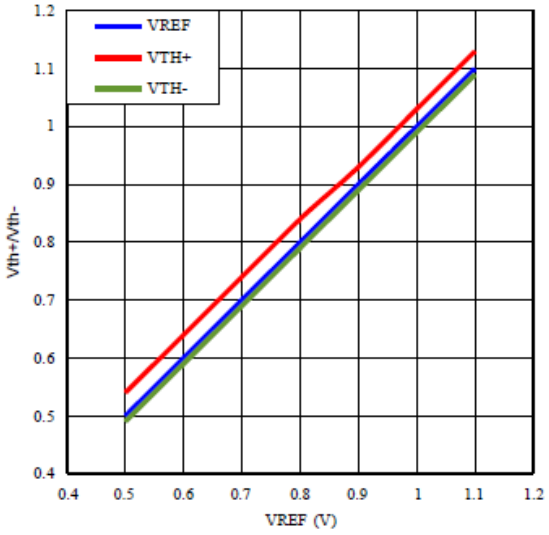
Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to 85°C			Unit
				Min	Typ (Note 9)	Max	
V_{OH}	High−Level Output Voltage	A Port; I_{OH} = −100 μA	3.0 to 3.6	V_{CC} −0.2	−	−	V
		A Port; I_{OH} = −16 mA	3.0	2.0	−	−	
V_{OL}	Low−Level Output Voltage	A Port; I_{OL} = 8 mA	3.0	−	0.28	0.4	V
		A Port; I_{OL} = 12 mA	3.0	−	0.40	0.55	
		B Port; I_{OL} = 40 mA	3.0	−	0.23	0.4	
I_I	Input Leakage Current	DIR Input; V_I = V_{CC} or GND	3.6	−	−	±1	μA
		A Port; V_I = 5.5 V	0 or 3.6	−	−	10	
		A Port; V_I = V_{CC}	3.6	−	−	±1	
		A Port; V_I = 0 V	3.6	−	−	−5	
		B Port; V_I = V_{TT} or GND	3.6	−	−	±1	
I_{OZ}	OFF−State Leakage Current	A Port; V_I or V_O = 0 to 3.6 V	0	−	−	±100	μA
I_{CC}	Quiescent Supply Current	A Port; V_I = V_{CC} or GND; I_O = 0 mA	3.6	−	4	10	mA
		B Port; V_I = V_{TT} or GND; I_O = 0 mA	3.6	−	4	10	
ΔI_{CC} (Note 10)	Increase in Quiescent Supply Current (per input)	A Port or DIR; V_I = V_{CC} – 0.6 V	3.6	−	−	700	μA
C_I	Input Capacitance	DIR Input; V_I = 3.0 V or 0 V	−	−	2	4	pF
$C_{I/O}$	Input/Output Capacitance	A Port; V_O = 3.0 V or 0 V	−	−	8	10	pF
		B Port; V_O = V_{TT} or 0 V	−	−	3	5	

9. All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
10. Defined as the increase in the supply current for each input that is set to the specified input voltage level rather than V_{CC} or GND.

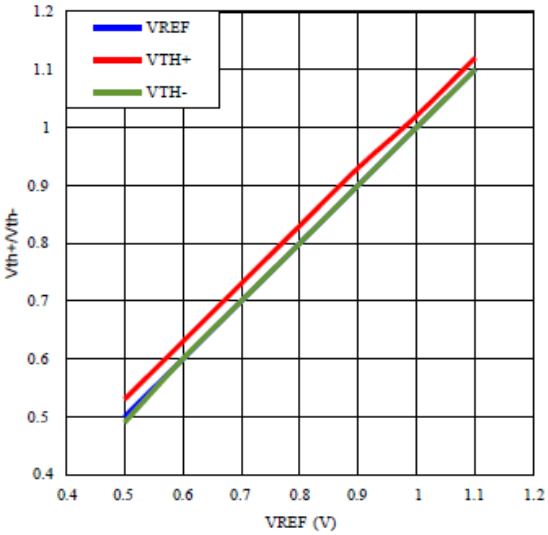
Typical Characteristics



a. V_{CC} = 3.0 V; T_A = −40°C



b. V_{CC} = 3.3 V; T_A = 25°C



c. V_{CC} = 3.6 V; T_A = 85°C

V_{REF} is equal to the reference voltage on the GTL bus.
V_{th+} is the GTL input high threshold, which is typically equal to Vref + 50 mV.
V_{th-} is the GTL input low threshold, which is typically equal to Vref − 50 mV.

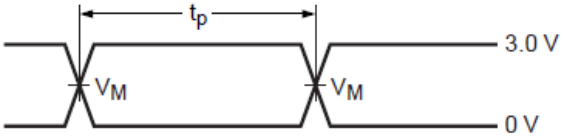
Figure 4. GTL V_{th+} and V_{th-} vs V_{REF}

Table 6. DYNAMIC CHARACTERISTICS
V_{CC} = 3.0 V to 3.6 V and T_A = −40 to +85°C, unless otherwise specified. See Figure 8 for test setup and timing definitions.

Symbol	Parameter	Conditions	T_A = −40°C to 85°C									Unit
			GTL−			GTL			GTL+			
			V_{REF} = 0.6 V; V_{TT} = 0.9 V			V_{REF} = 0.8 V; V_{TT} = 1.2 V			V_{REF} = 1.0 V; V_{TT} = 1.5 V			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	LOW to HIGH Propagation Delay	An to Bn; See Figure 6	−	2.8	5	−	2.8	5	−	2.8	5	ns
t_{PHL}	HIGH to LOW Propagation Delay		−	3.3	7	−	3.4	7	−	3.4	7	
t_{PLH}	LOW to HIGH Propagation Delay	Bn to An; See Figure 7	−	5.3	8	−	5.2	8	−	5.1	8	ns
t_{PHL}	HIGH to LOW Propagation Delay		−	5.2	8	−	4.9	7.2	−	4.7	7.2	

Waveforms

V_M = 1.5 V at $V_{CC} \geq$ 3.0 V; $V_M = V_{CC}/2$ at $V_{CC} \leq$ 2.7 V for A ports and control pins; $V_M = V_{REF}$ for B ports.



V_M = 1.5 V for A port and V_{REF} for B port

Figure 5. Pulse Duration

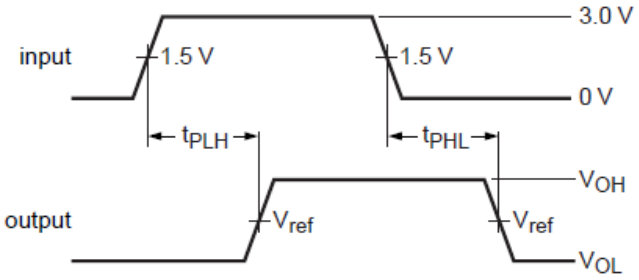
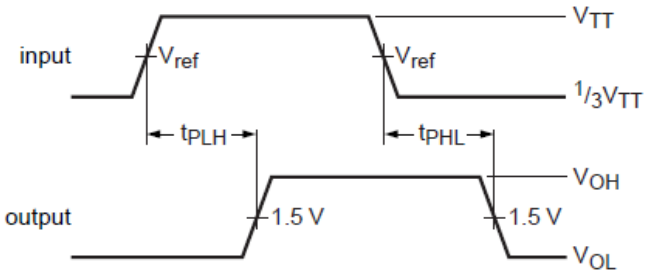


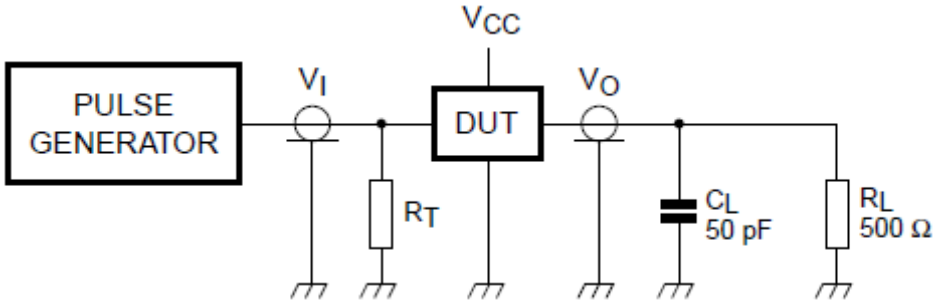
Figure 6. Propagation Delay, An to Bn



PRR ≤ 10 MHz; Z_0 = 50 Ω; $t_r \leq$ 2.5 ns; $t_f \leq$ 2.5 ns

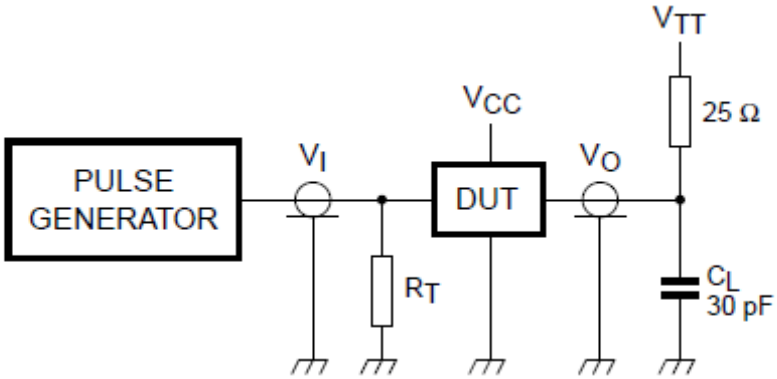
Figure 7. Propagation Delay, Bn to An

Test Setups



R_L — Load resistor
C_L — Load capacitance; includes jig and probe capacitance
R_T — Termination resistance; should be equal to output impedance of pulse generators.

Figure 8. Load Circuit for Switching Times



R_L — Load resistor
C_L — Load capacitance; includes jig and probe capacitance
R_T — Termination resistance; should be equal to output impedance of pulse generators.

Figure 9. Load Circuit for B Outputs

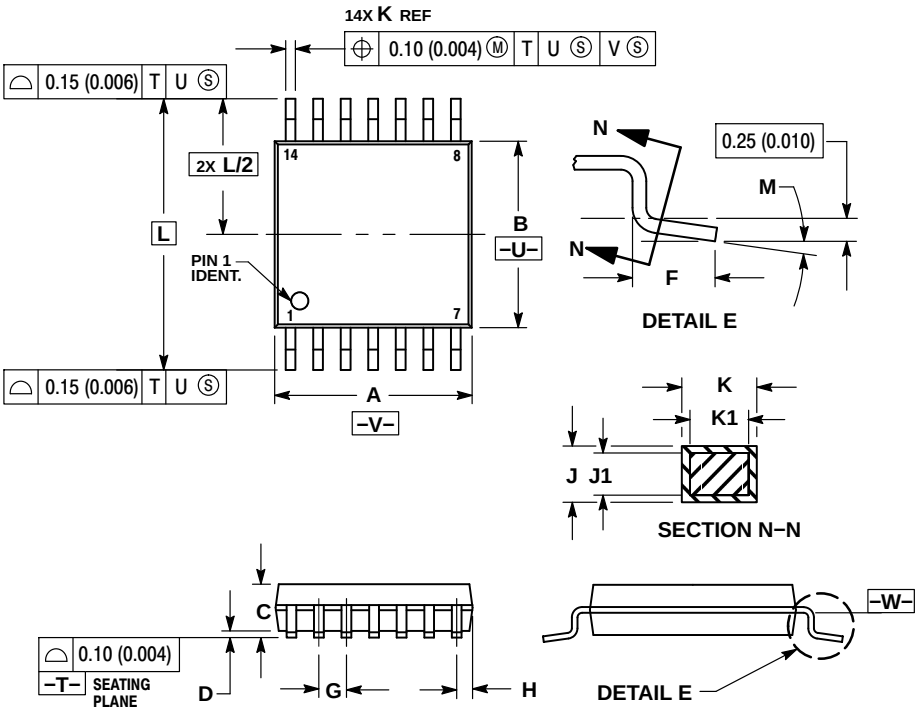
ORDERING INFORMATION

Device	Package	Shipping†
NLGTL2014DTR2G	TSSOP−14 (Pb−Free)	2500 / Tape & Reel
NLGTL2014MUTAG	UQFN−12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

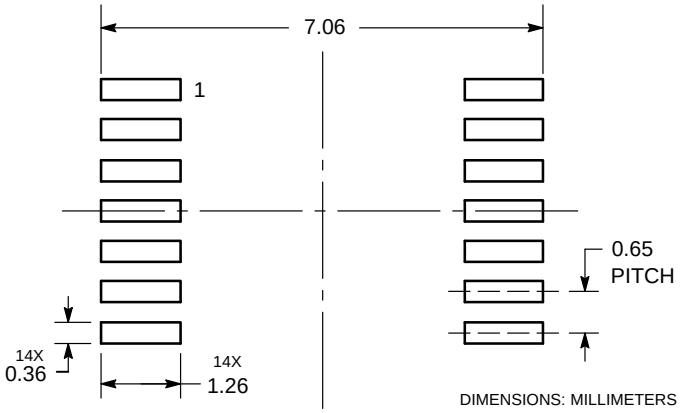
TSSOP−14
CASE 948G
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

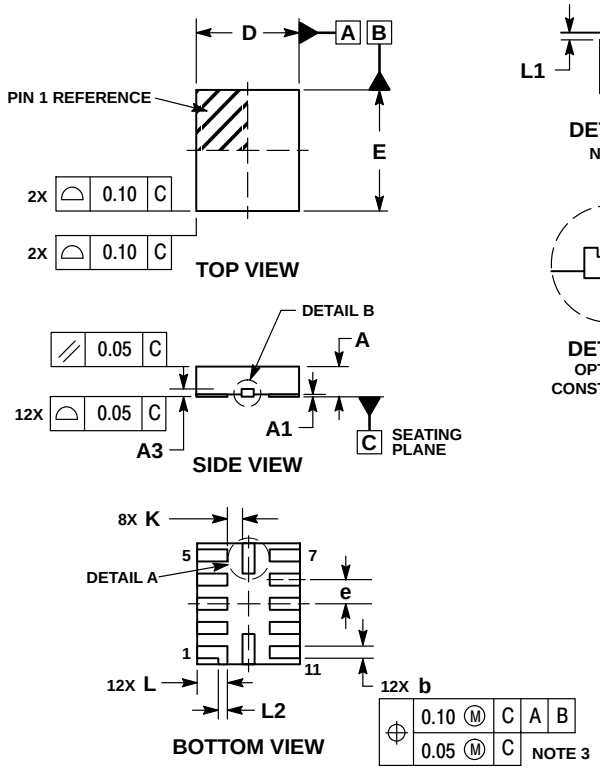
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

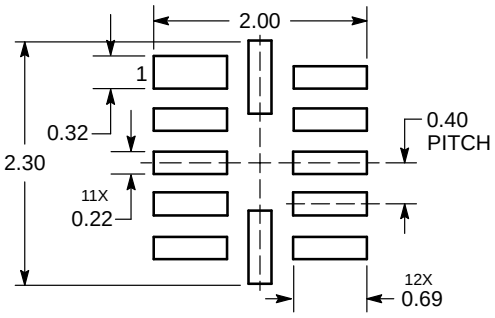
UQFN12 1.7x2.0, 0.4P
CASE 523AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

MOUNTING FOOTPRINT
SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Email: orderlit@onsemi.com

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Japan Customer Focus Center
Phone: 81−3−5817−1050

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