NLV18HC1Gxx, NLV18HC1GTxx

Automotive High Speed Logic Gates

The NLV18HC1Gxx and NLV18HC1GTxx are automotive−grade High−Speed CMOS logic gates.

The NLV18HC1Gxx devices have CMOS input voltage levels while the NLV18HC1GTxx devices have TTL input voltage levels.

Features

- High Speed: t_{PD} = 7 ns (Typ) at V_{CC} = 6 V
- Low Power Dissipation: I_{CC} = 1 μA (Max) at T_A = 25°C
- High Noise Immunity
- Balanced Propagation Delays ($t_{PLH} = t_{PHL}$)
- Symmetrical Output Impedance ($I_{OH} = I_{OL}$ = 2 mA)
- Operating Temperature: −55°C to +125°C
  AEC Grade 1−Compliant: −40°C to +125°C
- Tiny SC−88A Package (other package offerings may be available upon request)
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and RoHS Compliant

FUNCTION LIST

xx	Function
00	2−Input NAND
02	2−Input NOR
04	Inverter
05	Open−Drain Inverter
07	Open−Drain Buffer
08	2−Input AND
14	Schmitt−Trigger Inverter
17	Schmitt−Trigger Buffer
32	2−Input OR
34	Buffer
86	2−Input XOR
125	Tri−State Buffer
126	Tri−State Buffer
U04	Unbuffered Inverter

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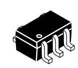
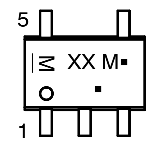


SC−88A
DF SUFFIX
CASE 419A

MARKING DIAGRAM



XX = Device Code
M = Date Code*
▪ = Pb−Free Package

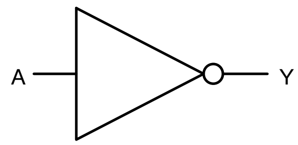
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

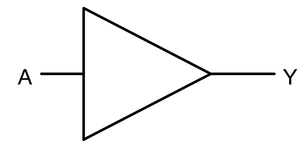
See detailed ordering and shipping information on page 10 of this data sheet.

Functions and Function Tables – Buffers and Inverters



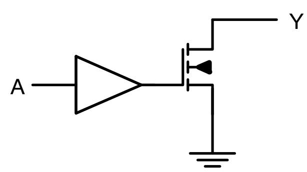
04 – Inverter
U04 – Unbuffered Inverter

A	Y
0	1
1	0



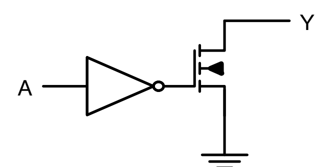
34 – Buffer

A	Y
0	0
1	1



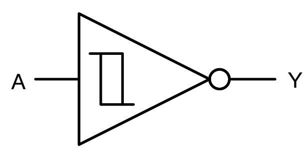
05 – Open–Drain Inverter

A	Y
0	Hi–Z
1	0



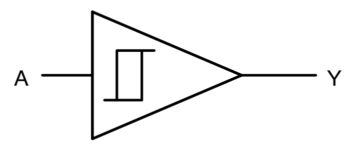
07 – Open–Drain Buffer

A	Y
0	0
1	Hi–Z



14 – Schmitt–Trigger Inverter

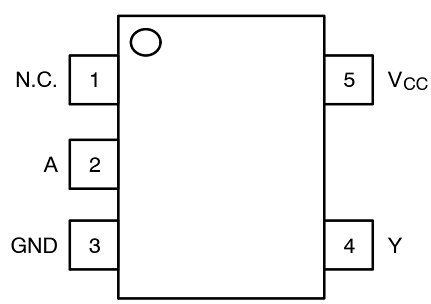
A	Y
0	1
1	0



17 – Schmitt–Trigger Buffer

A	Y
0	0
1	1

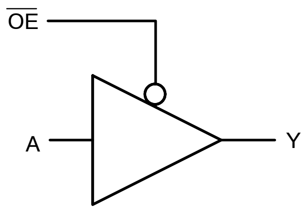
Pin Assignment



Pinout (Buffers and Inverters)

Pin	Name	Description
1	N.C.	No Connection
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply

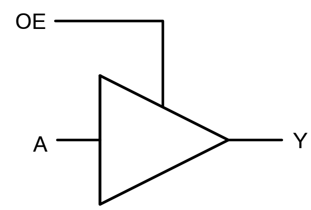
Functions and Function Tables – Tri–State Buffers and Bus Drivers



125 – Tri–State Buffer

$\overline{OE}$	A	Y
0	0	0
0	1	1
1	X	Hi–Z

X = Don’t Care

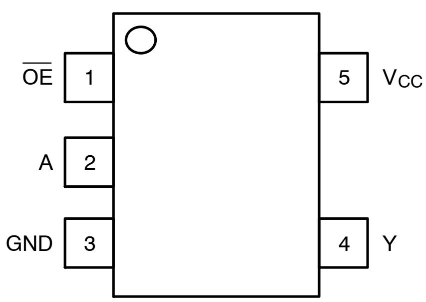


126 – Tri–State Buffer

OE	A	Y
0	X	Hi–Z
1	0	0
1	1	1

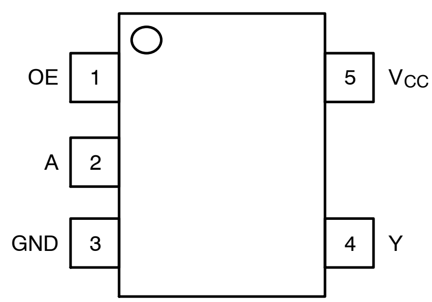
X = Don’t Care

Pin Assignments



Pinout (125)

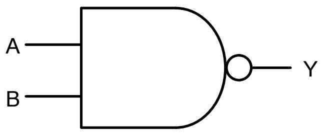
Pin	Name	Description
1	$\overline{OE}$	Enable (Active–Low)
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply



Pinout (126)

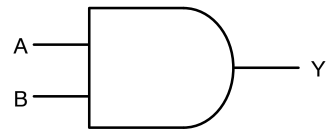
Pin	Name	Description
1	OE	Enable (Active–High)
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply

Functions and Function Tables – Gates



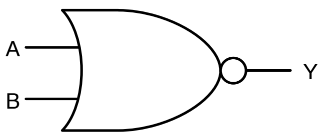
00 – NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



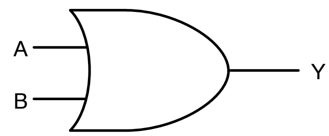
08 – AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



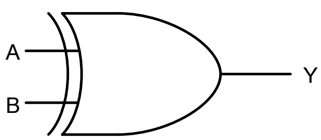
02 – NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



32 – OR

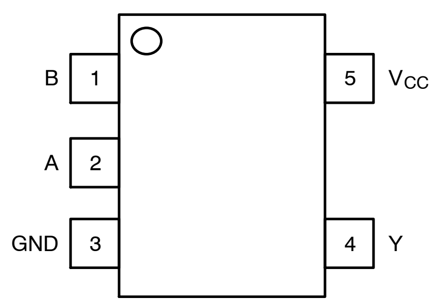
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



86 – XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Pin Assignment



Pinout (Gates)

Pin	Name	Description
1	B	Input
2	A	Input
3	GND	Ground
4	Y	Output
5	V_{CC}	Supply

Table 1. MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±20	mA
I_{OUT}	DC Output Source/Sink Current		±12.5	mA
I_{CC} or I_{GND}	DC Supply Current Per Supply Pin or Ground Pin		±25	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)		659	°C/W
P_D	Power Dissipation in Still Air at 85°C		190	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	2000 1000	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 20 ounce copper trace with no air flow.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	NLV18HC1Gxx	2.0	6.0	V
		NLV18HC1GTxx	4.5	5.5	
V_{IN}	Digital Input Voltage		0	V_{CC}	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate				ns/V
	Functions 14 and 17		0	No Limit	
	All Other Functions	V_{CC} = 1.65 V to 1.95 V	0	20	
		V_{CC} = 2.3 V to 2.7 V	0	20	
		V_{CC} = 3.0 V to 3.6 V	0	10	
		V_{CC} = 4.5 V to 5.5 V	0	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC ELECTRICAL CHARACTERISTICS (NLV18HC1Gxx)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to 85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
NLV18HC1G14 and NLV18HC1G17											
V_{T+}	Positive−Going Threshold		2.0	–	1.29	1.5	–	1.5	–	1.5	V
			3.0	–	1.91	2.20	–	2.20	–	2.20	
			4.5	–	2.77	3.15	–	3.15	–	3.15	
			5.5	–	3.37	3.85	–	3.85	–	3.85	
V_{T-}	Negative−Going Threshold		2.0	0.5	0.75	–	0.5	–	0.5	–	V
			3.0	0.9	1.2	–	0.9	–	0.9	–	
			4.5	1.35	1.91	–	1.35	–	1.35	–	
			5.5	1.65	2.38	–	1.65	–	1.65	–	
V_H	Hysteresis Voltage		2.0	0.2	0.55	1.0	0.2	1.0	0.2	1.0	V
			3.0	0.3	0.7	1.2	0.3	1.2	0.3	1.2	
			4.5	0.4	0.86	1.4	0.4	1.4	0.4	1.4	
			5.5	0.5	0.98	1.6	0.5	1.6	0.5	1.6	
NLV18HC1GU04 (Under Development)											
V_{IH}	High− Level Input Voltage		2.0	TBD	–	–	TBD	–	TBD	–	V
			3.0	TBD	–	–	TBD	–	TBD	–	
			4.5	TBD	–	–	TBD	–	TBD	–	
			6.0	TBD	–	–	TBD	–	TBD	–	
V_{IL}	Low− Level Input Voltage		2.0	–	–	TBD	–	TBD	–	TBD	V
			3.0	–	–	TBD	–	TBD	–	TBD	
			4.5	–	–	TBD	–	TBD	–	TBD	
			6.0	–	–	TBD	–	TBD	–	TBD	
ALL OTHER PARTS											
V_{IH}	High− Level Input Voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			4.5	3.15	–	–	3.15	–	3.15	–	
			6.0	4.20	–	–	4.20	–	4.20	–	
V_{IL}	Low− Level Input Voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			4.5	–	–	1.35	–	1.35	–	1.35	
			6.0	–	–	1.80	–	1.80	–	1.80	
ALL PARTS											
V_{OH} (Note 4)	High− Level Output Voltage	$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-}) I_{OH} = −20 μA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
			6.0	5.9	6.0	–	5.9	–	5.9	–	
		$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-})									
		I_{OH} = −2 mA	4.5	4.18	4.31	–	4.13	–	4.08	–	
		I_{OH} = −2.6 mA	6.0	5.68	5.80	–	5.63	–	5.58	–	

Table 3. DC ELECTRICAL CHARACTERISTICS (NLV18HC1Gxx)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = −40°C to 85°C Min	T_A = −40°C to 85°C Max	T_A = −55°C to +125°C Min	T_A = −55°C to +125°C Max	Unit
ALL PARTS											
V_{OL}	Low− Level Output Voltage	$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-}) I_{OL} = 20 μA	2.0	–	0.0	0.1	–	0.1	–	0.1	V
			3.0	–	0.0	0.1	–	0.1	–	0.1	
			4.5	–	0.0	0.1	–	0.1	–	0.1	
			6.0	–	0.0	0.1	–	0.1	–	0.1	
		$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-})									
		I_{OL} = 2 mA	4.5	–	0.17	0.26	–	0.33	–	0.40	
		I_{OL} = 2.6 mA	6.0	–	0.18	0.26	–	0.33	–	0.40	
I_{IN}	Input Leakage Current	V_{IN} = 6.0 V or GND	6.0	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	6.0	–	–	1.0	–	10	–	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The V_{OH} parameter does not apply to devices with open−drain output, NLV18HC1G05, NLV18HC1G07, NLV18HC1GT05 and NLV18HC1GT07.

Table 4. DC ELECTRICAL CHARACTERISTICS (NLV18HC1GTxx)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C Min	T_A = 25 °C Typ	T_A = 25 °C Max	T_A = −40°C to 85°C Min	T_A = −40°C to 85°C Max	T_A = −55°C to +125°C Min	T_A = −55°C to +125°C Max	Unit
NLV18HC1GT14 and NLV18HC1GT17											
V_{T+}	Positive−Going Threshold		4.5	–	1.64	2.0	–	2.0	–	2.0	V
			5.5	–	1.85	2.1	–	2.1	–	2.1	
V_{T-}	Negative−Going Threshold		4.5	0.5	1.0	–	0.5	–	0.5	–	V
			5.5	0.6	1.14	–	0.6	–	0.6	–	
V_H	Hysteresis Voltage		4.5	0.4	0.64	1.4	0.4	1.4	0.4	1.4	V
			5.5	0.5	0.71	1.6	0.5	1.6	0.5	1.6	
ALL OTHER PARTS											
V_{IH}	High− Level Input Voltage		4.5 – 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	Low− Level Input Voltage		4.5 – 5.5	–	–	0.8	–	0.8	–	0.8	V
ALL PARTS											
V_{OH} (Note 4)	High− Level Output Voltage	$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-})									V
		I_{OH} = −20 μA	4.5	4.4	4.5	–	4.4	–	4.4	–	
		I_{OH} = −2 mA	4.5	4.18	4.32	–	4.13	–	4.08	–	
V_{OL}	Low− Level Output Voltage	$V_{IN} = V_{IH}$ (V_{T+}) or V_{IL} (V_{T-})									V
		I_{OL} = 20 μA	4.5	–	0.0	0.1	–	0.1	–	0.1	
		I_{OL} = 2 mA	4.5	–	0.17	0.26	–	0.33	–	0.40	
I_{IN}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND; I_O = 0 A	5.5	–	–	1.0	–	10	–	40	μA
ΔI_{CC}	Additional Supply Current per Input	$V_{IN} = V_{CC}$ − 2.1 V; I_O = 0 A; Other input at V_{CC} or GND	4.5 – 5.5	–	–	1.0	–	1.5	–	1.65	mA

Table 5. AC ELECTRICAL CHARACTERISTICS (NLV18HC1Gxx) (Input $t_r = t_f = 6.0$ nS)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to 85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y	C_L = 15 pF	5.0	–	3.5	15	–	20	–	25	ns
		C_L = 50 pF	2.0	–	20	100	–	125	–	155	
			3.0	–	11	27	–	35	–	90	
			4.5	–	8	20	–	25	–	35	
			6.0	–	7	17	–	21	–	26	
t_{TLH}, t_{THL}	Output Transition Time	C_L = 15 pF	5.0	–	3	10	–	15	–	20	ns
		C_L = 50 pF	2.0	–	25	125	–	155	–	200	
			3.0	–	16	35	–	45	–	60	
			4.5	–	11	25	–	31	–	38	
			6.0	–	9	21	–	26	–	32	
t_{PZH}, t_{PZL} (Note 5)	Enable Time, (A or $\overline{OE}$ or OE) to Y	C_L = 50 pF	2.0	–	19	TBD	–	155	–	190	ns
			3.0	–	TBD	TBD	–	TBD	–	TBD	
			4.5	–	9	TBD	–	31	–	38	
			6.0	–	7	TBD	–	26	–	32	
t_{PHZ}, t_{PLZ} (Note 5)	Disable Time, (A or $\overline{OE}$ or OE) to Y	C_L = 50 pF	2.0	–	19	TBD	–	155	–	190	ns
			3.0	–	TBD	TBD	–	TBD	–	TBD	
			4.5	–	9	TBD	–	31	–	38	
			6.0	–	7	TBD	–	26	–	32	
C_{IN}	Input Capacitance			–	5	10	–	10	–	10	pF

5. These parameters apply only to devices where the output may be tri−stated. These specifications are still under development.

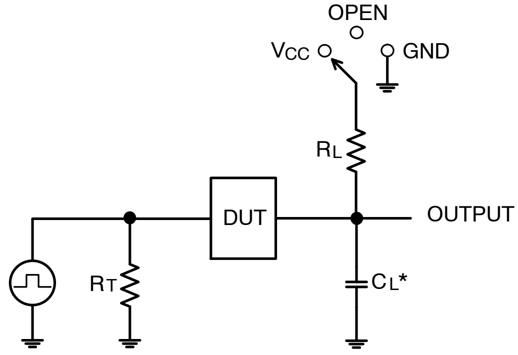
Table 6. AC ELECTRICAL CHARACTERISTICS (NLV18HC1GTxx) (Input $t_r = t_f = 6.0$ nS)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to 85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, (A or B) to Y	C_L = 15 pF	5.0	–	3.5	15	–	20	–	25	ns
		C_L = 50 pF	4.5	–	8	20	–	25	–	35	
t_{TLH}, t_{THL}	Output Transition Time	C_L = 15 pF	5.0	–	3	10	–	15	–	20	ns
		C_L = 50 pF	4.5	–	11	25	–	31	–	38	
t_{PZH}, t_{PZL} (Note 5)	Enable Time, (A or $\overline{OE}$ or OE) to Y	C_L = 50 pF	4.5	–	9	TBD	–	31	–	38	ns
t_{PHZ}, t_{PLZ} (Note 5)	Disable Time, (A or $\overline{OE}$ or OE) to Y	C_L = 50 pF	4.5	–	9	TBD	–	31	–	38	ns

Table 7. CAPACITANCE

Symbol	Parameter	Typical @ = 25°C, V_{CC} = 5.0 V	Unit
C_{IN}	Input Capacitance	5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \times V_{CC}{}^2 \times f_{in} + I_{CC} \times V_{CC}$.



Test	Switch Position	C_L, pF	R_L, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	X
t_{TLH} / t_{THL} (Note 7)	Open		X
t_{PLZ} / t_{PZL}	V_{CC}		1 k
t_{PHZ} / t_{PZH}	GND		1 k

X – Don't Care

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 1. Test Circuit

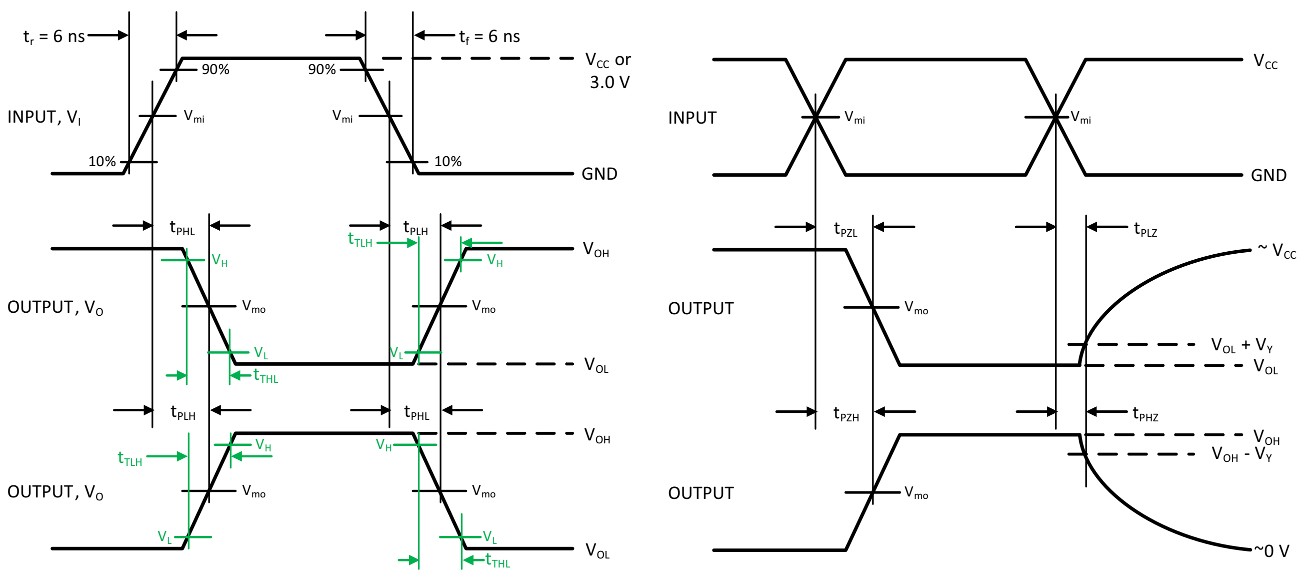


Figure 2. Switching Waveforms

	Input		Output			
Device Type	**V_I, V**	**V_{mi}, V**	**V_{mo}, V**	**V_L, V**	**V_H, V**	**V_Y, V**
NLV18HC1Gxx	GND to V_{CC}	$V_{CC}/2$	$V_{CC}/2$	V_{OL} + 0.1 (V_{OH}–V_{OL})	V_{OL} + 0.9 (V_{OH}–V_{OL})	0.3
NLV18HC1GTxx	GND to 3.0 V	1.3 V	1.3 V	V_{OL} + 0.1 (V_{OH}–V_{OL})	V_{OL} + 0.9 (V_{OH}–V_{OL})	0.3

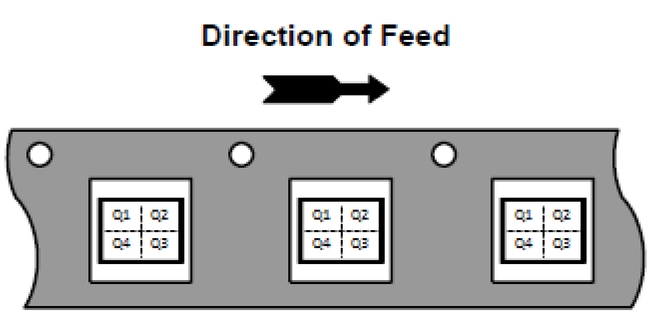
7. t_{TLH} and t_{THL} are measured from 10% to 90% of (V_{OH} – V_{OL}), and 90% to 10% of (V_{OH} – V_{OL}), respectively.

ORDERING INFORMATION

Device	Package	Marking	Pin 1 Orientation (See below)	Shipping†
NLV18HC1G00DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G02DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G04DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G05DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G07DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G08DFT2G	SC−88A	H2	Q4	3000 / Tape & Reel
NLV18HC1G14DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G17DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G32DFT2G	SC−88A	H4	Q4	3000 / Tape & Reel
NLV18HC1G34DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G86DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G125DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1G126DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GU04DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT00DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT02DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT04DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT05DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT07DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT08DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT14DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT17DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT32DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT34DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT86DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT125DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel
NLV18HC1GT126DFT2G (in development)	SC−88A	TBD	Q4	3000 / Tape & Reel

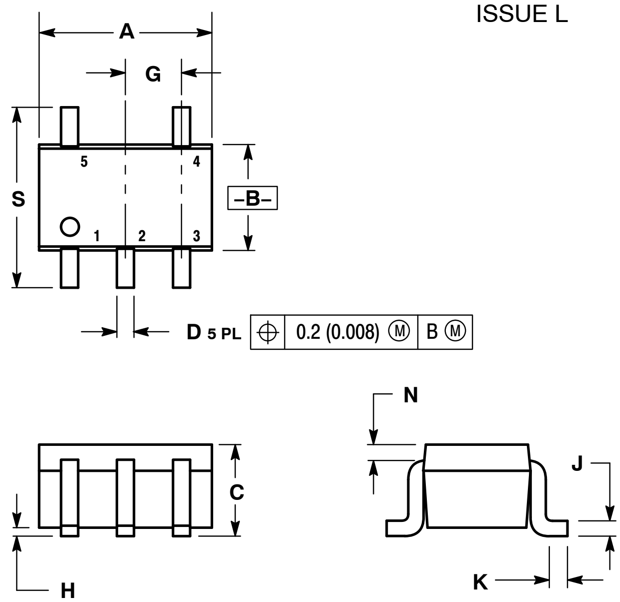
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

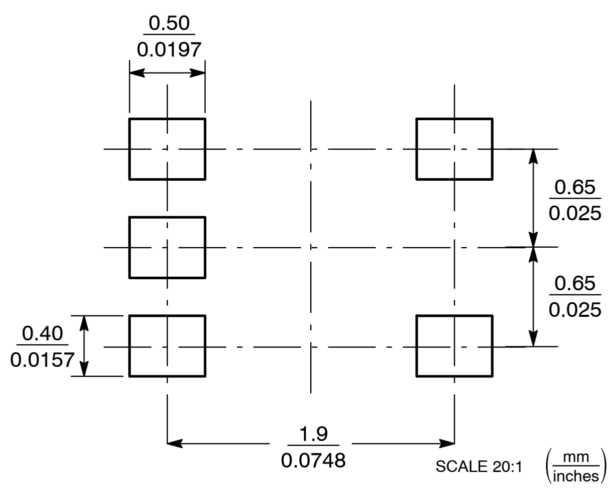
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



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