ON Semiconductor®

NOII4SM014KA

IBIS4-14000 14-Megapixel CMOS Image Sensor

Features

- 3048 × 4560 active pixels
- 8-µm 8-µm square pixels
- 36-mm × 24-mm focal plane array
- 35 mm optical format
- 3 frames per second (fps) frame rate
- Rolling shutter mode
- On-chip FPN correction
- 4 parallel analog outputs
- Serial peripheral interface (SPI)
- ROI read out and smart sub-sampling
- Dynamic range: 65.4 dB
- Supplies: 3.3 V
- 49-pin PGA package
- <0.760-W power dissipation

Applications

- Machine Vision (PCB printing)
- Document scanning
- Biometrics (finger printing)
- Digital Photography

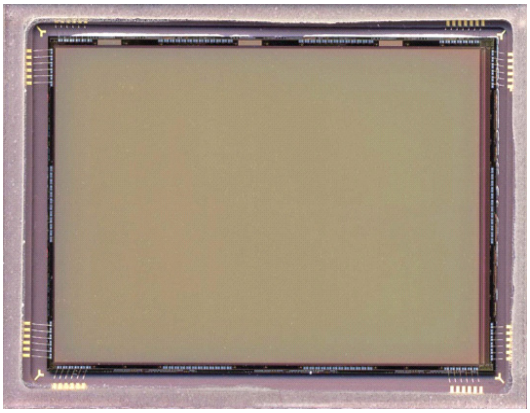
Description

ON Semiconductor IBIS4-14K CMOS image sensor has an image resolution of 3048 by 4560 active pixels. The pixels are 8-µm × 8-µm in size and consist of high sensitivity 3T rolling shutter capability.

The IBIS4-14K is available with 14 Megapixels resolution at 3 fps which makes this product ideal for document scanning, biometrics and low speed machine vision applications.

The IBIS4-14K is housed in a 49-pin ceramic PGA package Contact your local ON Semiconductor representative for more information.

Figure 1. IBIS4-14K Photo



Ordering Information

Marketing Part Number	Description	Package
NOII4SM014KA-GEC	Mono with double-sided AR coating	49-pin PGA

Note Refer to Ordering Code Definition on page 21 for more information.

June, 2011 - Rev. 7

Publication Order Number:
NOII4SM014KA/D

Contents

Specifications

All parameters are measured using the default settings (see recommended operating conditions) unless otherwise specified.

General Specifications

Parameter	Value
Pixel architecture	3T pixel
Technology	CMOS
Pixel size	8-μm × 8-μm
Resolution	3048 × 4560
Power supply	3.3 V
Shutter type	Rolling shutter
Pixel rate	15 MHz nominal
Frame rate at full resolution	3.25 frames/s
Power dissipation	176 mW/53 mA
Dynamic range	65.4 dB
Packaging	49-pins PGA

Electro-Optical Specifications

Parameter	Value
Effective conversion gain [1]	18.5 V/e-
Spectral response × fill factor	0.22 A/W (peak)
Peak quantum efficiency (QE) × fill factor	45% between 500-700 nm range
Full Well Charge [1]	65000 electrons
Linear range	90% of full well charge
Temporal noise (kTC noise limited)	35 electrons
Sensitivity (at 650 nm)	1256 $V.m^2/W.s$
Dynamic range [1]	1857:1 (65.4 dB)
Linear dynamic range [1]	1671:1 (64.5 dB)
Average dark current @ 24 °C	55 pA/cm^2
Dark current signal @ 24 °C	223 electrons/s, 4.13 mV/s
MTF at Nyquist @ 600 nm	0.55 in X, 0.57 in Y
Fixed pattern noise (local 32 x 32 pixel window)	0.11% Vsat RMS
Fixed pattern noise (global)	0.15% Vsat RMS
Photo response non-uniformity (PRNU)	<1% RMS of signal
Anti-blooming	10^5

Table 1. Absolute Maximum Ratings [1]

Symbol	Description	Min	Max	Units
V_{DC}	DC supply voltage	–0.5	4.5	V
V_{IN}	DC input voltage	–0.5	V_{DC} + 0.5	V
V_{OUT}	DC output voltage	–0.5	V_{DC} + 0.5	V
I_{DC}	DC current per pin; any single input or output		±50	mA
T_S[2]	ABS Storage temperature range	0	150	°C
	ABS Storage humidity range	5	90	%RH
Electrostatic discharge (ESD)[2]	Human Body Model (HBM)	JEDEC Rating: Class 0		V
	Charged Device Model (CDM)	JEDEC Rating: Class I		V
LU[2]	Latch-up	IBIS4-14K is not rated for latch-up		mA

Notes
1. Absolute maximum ratings are limits beyond which damage may occur.
2. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. .

Table 2. Recommended Operating Conditions[3], [4], [5]

Parameter	Description	Min	Typ	Max	Unit
T_J[4]	Operating temperature range	0		70	°C
T_S[5]	Storage temperature range	20		40	°C
	Storage humidity range	30		60	%RH
VDD	Nominal power supply	–	3.3	3.6	V
VDDRL VDDRR	Reset power supply level	–	4	–	V
VDD_ARRAY	Pixel supply level	–	3	–	V
DARKREF	Dark reference offset level	1.7	2.65	3	V
GNDAB	Anti-blooming ground level	0	0	1	V
V_{OUT}	Analog output level	0.5	–	3	V
V_{IH}	Logic input high level	2.5	–	3.3	V
V_{IL}	Logic input low level	0	–	1	V

Table 3. Biasing Currents[3], [4], [5]

Pin Number	Pin Name	Connection	Input Current	Pin Voltage
1	OBIAS	10 k to V_{DD}	179 μA	1.51 V
36	CBIAS	22 k to V_{DD}	91 μA	1.29 V
37	PCBIAS	22 k to V_{DD}	91 μA	1.29 V
48	XBIAS	10 k to V_{DD}	181 μA	1.49 V
49	ABIAS	or 10 M to V_{DD}	–	0.8 V

Notes:
3. Settings: VDD = 3.3V, VDDR = 4V and VDD_ARRAY = 3V.
4. Operating ratings are conditions in which operation of the device is intended to be functional.
5. Tolerance on bias reference voltages: ±150 mV due to process variances.

Architecture and Operation

Floor Plan

The architecture of the sensor is shown in the Figure 2. The Y-shift registers point at a row of imager arrays. The imager arrays row is selected by the row drivers or reset by them. There are two Y-shift registers, one points to the row that is read out and the other points to the row to be reset. The second pointer may lead the first pointer by a specific number of rows. In that case, the time difference between both pointers is the integration time. Alternatively, both shift registers can point at the same row for reset and readout for a faster reset sequence. When the row is read out, it is also reset. This is to do double sampling for FPN reduction.

The pixel array of the IBIS4-14000 consists of 4536 × 3024 active pixels and 24 additional columns and rows which can be addressed (see Figure 3). The column amplifiers read out the pixel information and perform the double sampling operation. They also multiplex the signals on the readout buses, which are buffered by the output amplifiers.

The shift registers can be configured for various subsampling modes. The output amplifiers can be individually powered down and some other additional functions are available. These options are configurable using a serial input port.

Figure 2. IBIS4-14K Block Diagram

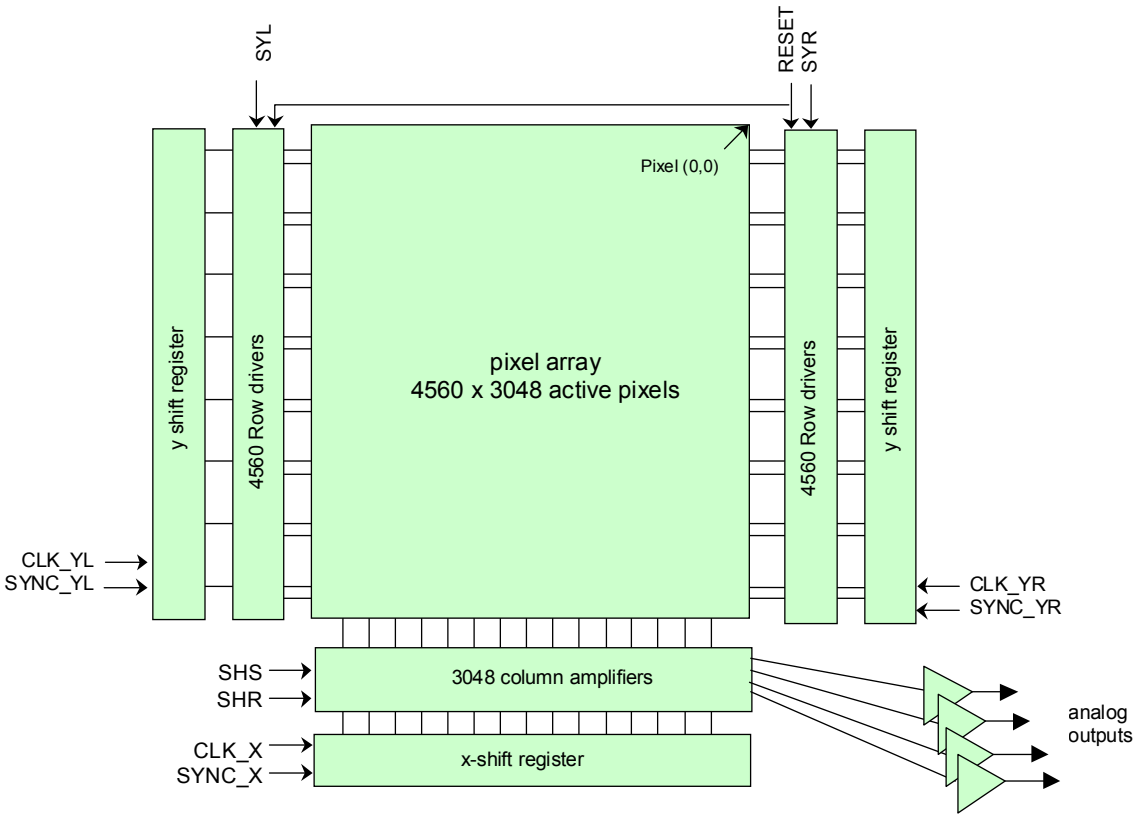
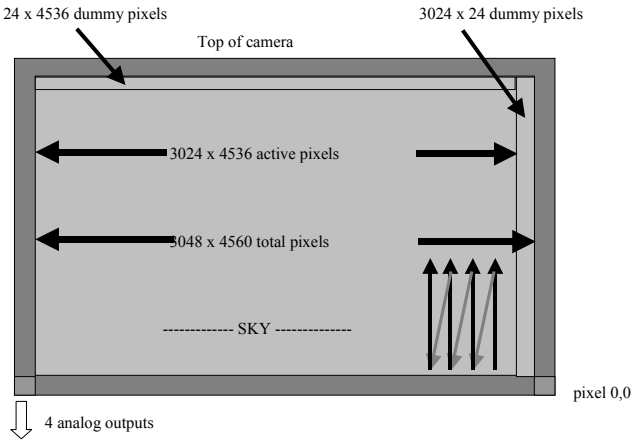


Figure 3. Location of 24 Additional Columns and Rows, Scan Direction of the Array



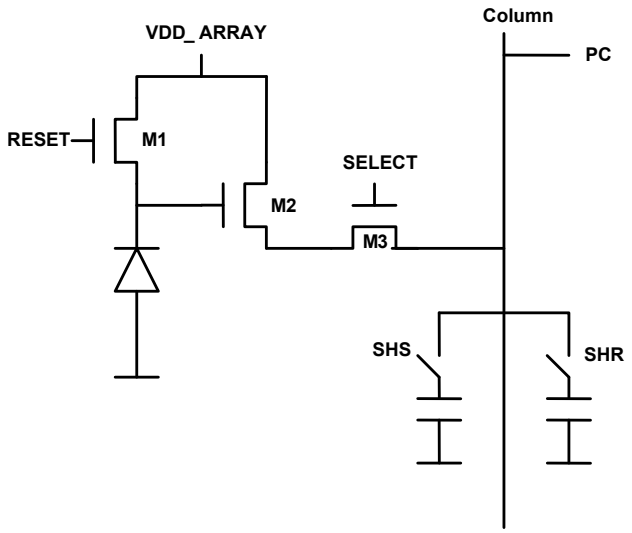
Pixel Specifications

The pixel is a classic three transistor active pixel. The photodiode is a high-fill-factor n-well/p-substrate diode. The chip has separate power supplies for the following:

- General power supply for the analog image core (VDD)
- Power supply for the reset line drivers (VDDR)

Separate power supply for the pixel itself (VDDARRAY).

Figure 4. Pixel and Column Structure Schematic



FPN and PRNU

FPN correction is done on-chip using the double sampling technique. The pixel is read out and this voltage value is sampled on the capacitor SHS. After readout, the pixel is reset again and this value is sampled by SHR. Both sample and reset values of each pixel are subtracted in the column amplifiers to subtract FPN. Raw images taken by the sensor typically feature a residual (local) FPN of 0.11% RMS of the saturation voltage.

The photo response nonuniformity (PRNU), caused by mismatch of photodiode node capacitances, is not corrected on-chip. Measurements indicate that the typical PRNU is less than 1% RMS of the signal level.

Output Stage

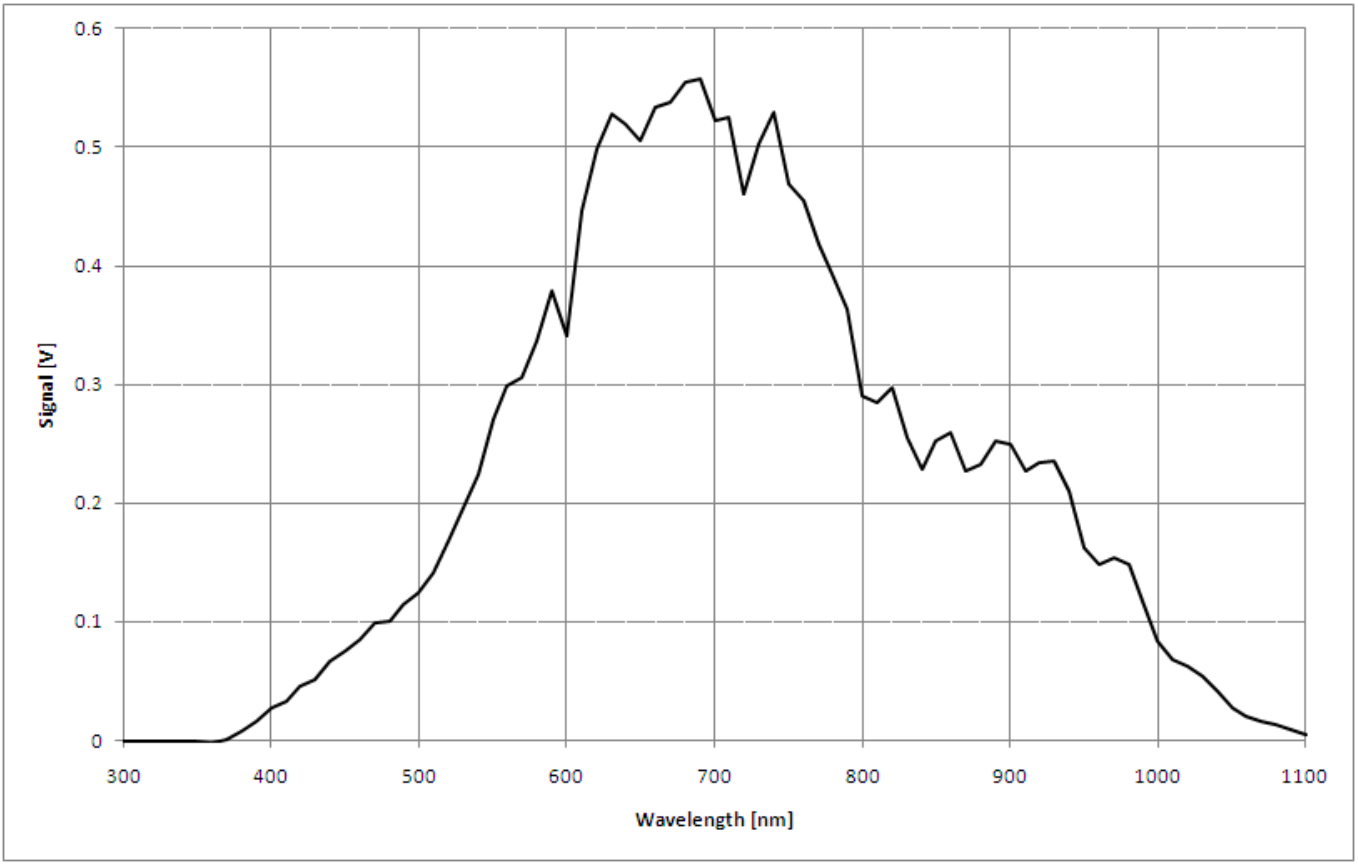
Unity gain buffers are implemented as output amplifiers. These amplifiers can be directly DC-coupled to the analog-digital converter or coupled to an external programmable gain amplifier (PGA).

The dark reference offset of the output signal is adjustable between 1.7 V and 3 V. The amplifier output signal is negative going with increasing light levels, with a maximum amplitude of 1.2 V (at 4 V reset voltage, in hard reset mode). The output signal range of the output amplifiers is between 0.5 V and 3 V.

Notes on analog video signal and output amplifier specifications:

- Video polarity: the video signal is negative going with increasing light level.
- Signal offset: the analog offset of the video signal can be set by an external DC bias (pin 12 DARKREF). The settable range is between 1.7 V and 3 V, with 2.65 V being the nominal expected set point. Hence, the output range (including 1.2 V video signal) is between 3 V and 0.5 V.
- Power control: the output amplifiers can be switched between an ‘operating’ mode and a ‘standby’ mode via the serial port of the imager (see SPI Register on page 13 for the configuration).
- Coupling: the IBIS4-14000 can be DC- or AC-coupled to the A/D converter.

Figure 5. Spectral Response Curve

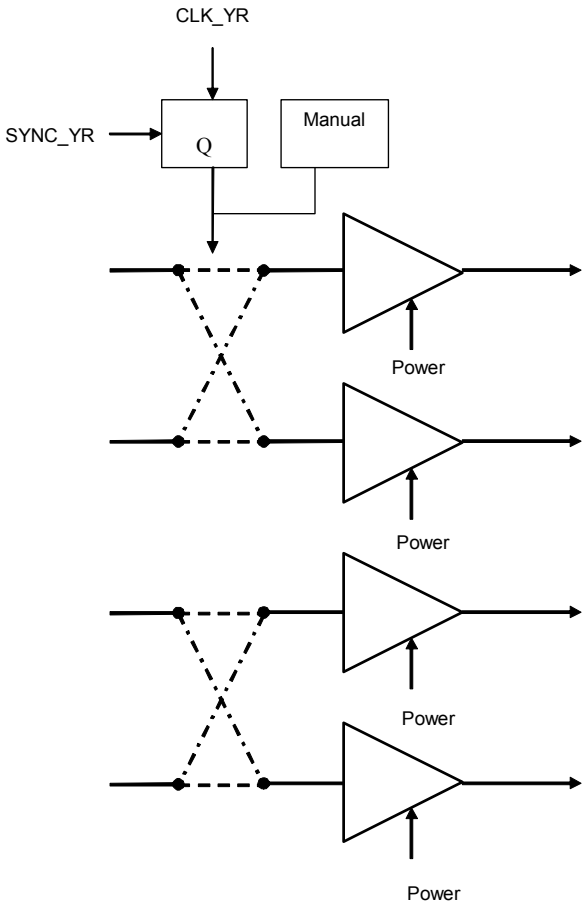


Output Amplifier Crossbar Switch (multiplexer)

A crossbar switch is available that routes the green pixels always to the same output. The switch can be controlled automatically (with a toggle on every CLK_Y rising edge) or manually (through the SPI register).

A pulse on SYNC_Y resets the crossbar switch. The initial state after reset of the switchboard is read from the SPI control register. When the automatic toggling of the switchboard is enabled, it toggles on every rising edge of the CLK_Y clock. Separate pins are used for the SYNC_Y and CLK_Y signals on the crossbar logic these pins can be connected to the SYNC_YL and CLK_YL pins of the shift register that is used for readout as shown in Figure 6.

Figure 6. Output Amplifier Crossbar Switch



Readout and Subsampling Modes

The subsampling modes available on the IBIS4-14000 are summarized in Table 4.

Table 4. Subsampling Modes

Subsampling Modes Programmed into SPI Register		
X-shift register subsampling settings		
Bit-code	**Mode**	**Use**
000 001 010	1:1 Full resolution (all columns)	Full resolution (4 outputs) 4:1 subsampling
011	24:1 Select 4 columns/ skip 20	24:1 subsampling (2 outputs)
100	8:1 Select 4 columns / skip 4s	8:1 subsampling (2 outputs)
101	12:1 Select 4 columns / skip 8	12:1 subsampling (2 outputs)
Y-shift register subsampling settings		
Bit-code	**Mode**	**Use**
000 010 100	4:1 Select 2 rows / skip 2	4:1 subsampling
001	1:1 Full resolution (all rows)	Full resolution
011	6:1 Select 2 rows / skip 4	6:1 subsampling
101	12:1 Select 2 rows / skip 10	12:1 subsampling

Each mode is selected independently for the X-shift and Y-shift registers. The subsampling mode is configured via the serial input port of the chip. The Y-shift and X-shift registers have some difference in subsampling modes because of constraints in the design of the chip.

The baseline full resolution operation mode uses four outputs to read out the entire image. Four consecutive pixels of a row are put in parallel on the four parallel outputs.

Subsampling is implemented by a shift register with hard coded subsample modes. Depending on the selected mode, the shift register skips the required number of pixels when shifting the row or column pointer.

The X-shift register always selects four consecutive columns in parallel. You can subsample in X by activating one of the modes wherein a multiple of four consecutive columns are skipped on a CLK_X pulse. The Y-shift register selects a single row. It consecutively selects two adjacent rows and then skips a set number of rows (the number of rows to skip is set in the subsample mode).

One output can be used and every second row selected by the Y-shift register can be skipped. This doubles the frame rate. Note that for 2 or 1 channel readout, you can power down the not-used output amplifiers through the SPI shift register.

Rows can also be skipped by extra CLK_Y pulses. You do not need to apply additional control pulses to rows that are skipped. This is another way to implement extra subsampling schemes.

For example, to support the 24:1 X-shift register mode vertically, set the Y-shift register to the 12:1 mode and given an additional CLK_Y pulse at the start of each row.

Table 5 lists the frame rates of the IBIS4-14000 in various subsample modes with only one output. The row blanking time (dead time between readout of successive rows) is set to 17.5 s.

Table 5. Frame Rates and Resolution for Various Subsample Modes

Ratio	# Outputs	Image Resolution	Frame rate [frames/s]	Frame readout time [s]
1:1	4	3024 x 4536	3.25	0.308
4:1	1	756 x 1134	12.99	0.077
8:1	1	378 x 567	41.30	0.024
12:1	1	252 x 378	77.13	0.013

Note The 24 additional columns and rows do not subsample (see Figure 3 on page 6).

Sensor Read Out Timing Diagrams

Row Sequencer

The row sequencer controls pulses to be given at the start of each new line. Figure 7 on page 10 shows the timing diagram for this sequence.

The signals to be controlled at each row are:

- CLK_YL and CLK_YR: These are the clocks of the YL and YR shift register. They can be driven by the same signals and at a continuous frequency. At every rising edge, a new row is being selected.
- SELECT: This signal connects the pixels of the currently sampled line with the columns. It is important that PC and SELECT are never active together.
- PC: An initialization pulse that needs to be given to precharge the column.
- SHS (Sample & Hold pixel Signal): This signal controls the track and hold circuits in the column amplifiers. It is used to sample the pixel signal in the columns. (0 = track ; 1 = hold).
- RESET: This pulse resets the pixels of the row that is currently being selected. In rolling shutter mode, the RESET signal is pulsed a second time to reset the row selected by the YR shift register. For “reset black” dark reference signals, the reset pulse can be pulsed also during the first PC pulse. Normally, the rising edge of RESET and the falling edge of PC occur at the same position. The falling edge of RESET lags behind the rising PC edge.
- SHR (Sample & Hold pixel Reset level): This signal controls another track and hold circuit in the column amplifiers. It is used to sample the pixel reset level in the columns (for double sampling). (0 = track ; 1 = hold).
- SYL (Select YL register): Selects the YL shift register to drive the reset line of the pixel array.
- SYR (Select YR register): Selects the YR shift register to drive the reset line of the pixel array. For rolling shutter applications, SYL and SYR are complementary. In full frame readout, both registers may be selected together, only if it is guaranteed that both shift registers point to the same row. This can reduce the row blanking time.
- SYNC_YR and SYNC_YL: Synchronization pulse for the YR and YL shift registers. The SYNC_YR/SYNC_YL signal is clocked in during a rising edge on CLK_YR/CLK_YL and resets the YR/YL shift register to the first row. Both pulses are pulsed only once each frame. The exact pulsing scheme depends on the mode of use (full frame/ rolling shutter). A 200 ns setup time applies. See Table 6 on page 10.
- SYNC_X: Resets the column pointer to the first row. This has to be done before the end of the first PC pulse in case the previous line has not been read out completely.

Figure 7 shows the basic timing diagram of the IBIS4-14000 image sensor and Table 6 on page 10 shows the timing specifications of the clocking scheme.

Figure 7. Line Read Out Timing

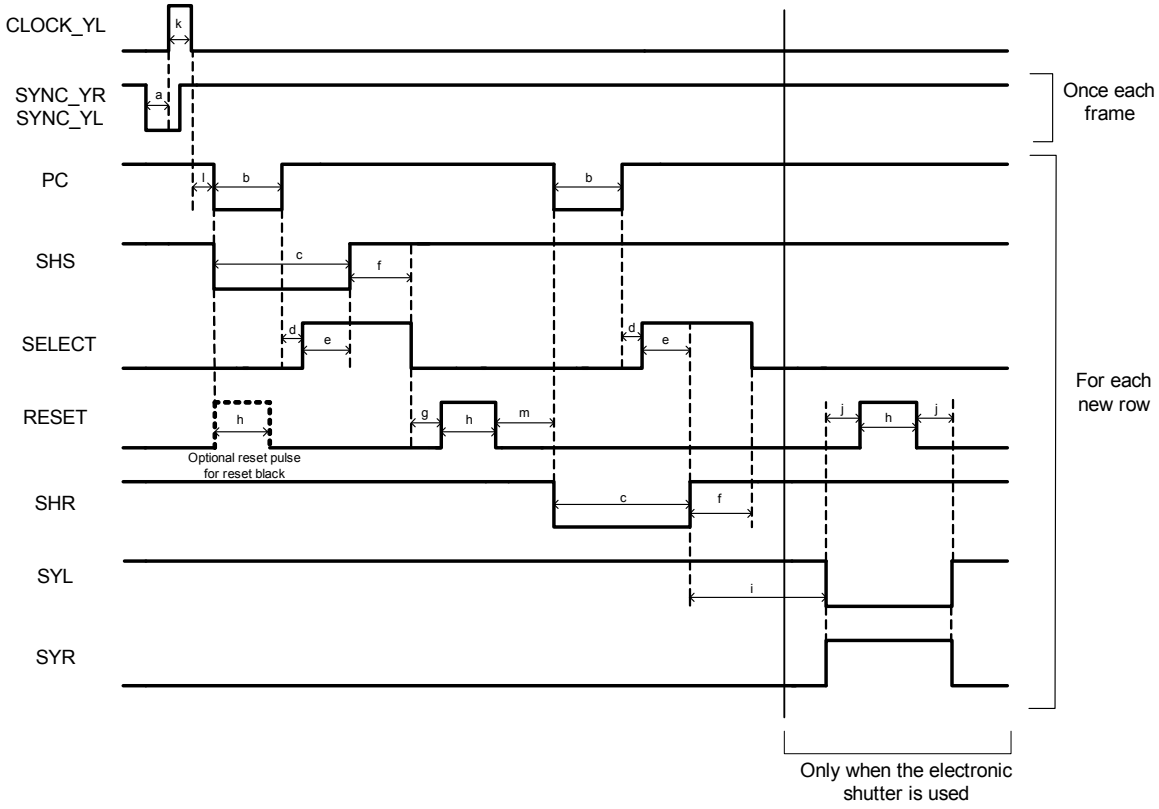


Table 6. Timing Constraints for the Row Sequencer

Symbol	Min	Typ	Units	Description
a	200	600	ns	Min. SYNC set-up times. SYNC_Y is clocked in on rising edge on CLK_Y. SYNC_Y pulse must overlap CLK_Y by one clock period. Setup times of 200 ns apply after SYNC edges. Within this setup time no rising CLK edge may occur.
b	–	2.7	µs	Duration of PC pulse.
c	–	10	µs	Delay between falling edge on PC and rising edge on SHS/SHR. Duration of SHS/SHR pulse.
d	–	1.3	µs	Delay between rising edge on PC and rising edge on SELECT.
e	–	6.5	µs	Delay between rising edge on SELECT and rising edge on SHS/SHR.
f	–	100	ns	Delay between rising edge on SHS and falling edge on SELECT.
g	–	1.4	µs	Delay between falling edge of SELECT and rising edge of RESET.
h	–	5	µs	Duration of RESET pulse.
i	–	1.28	µs	Delay between rising edge on SHR and rising edge on SYR.
j	h+2*CLK	500	ns	SYL and SYR pulses must overlap second RESET pulse at both sides by one clock cycle.
k	–	240	ns	Duration of CLOCK_Y pulse.
l	–	3	µs	Delay between falling edge of CLK_Y and Falling edge of PC and SHS.
m	–	500	ns	Delay between falling edge of RESET and falling edge of PC and SHR.

Notes CLK = one clock period of the master clock, shortest system time period available.

In Figure 7 on page 10 timing diagram, the YR shift register is used for the electronic shutter. The CLK_YR is driven identically as CLK_YL. The SYNC_YR pulse leads the SYNC_YL pulse by a given number of rows. Relative to the row timing, both SYNC pulses are given at the same time position.

SYNC_YR and SYNC_YL are only pulsed once each frame, SYNC_YL is pulsed when the first row is read out and SYNC_YR is pulsed for the electronic shutter at the appropriate moment.

This timing assumes that the registers that control the subsampling modes have been loaded in advance (through the SPI interface), before the pulse on SYNC_YL or SYNC_YR.

The second reset pulse and the pulses on SYL and SYR (all pulses drawn in red) are only applied when the rolling electronic shutter is used. For full frame integration, these pulses are skipped.

The SYNC_Y pulse is also used to initialize the switchboard (output multiplexer). This is also done by a synchronous reset on the rising edge of CLK_Y. Normally the switchboard is controlled by the shift register used for readout (this is the YL shift register). This means that pin SYNC_Y can be connected to SYNC_YL, and pin CLK_Y can be connected to CLK_YL.

The additional RESET BLACK pulse (indicated in dashed lines in Figure 7 on page 10) can be given to make one or more lines black. This is useful to generate a dark reference signal.

Timing Pulse Pattern for Readout of a Pixel

Figure 8 shows the timing diagram to preset (sync) the X shift register, read out the image row, and analog-digital conversion. There are 3 tasks:

- Preset the X shift register: Apply a low level to SYNC_X during a rising edge on CLK_X at the start of a new row
- Readout of the image row: Pulse CLK_X
- Analog-digital conversion: Clock the ADC

The SYNC pulses perform a synchronous reset of the shift registers to the first row/column on a rising edge on CLK. This is identical for all shift registers (YR, YL and X).

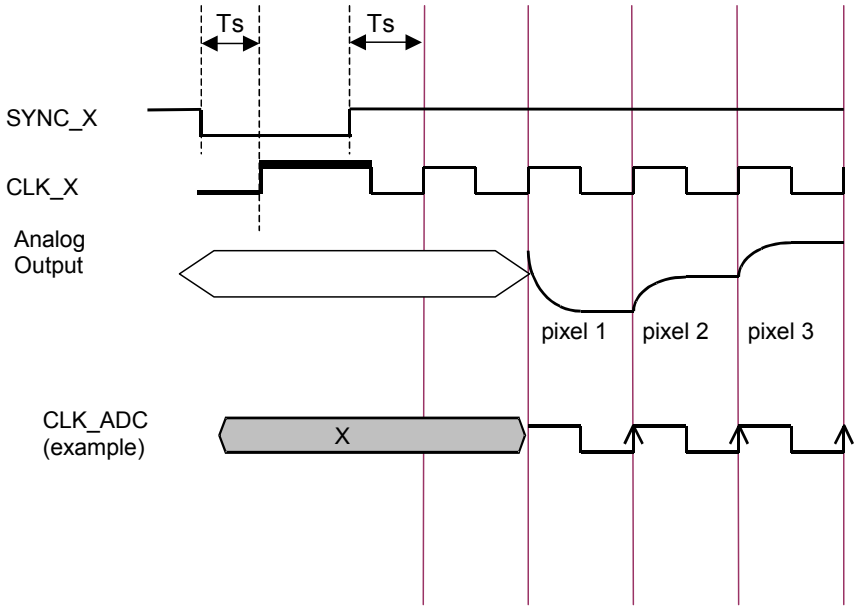
Note The SYNC_X signal has a setup time Ts of 150 ns. For the YR and YS shift registers, the setup time is 200 ns. CLK_X must be stable at least during this setup time.

If a partial row readout is performed, 2 CLK_X pulses (with SYNC_X = LOW) are required to fully deselect the column where the X pointer is stopped. A single CLK_X leaves the column partially selected which then has a different response when read out in the next row.

When full row readout is performed, the last column is fully deselected by a single CLK_X pulse (with SYNC_X = LOW). The X-register is reset by a single CLK_X pulse (with SYNC_X = LOW). In case of partial row readout, give the SYNC_X pulse before the sample pulses (SHR and SHS) of the process to avoid a different response of the last column of the previous window.

For the X shift register the analog signal is delayed by 2 clock periods before it becomes available at the output (due to internal processing of the signal in the columns and output amplifier). Figure 8 gives an example of an ADC clock for an ADC that samples on the rising edge.

Figure 8. Row Readout Timing Sequence



Fast Frame Reset Timing Diagram

Figure 9 shows the reset timing for a fast frame reset.

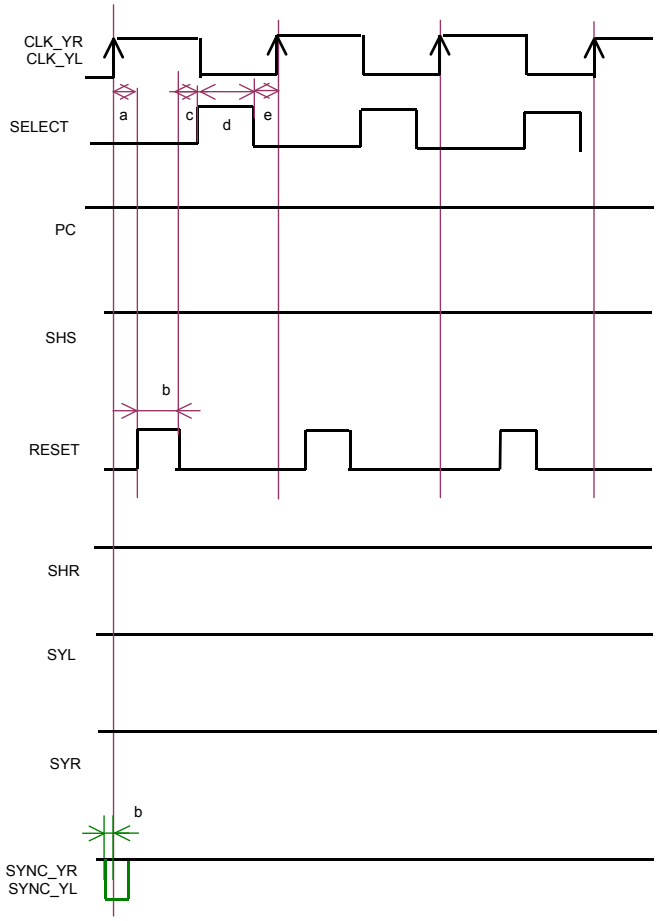
Keep both SYL and SYR high to speed up the reset mechanism and reduce propagation delays. PC, SHS, SHR can be kept high since they do not interact with the pixel reset mechanism.

Table 7 lists the timing specifications for RESET, CLK_Y and SELECT.

Table 7. Fast Reset Timing Constraints

Symbol	Typical	Description
a	0 μs	Delay between rising CLK_Y edge and Reset.
b	4 μs	Reset pulse width.
c	0	Reset hold time.
d	1.6 μs	Select pulse width.
e	1 μs	Setup hold time. CONSTRAINT: a + e > 1 us due to propagation delay on pixel select line.

Figure 9. Fast Reset Sequence Timing



SPI Register

SPI Interface Architecture

The elementary unit cell of the serial to parallel interface consists of two D-flip-flops. The architecture is shown in Figure 10. 16 of these cells are connected in parallel, having a common /CS and SCLK form the entire uploadable parameter block, where D_{in} is connected to D_{out} of the next cell. The uploaded settings are applied to the sensor on the rising edge of signal /CS.

Figure 10. SPI Interface

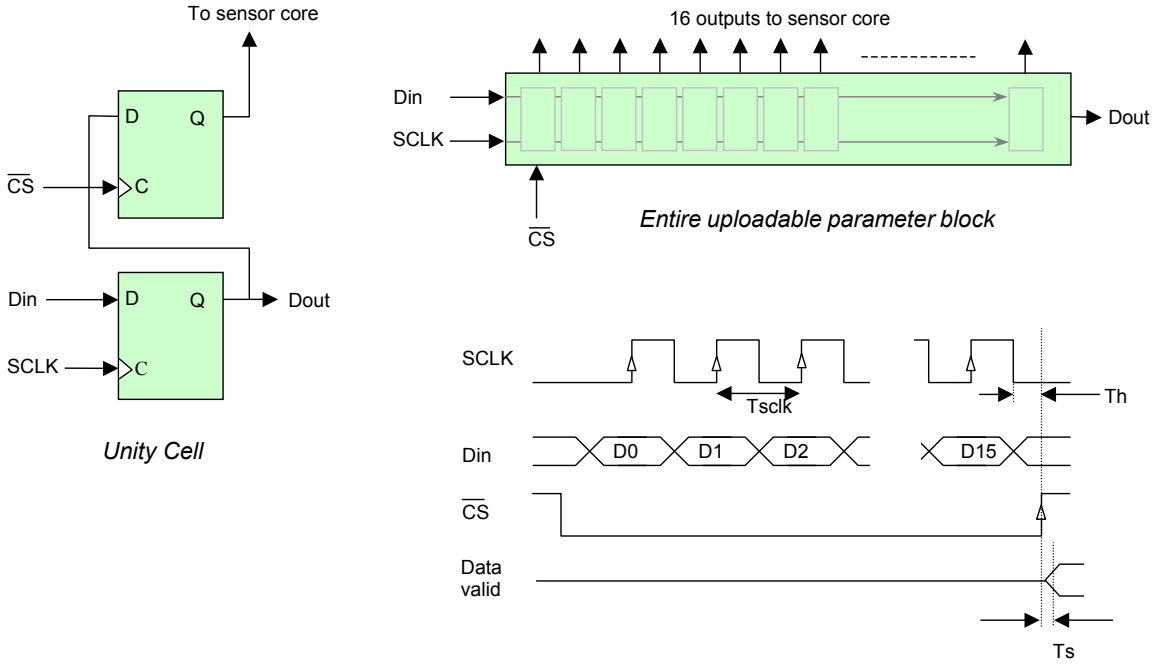


Table 8. Timing Requirements Serial Parallel Interface

Parameter	Value
Tsclk	100 ns
Ts	50 ns
Th	50 ns

SPI Register Definition

Sensor parameters can be serially uploaded inside the sensor at the start of a frame. The parameters are:

- Subsampling modes for X and Y-shift registers (3-bit code for six subsampling modes)
- Power control of the output amplifiers, column amps and pixel array. Each amplifier can be individually powered up/down
- Output crossbar switch control bits. The crossbar switch is used to route the green pixels to the same output amplifiers at all times. A first bit controls the crossbar. When a second bit is set, the first bit toggles on every CLK_Y edge to automatically route the green pixels of the bayer filter pattern.

The code is uploaded serially as a 16-bit word (LSB uploaded first).

Table 9 on page 14 lists the register definition. The default code for a full resolution readout is 33342 (decimal) or 1000 0010 0011 1110.

Table 9. Serial Sensor Parameters Register Bit Definitions

BIT	Description'
0 (LSB)	set to zero (0).
1	1 = power on sensor array ; 0 = power-down.
2	1 = power up output amplifier 4; 0 = power-down.
3	1 = power up output amplifier 3; 0 = power-down.
4	1 = power up output amplifier 2; 0 = power-down.
5	1 = power up output amplifier 1; 0 = power-down.
6 7 8	3-bit code for subsampling mode of X shift register: 000 = full resolution 011 = select 4, skip 20 001 = full resolution 100 = select 4, skip 4 010 = full resolution 101 = select 4, skip 8
9 10 11	3-bit code for subsampling mode of Y-shift registers: 000 = select 2, skip 2 011 = select 2, skip 4 001 = full resolution 100 = select 2, skip 2 010 = select 2, skip 2 101 = select 2, skip 2
12	Crossbar switch (output multiplexer) control bit initial value. This initial value is clocked into the crossbar switch at a SYNC_YR rising edge pulse (when the array pointers jump back to row 1). The crossbar switch control bit selects the correspondence between multiplexer busses and output amplifiers. Bus-to-output correspondence is according to the following table: **Bus** **when bit set to 0** **when bit set to 1** 1 output 1 output 2 2 output 2 output 1 3 (4 outputs) output 3 output 4 4 (4 outputs) output 4 output 3
13	1 = Toggle crossbar switch control bit on every odd/even line. In order to let green pixels always use the same output amplifier automatically, this bit must be set to 1. On every CLK_Y rising edge (when a new row is selected), the crossbar switch control bit will toggle. Initial value (after SYNC_Y) is set by bit 12.
14	Not used.
15 (MSB)	1 = Power-up sensor array; 0 = Power-down.

Three pins are used for the serial data interface. This interface converts the serial data into an (internal) parallel data bus (Serial-Parallel Interface or SPI). The control lines are:

■ DATA: The data input. LSB is clocked in first.

■ CLK: Clock, on each rising edge, the value of DATA is clocked in

■ CS: Chip select, a rising edge on CS loads the parallelized data into the on-chip register.

The initial state of the register is undefined. However, no state exists that destroys the device.

Package Information

Pin Configuration

Table 10 lists the pin configuration of the IBIS4-14000. Figure 12 on page 18 shows the assignment of pin numbers on the package.

Table 10. Pinout Configuration

Pin #	Name	Function	Comment
1	OBIAS	Bias current output amplifiers	Connect with 10 kΩ to V_{DD} and decouple with 100 nF to GND
2	GND	Ground for output 3	
3	OUT3	Output 3	
4	GND	Ground for output 4	
5	OUT4	Output 4	
6	VDD	Power supply	Nominal 3.3 V
7	GND	Ground	0 V
8	OUT2	Output 2	
9	GND	Ground for output 2	
10	OUT1	Output 1	
11	GND	Ground for output 1	
12	DARKREF	Offset level of output signal	Typ. 2.6 V. min. 1.7 V max. 3 V
13	TEMP1	Temperature sensor. Located near the output amplifiers (pixel 4536, 0) near the stitch line)	Any voltage above GND forward biases the diode. Connect to GND if not used
14	PHDIODE	Photodiode output. Yields the equivalent photocurrent of 250 x 50 pixels. Diode is located right under the pad	Reverse biased by any voltage above GND Connect to GND if not used.
15	CLK_Y	Y clock for switchboard	Clocks on rising edge Connect to CLK_YL (or drive identically)
16	SYNC_Y	Y SYNC pulse for switchboard	Low active: synchronous sync on rising edge of CLK_Y Connect to SYNC_YL (or drive identically)
17	TEMP2	Temperature sensor Located near pixel (24,0)	Any voltage above GND forward biases the diode Connect to GND if not used
18	GNDAB	Anti-blooming reference level (= pin 33)	Typ. 0 V. Set to 1.5 V for improved anti-blooming
19	GND	Ground	0 V
20	VDD	Power supply	Nominal 3.3 V
21	VDDR	Power supply for reset line drivers	Nominal 4 V Connected on-chip to pin 30
22	CLK_YR	Clock of YR shift register	Shifts on rising edge
23	SYR	Activate YR shift register for driving of reset and select line of pixel array	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected
24	SYNC_YR	Sets the YR shift register to row 1	Low active. Synchronous sync on rising edge of CLK_YR 200 ns setup time
25	VDDARRAY	Pixel array power supply (= pin 26)	3 V
26	VDDARRAY	Pixel array power supply (= pin 25)	3 V
27	SYNC_YL	Sets the YL shift register to row 1	Low active. Synchronous sync on rising edge of CLK_YL 200 ns setup time
28	SYL	Activate YL shift register for driving of reset and select line of pixel array	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected

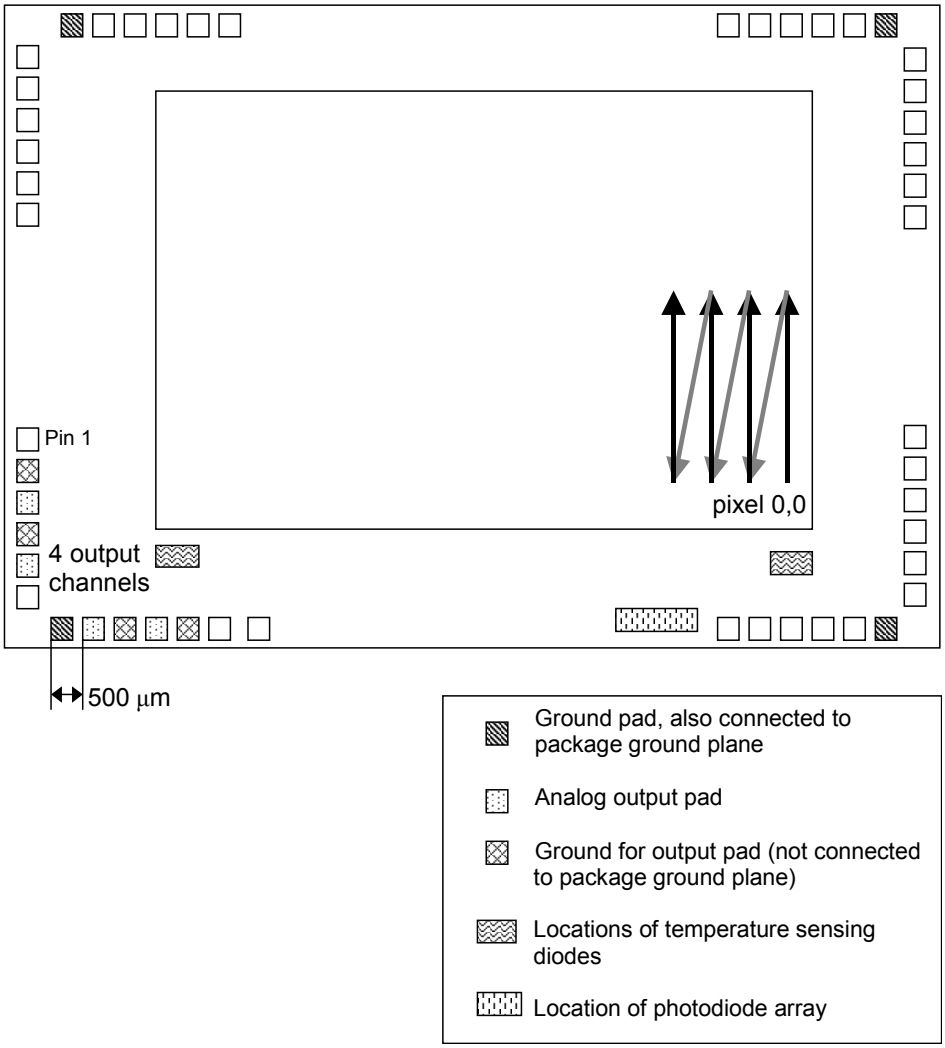
Table 10. Pinout Configuration(continued)

Pin #	Name	Function	Comment
29	CLK_YL	Clock of YL shift register	Shifts on rising edge
30	VDDR	Power supply for reset line drivers	Nominal 4 V Connected on-chip to pin 21
31	VDD	Power supply	Nominal 3.3 V
32	GND	Ground	0 V
33	GNDAB	Anti-blooming reference level (pin 33)	Typ. 0 V. Set to 1 V for improved anti-blooming
34	SELECT	Control select line of pixel array	High active. See timing diagrams
35	RESET	Reset of the selected row of pixels	High active. See timing diagrams
36	CBIAS	Bias current column amplifiers	Connect with 22 kΩ to V_{DD} and decouple with 100 nF to GND
37	PCBIAS	Bias current	Connect with 22 kΩ to V_{DD} and decouple with 100 nF to GND
38	DIN	Serial data input	16-bit word. LSB first
39	SCLK	SPI interface clock	Shifts on rising edge
40	CS	Chip select	Data copied to registers on rising edge
41	PC	Row initialization pulse	See timing diagrams
42	SYNC_X	Sets the X-shift register to row 1	Low active. Synchronous sync on rising edge of CLK_X 150 ns setup time
43	GND	Ground	0 V
44	VDD	Power supply	Nominal 3.3 V
45	CLK_X	Clock of YR shift register	Shifts on rising edge
46	SHR	Row track and hold reset level (1 = hold; 0 = track).	See timing diagram
47	SHS	Row track and hold signal level (1 = hold; 0 = track)	See timing diagram
48	XBIAS	Bias current X multiplexer	Connect with 10 kΩ to V_{DD} and decouple with 100 nF to GND
49	ABIAS	Bias current pixel array	Connect with 10 MΩ to V_{DD} and decouple with 100 nF to GND

Geometry and Mechanical

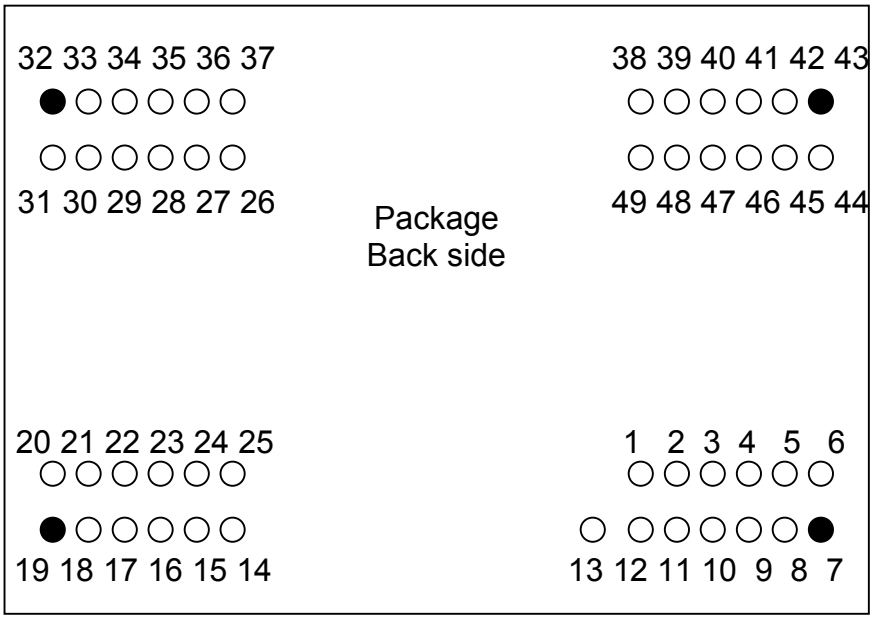
Die Geometry

Figure 11. Die Geometry and Location of Pixel (0,0)



Pin Number Assignment

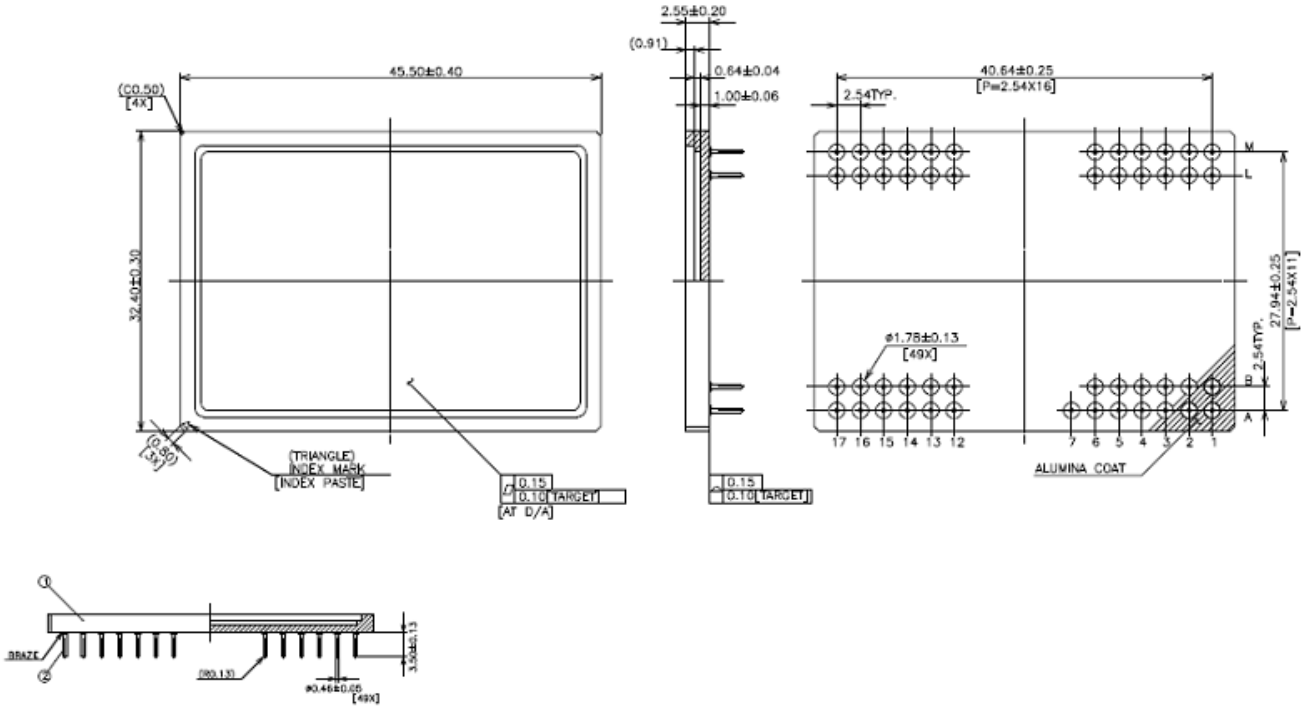
Figure 12. Pin Number Assignment



Note Pins in black are connected to die attach area for a proper ground plane.

Package Diagram

Figure 13. Package Dimensions



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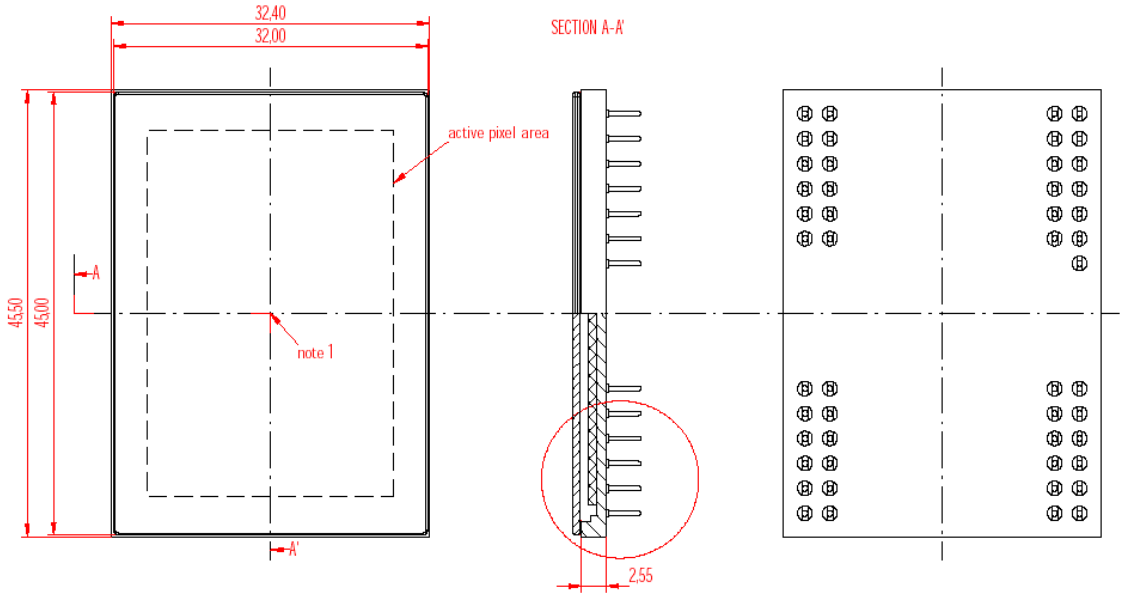
Die Placement Dimensions and Accuracy

Figure 14. Die Placement



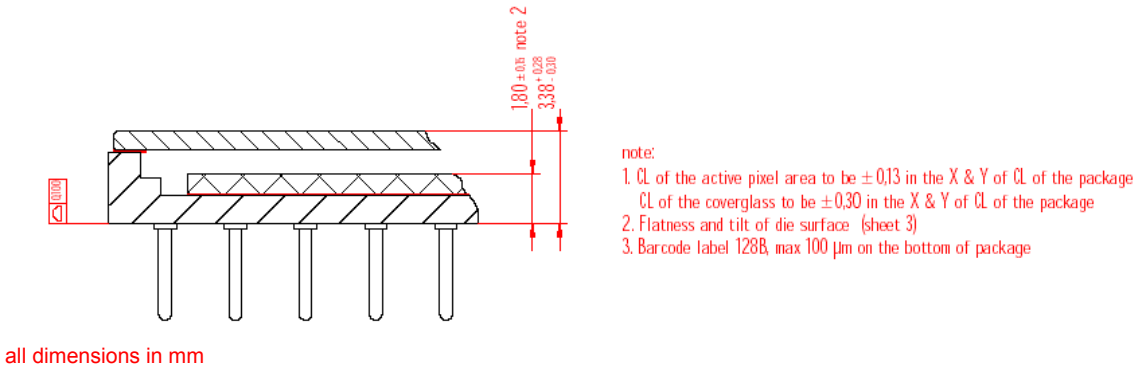
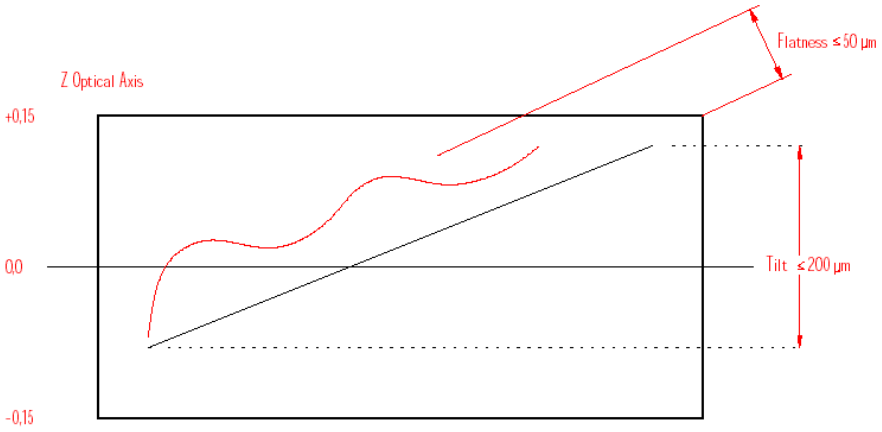


Figure 15. Tolerances



Glass Lid

The CYII4SM014KAA-GEC device uses the glass lid with double sided AR coating.

Handling Precautions

For proper handling and storage conditions, refer to the ON Semiconductor application note AN52561.

Limited Warranty

ON Semiconductor Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within two (2) years period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

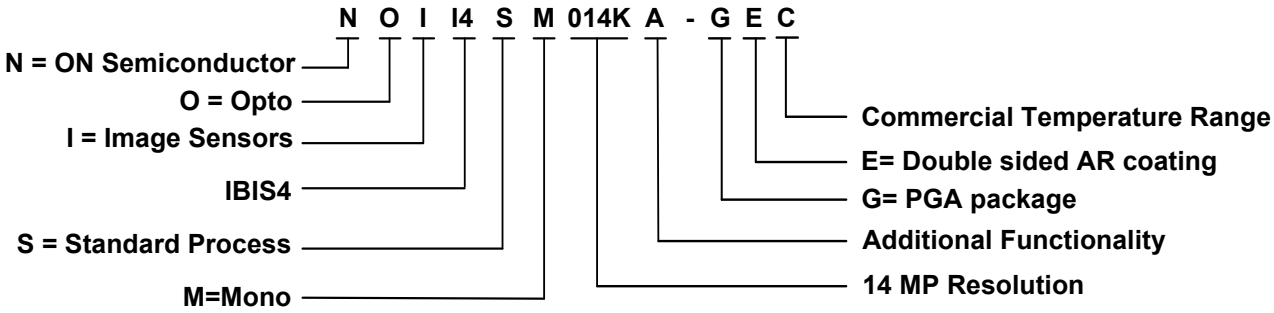
Return Material Authorization (RMA)

ON Semiconductor packages all of its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

Acceptance Criteria Specification

The Product Acceptance Criteria is available on request. This document contains the criteria to which the IBIS4-14000 is tested before being shipped.

Ordering Code Definition



Acronyms

Acronym	Description
ADC	analog-to-digital converter
AFE	analog front end
ANSI	American National Standards Institute
BGA	ball grid array
BL	black pixel data
CDM	Charged Device Model
CDS	correlated double sampling
CIS	CMOS image sensor
CMOS	complementary metal oxide semiconductor
CMY	cyan magenta yellow
CRC	cyclic redundancy check
DAC	digital-to-analog converter
DDR	double data rate
DFT	design for test
DNL	differential nonlinearity
DSNU	dark signal nonuniformity
EIA	Electronic Industries Alliance
ESD	electrostatic discharge
FE	frame end
FF	fill factor
FOT	frame overhead time
FPN	fixed pattern noise
FPS	frames per second
FS	frame start
HBM	Human Body Model
HMUX	horizontal multiplexer
I2C	inter-integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
IMG	regular pixel data

Acronym	Description
INL	integral nonlinearity
IP	intellectual property
JTAG	Joint Test Action Group
LE	line end
LS	line start
LSB	least significant bit
LVDS	low-voltage differential signaling
MBS	mixed boundary scan
MSB	most significant bit
MTF	modulation transfer function
NDR	nondestructive readout
NIR	near infrared
PGA	programmable gain amplifier
PLS	parasitic light sensitivity
PRBS	pseudo-random binary sequence
PRNU	pixel random nonuniformity
QE	quantum efficiency
RGB	red green blue
RMS	root mean square
ROI	region of interest
ROT	row overhead time
S/H	sample and hold
SNR	signal-to-noise ratio
SPI	serial peripheral interface
TAP	test access port
TBD	to be determined
TIA	Telecommunications Industry Association
TR	training pattern
uPGA	micro pin grid array

Glossary

blooming	The leakage of charge from a saturated pixel into neighboring pixels.
camera gain constant	A constant that converts the number of electrons collected by a pixel into digital output (in DN). It can be extracted from photon transfer curves.
column noise	Variation of column mean signal strengths. The human eye is sensitive to line patterns so this noise is analyzed separately.
conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
CFA	Color filter array. The materials deposited on top of pixels that selectively transmit color.
color crosstalk	The leakage of signal from one color channel into another when the imager is NOT saturated. The signal can leak through either optical means, in which a photon enters a pixel of the ‘wrong’ color, or electrical means, in which a charge carrier generated within one pixel diffuses into a neighboring pixel.
CRA	Chief ray angle. Oblique rays that pass through the center of a lens system aperture stop. Color filter array, metal, and micro lens shifts are determined by the chief ray angle of the optical system. In general, optical systems with smaller CRA are desired to minimize color artifacts
DN	Digital number. The number of bits (8, 12, 14, …) should also be specified.
DNL	Differential nonlinearity (for ADCs)
DSNU	Dark signal nonuniformity. This parameter characterizes the degree of nonuniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
grating monochromator	An instrument that produces a monochromatic beam of light. It typically consists of a broadband light source such as a tungsten lamp and a diffraction grating for selecting a particular wavelength.
INL	Integral nonlinearity (for ADCs)
luminance	Light flux per unit area in photometric units (lux)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
irradiance	Light flux per unit area in radiometric units (W/m^2)
Lag	The persistence of signal after pixel reset when the irradiance changes from high to low values. In a video stream, lag appears as ‘ghost’ images that persist for one or more frames.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 $lumen/m^2$ = 1/683 W/m^2)
NIR	Near Infrared. NIR is part of the infrared portion of the spectrum and has wavelengths in the approximate range 750 nm to 1400 nm.
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
photon transfer	Measurement in which a bare imager (no external lens) is irradiated with uniform light from dark to saturation levels. Typically the source is collimated, monochromatic 550 nm light. Chapter 2 of J. Janesick's book, *Scientific Charge Coupled Devices,* describes the technique in detail.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response nonuniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
radiometric units	Units for light measurement based on physics.

read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. Soft reset occurs when the reset transistor is operated below the threshold. Hard reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
reverse saturation	Phenomenon in which the signal level decreases with increasing light intensity. It typically occurs at irradiance levels much higher than saturation, such as an image taken of the sun.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
row noise	Variation of row mean signal strengths. The human eye is sensitive to line patterns, so this noise is analyzed separately.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux = 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
shot noise	Noise that arises from measurements of discretised quanta (electrons or photons). It follows a Poisson distribution with the strength of the noise increasing as the square root of the signal.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.
tint	Integration time.

Document History Page

Document Title: NOII4SM014KA IBIS4-14000 14-MegaPixel CMOS Image Sensor				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	310213	SIL	See ECN	Initial release
*A	428177	FVK	See ECN	Layout converted Figure 8 on page 11 updated Storage and handling section added IBIS4-14000-C added
*B	642656	FPW	See ECN	Ordering information update+package spec label. Moved figure captions to the top of the figures and moved notes to the bottom of the page per new template. Verified all cross-referencing. Moved the specifications towards the back. Corrected all variables on the Master pages.
*C	2220967	FPW	See ECN	Eval kit section is removed. Reference to Defect Spec is added. Defect description for a RCCA added.
*D	2765859	NVEA	09/18/09	Updated Ordering Information table
*E	3007128	NVEA	08/13/10	Updated Ordering Information table. Added Acronyms, Ordering Code Definition, and Glossary sections. Updated package diagram.
*F	3048272	NVEA	10/7/2010	Updated Ordering Information table. Pruned High grade version. Removed reference to color MPN. Edited Spectral Response Curve. Revised section on Glass Lid and Ordering Code Definition.
7	N/A	SKW	06/03/2011	Conversion to ON Semiconductor format and orderable part number changes.

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