

NTGS3A033PZ

MOSFET – Power, Single, P-Channel, TSOP-6 -20 V, -5.9 A

Features

- Leading -20 V Trench for Low $R_{DS(on)}$
- -1.8 V Rated for Low Voltage Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch
- High Side Load Switch
- Charging Circuits and Battery Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V_{GS}	± 8	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-5.1	A
			$T_A = 85^\circ\text{C}$	-3.7	
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	-5.9		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	1.19	W
			$t \leq 5\text{ s}$	1.58	
Continuous Drain Current (Note 2)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-3.8	A
			$T_A = 85^\circ\text{C}$	-2.7	
Power Dissipation (Note 2)		P_D	$T_A = 25^\circ\text{C}$	0.65	W
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$	I_{DM}	-20	A	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	79	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	192	

1. Surface-mounted on FR4 board using 1 in. sq. pad size (Cu area = 1.127 in. sq., 2 oz).
2. Surface-mounted on FR4 board using minimum pad size (Cu area = 0.0775 in. sq.).

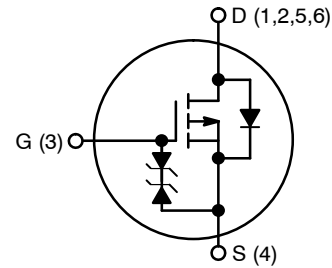


ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D MAX
-20 V	22 m Ω @ -4.5 V	-5.9 A
	29 m Ω @ -2.5 V	
	40 m Ω @ -1.8 V	

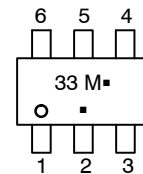
P-Channel MOSFET



MARKING DIAGRAM



TSOP-6
CASE 318G



33 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTGS3A033PZT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}, \text{ref to } 25^\circ\text{C}$		21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$	$T_J = 25^\circ\text{C}$		-1	μA
			$T_J = 85^\circ\text{C}$		-10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -5.1\text{ A}$		22	33	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -4.5\text{ A}$		29	40	
		$V_{GS} = -1.8\text{ V}, I_D = -1.5\text{ A}$		40	55	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -5.1\text{ A}$		23		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$		1870		pF
Output Capacitance	C_{oss}			203		
Reverse Transfer Capacitance	C_{rss}			174		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -5.1\text{ A}$		18.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.0		
Gate-to-Source Charge	Q_{GS}			2.7		
Gate-to-Drain Charge	Q_{GD}			5.0		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -1.0\text{ A}, R_G = 6.0\ \Omega$		9.4		ns
Rise Time	t_r			9.3		
Turn-Off Delay Time	$t_{d(off)}$			131		
Fall Time	t_f			56		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.7\text{ A}$	$T_J = 25^\circ\text{C}$		-0.7	-1.2	V
			$T_J = 125^\circ\text{C}$		-0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -1.7\text{ A}$		26		ns	
Charge Time	t_a			9.0			
Discharge Time	t_b			17			
Reverse Recovery Charge	Q_{RR}			11			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ ms}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

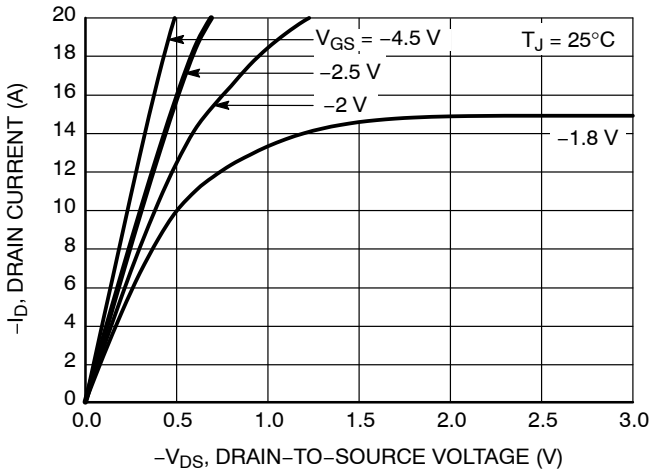


Figure 1. On-Region Characteristics

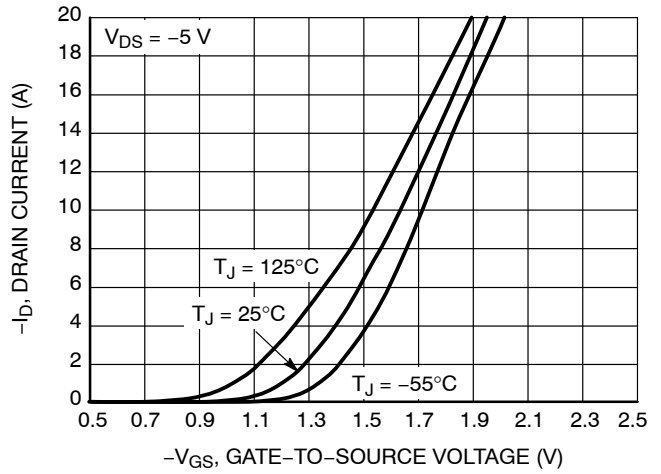


Figure 2. Transfer Characteristics

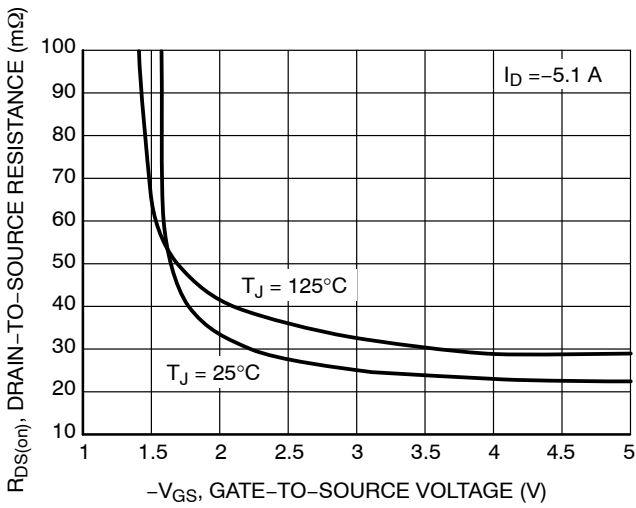


Figure 3. On-Resistance vs. Gate-to-Source Voltage

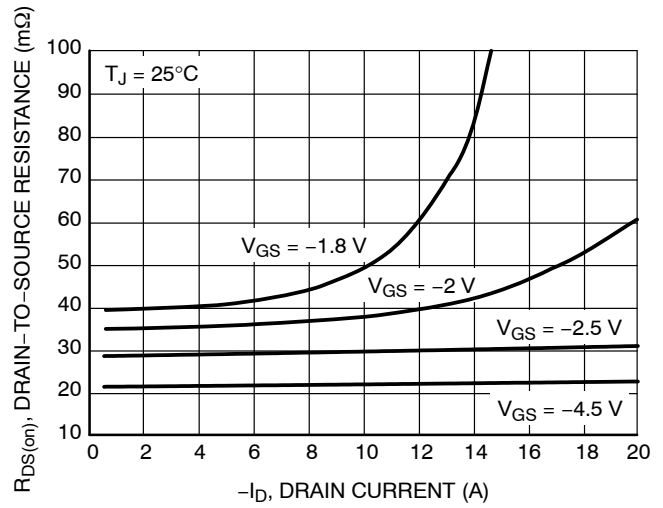


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

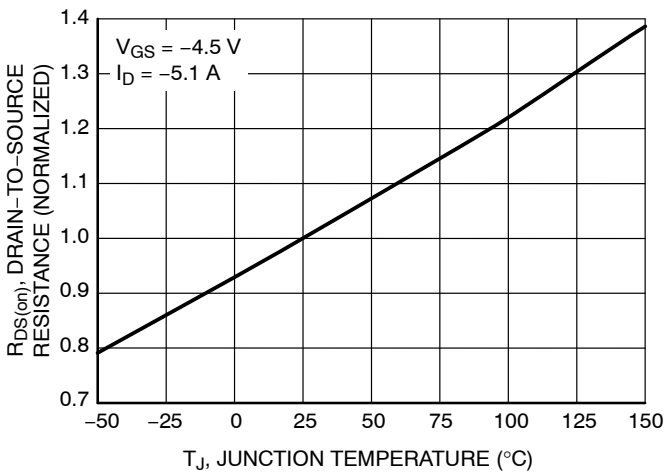


Figure 5. On-Resistance Variation with Temperature

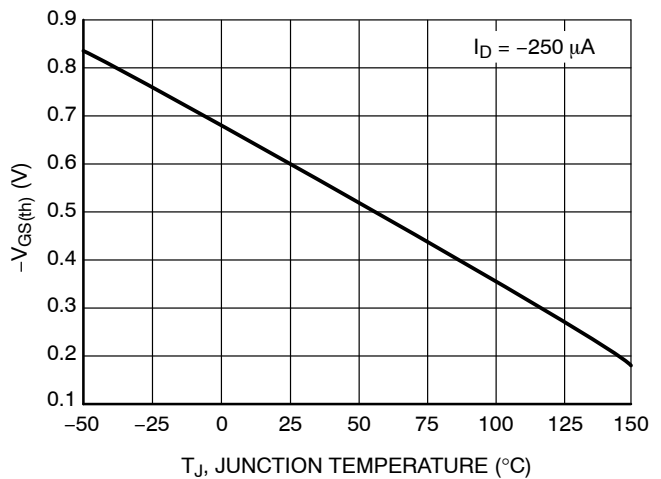


Figure 6. Threshold Voltage Variation with Temperature

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TYPICAL CHARACTERISTICS

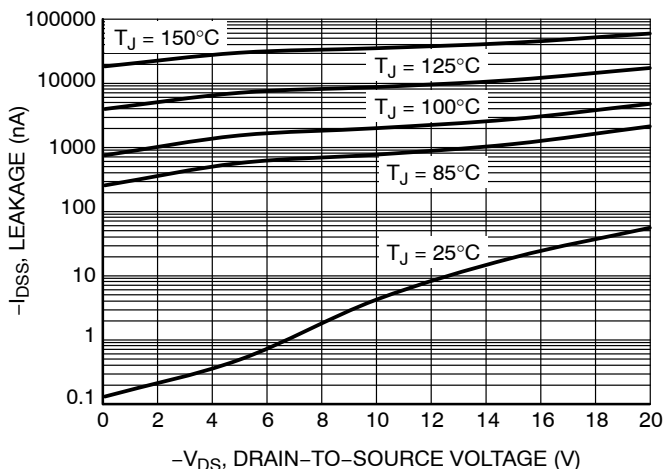


Figure 7. Drain-to-Source Leakage Current vs. Voltage

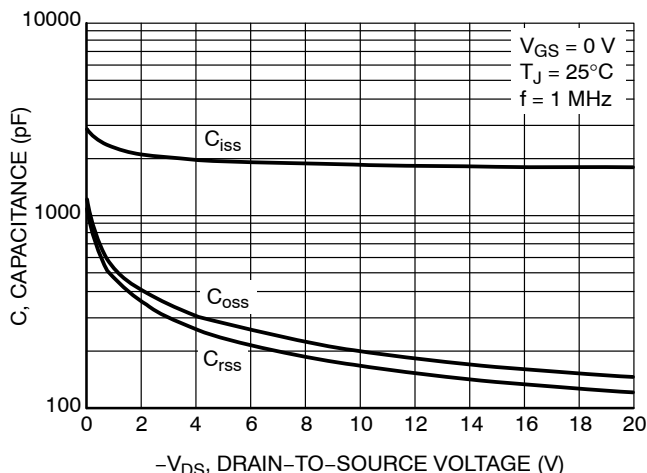


Figure 8. Capacitance Variation

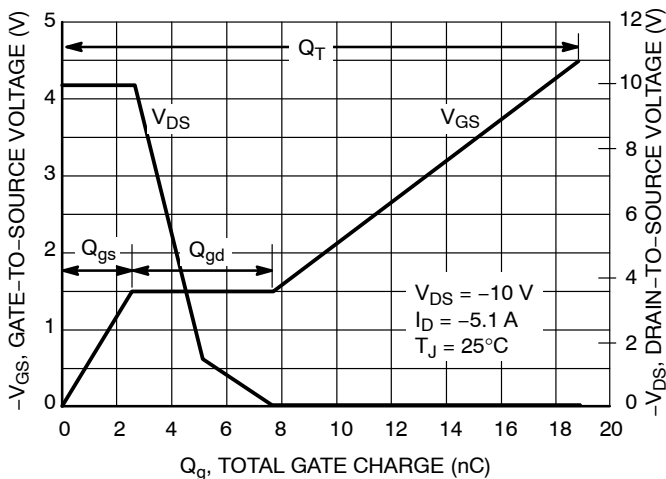


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

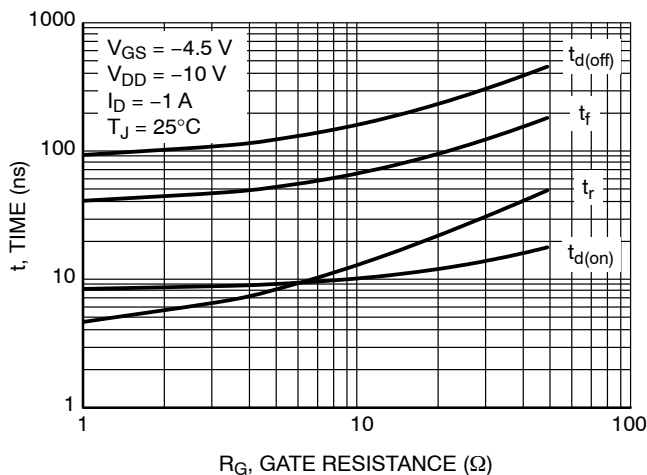


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

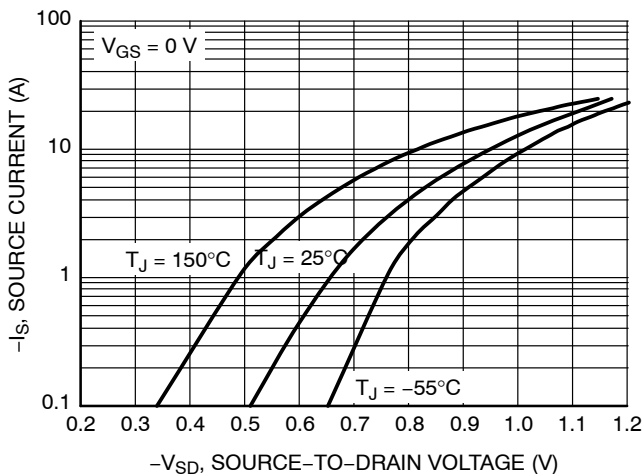


Figure 11. Diode Forward Voltage vs. Current

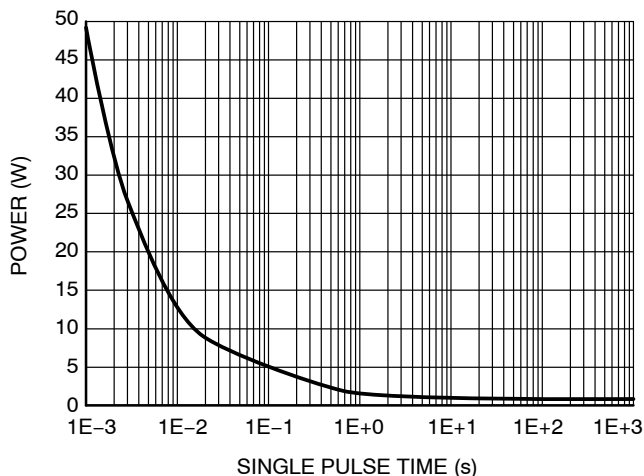


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS

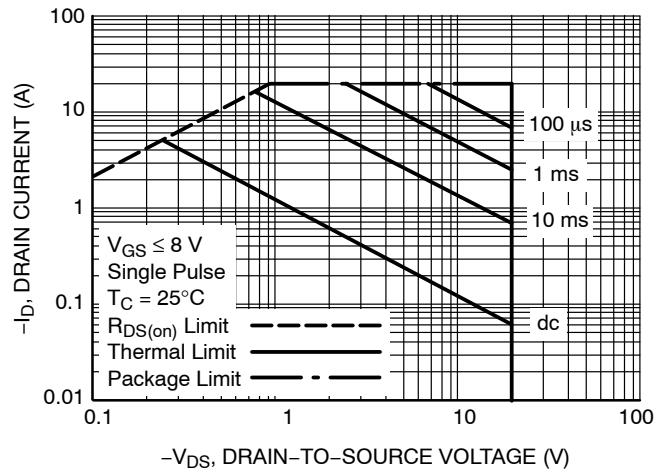


Figure 13. Maximum Rated Forward Biased Safe Operating Area

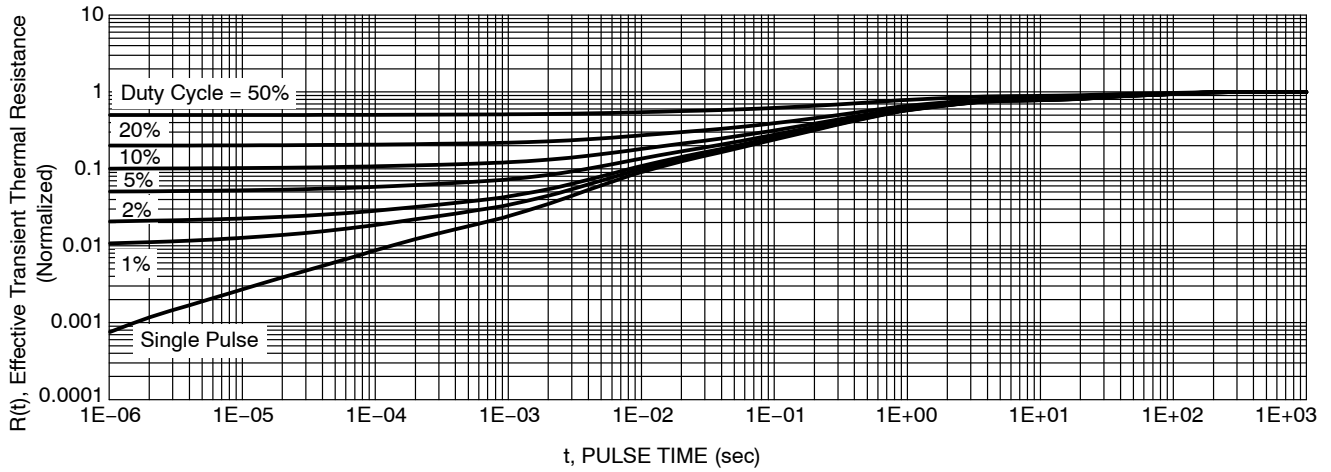
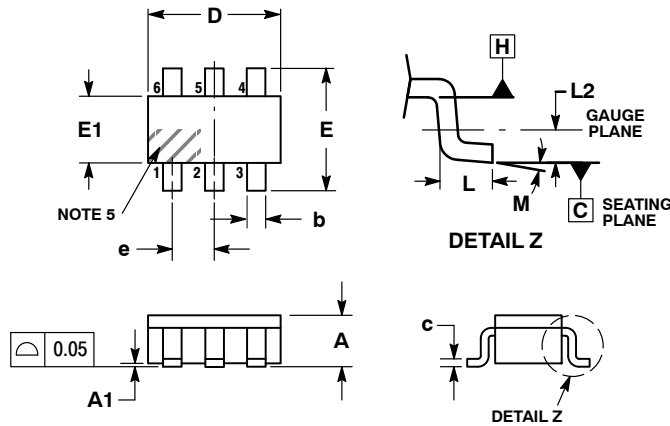


Figure 14. Thermal Response

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PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE V

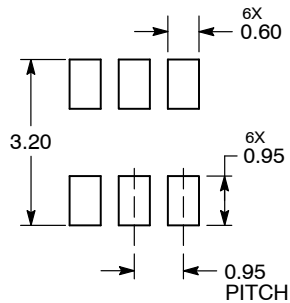


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	-		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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